Preliminary

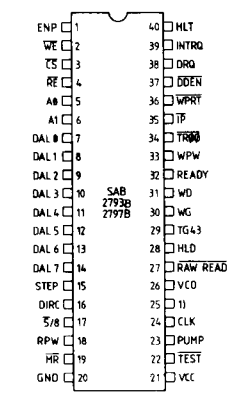
# SAB 2793B/2797B Advanced Floppy Disk Formatter/Controller Family

| Features | SAB 2793B | SAB 2797B |
|---|---|---|
| Single density (FM) | X | X |
| Double density (MFM) | X | X |
| True data bus | X | X |
| Side select output | | X |
| Internal CLK divide | X | |

- Improved On-chip PLL data separator
- On-chip write precompensation logic
- Single +5 V supply

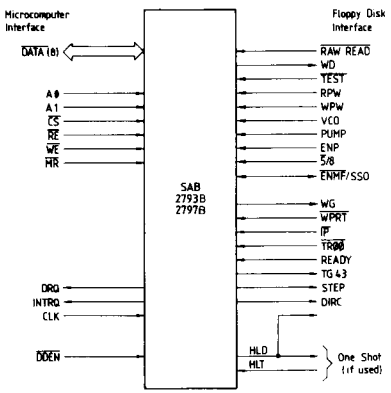
- Accommodates single and double-density formats
  IBM 3740 single density (FM)
  IBM System 34 double density (MFM)
- Automatic seek with verify
- Multiple sector read/write
- TTL-compatible
- Programmable control
  Selectable track-to-track access
  Head load timing
- Software-compatible with the SAB 179X floppy disk formatter/controller family
- Full functional- and pin-compatible to the SAB 2793A/2797A
- Soft sector format compatibility

**Pin Configuration**




1) SAB 2793B=ENMF
SAB 2797B=SSO

**Logic Symbol**




The SAB 2793B/2797B are floppy disk controllers in N-channel MOS LSI technology designed to interface with SAB 8080/8085/8051/8086/8088/80186/80188/80286 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems. Software-compatible with its predecessor, the SAB 179X, the device also contains a high-performance phase-lock-loop data separator as well as write precompensation logic.
When operating in double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼ "–8" floppy disk and microfloppy disk interface. 1.87

## Pin Definitions and Functions

| Symbol | Pin | Input (I) Output (O) | Function |
|---|---|---|---|
| ENP | 1 | I | ENABLE PRECOMP<br>A logic high on this input enables write precompensation to be performed on the write data output |
| $\overline{WE}$ | 2 | I | $\overline{WRITE\ ENABLE}$<br>A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low |
| $\overline{CS}$ | 3 | I | $\overline{CHIP\ SELECT}$<br>A logic low on this input selects the chip and enables computer communication with the device |
| $\overline{RE}$ | 4 | I | $\overline{READ\ ENABLE}$<br>A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low |
| AØ, A1 | 5, 6 | I | REGISTER SELECT LINES<br>These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:<br>$\overline{CS}$ A1 AØ $\overline{RE}$ $\overline{WE}$<br>Ø Ø Ø Status register Command register<br>Ø Ø 1 Track register Track register<br>Ø 1 Ø Sector register Sector register<br>Ø 1 1 Data register Data register |
| DALØ to DAL7 | 7–14 | I/O | DATA ACCESS LINES<br>8-bit bidirectional bus used for transfer of commands, status and data |
| STEP | 15 | O | STEP<br>The step output contains a pulse for each step |
| DIRC | 16 | O | DIRECTION<br>Direction output is active high when stepping in, active low when stepping out |
| $\overline{5}/8$ | 17 | I | 5¼", 8" SELECT<br>This input selects the internal VCO frequency for use with 5¼" drives or 8" drives |
| RPW | 18 | I | READ PULSE WIDTH<br>An external potentiometer tied to this input controls the phase comparator within the data separator |
| $\overline{MR}$ | 19 | I | $\overline{MASTER\ RESET}$<br>A logic low (50 µs min.) on this input resets the device and loads hex 03 into the command register. The "not ready bit" (status bit 7) is reset during $\overline{MR}$ active. When $\overline{MR}$ is brought to a logic high a restore command is executed, regardless of the state of the ready signal from the drive. Also hex 01 is loaded into sector register |
| $\overline{TEST}$ | 22 | I | $\overline{TEST}$<br>A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins |

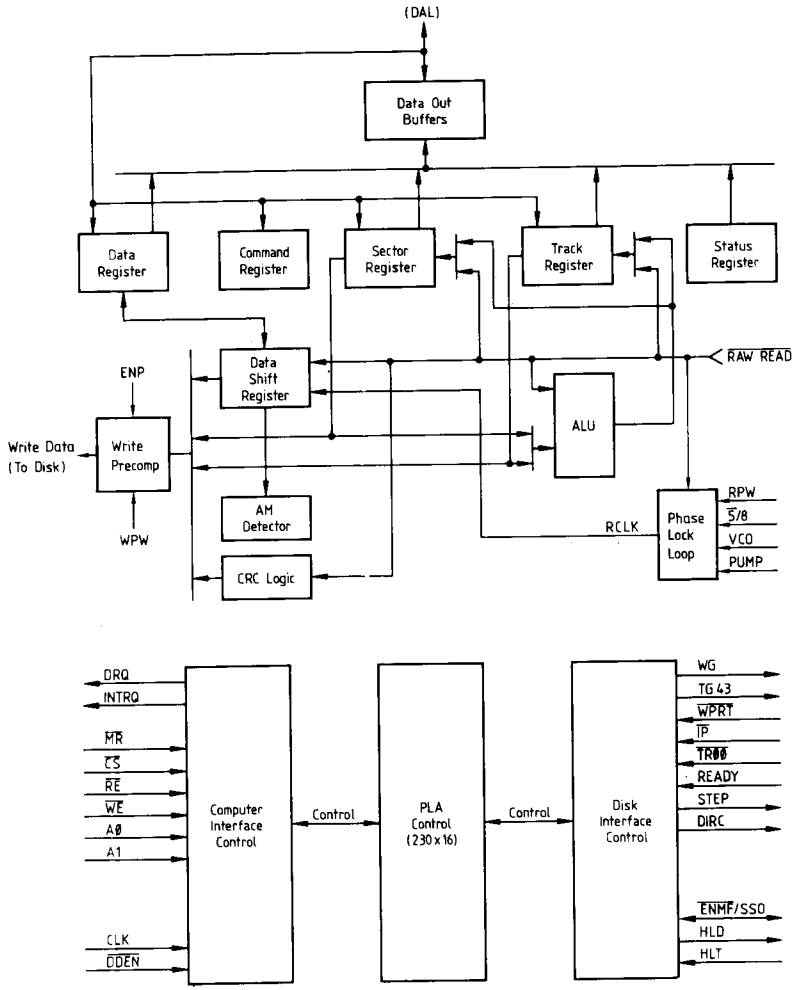
## Pin Definitions and Functions (cont'd)

| Symbol | Pin | Input (I) Output (O) | Function |
|---|---|---|---|
| PUMP | 23 | O | PUMP<br>High-impedance output signal which is forced high or low to increase/decrease the VCO frequency |
| CLK | 24 | I | CLOCK<br>This input requires a free-running, 50% duty cycle square-wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for minifloppies |
| $\overline{\text{ENMF}}$ | 25 | I | $\overline{\text{ENABLE MINIFLOPPY}}$ (SAB 2793B)<br>A logic low on this input enables an internal divide by 2 of the master clock. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on pin 24, this line must be left open or tied to a logic 1 |
| SSO | 25 | O | SIDE SELECT OUTPUT (SAB 2797B)<br>The logic level of the side select output is directly controlled by the U flag in type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the sector ID field. If they do not correspond, status bit 4 (RNF) is set. The side select output is only updated at the beginning of a type II or III command. It is forced to a logic 0 upon a master reset condition |
| VCO | 26 | – | VOLTAGE CONTROLLED OSCILLATOR<br>An external capacitor tied to this pin adjusts the VCO center frequency |
| $\overline{\text{RAW READ}}$ | 27 | I | $\overline{\text{RAW READ}}$<br>The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition |
| HLD | 28 | O | HEAD LOAD<br>The HLD output controls the loading of the read/write head against the media |
| TG43 | 29 | O | TRACK GREATER THAN 43<br>This output informs the drive that the read/write head is positioned between tracks 44 and 76. This output is valid only during read and write commands |
| WG | 30 | O | WRITE GATE<br>This output is made valid before writing is to be performed on the diskette |
| WD | 31 | O | WRITE DATA<br>MFM or FM output pulse per flux transition. WD contains the unique address marks as well as data and clock in both FM and MFM formats |
| READY | 32 | I | READY<br>This input indicates disk readiness and is sampled for a logic high before read or write commands are performed. If ready is low the read or write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of ready. The ready input appears in inverted format as status register bit 7 |

## Pin Definitions and Functions (cont'd)

| Symbol | Pin | Input (I) Output (O) | Function |
|---|---|---|---|
| WPW | 33 | I | WRITE PRECOMP WIDTH<br>An external potentiometer tied to his input controls the amount of delay in write precompensation mode |
| $\overline{TR00}$ | 34 | I | $\overline{TRACK\ 00}$<br>This input informs the SAB 2793B/2797B that the read/write head is positioned over track 00 |
| $\overline{IP}$ | 35 | I | $\overline{INDEX\ PULSE}$<br>This input informs the SAB 2793B/2797B when the index hole is encountered on the diskette |
| $\overline{WPRT}$ | 36 | I | $\overline{WRITE\ PROTECT}$<br>This input is sampled whenever a write command is received. A logic low terminates the command and sets the write protect status bit |
| $\overline{DDEN}$ | 37 | I | $\overline{DOUBLE\ DENSITY}$<br>This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected |
| DRQ | 38 | O | DATA REQUEST<br>This output indicates that the data register (DR) contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the computer through reading or loading the data register |
| INTRQ | 39 | O | INTERRUPT REQUEST<br>This output is set at the completion of any command and is reset when the status register is read or the command register is written to |
| HLT | 40 | I | HEAD LOAD TIMING<br>When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a single shot triggered by HLD |
| VCC | 21 | – | POWER SUPPLY (+5V) |
| VSS | 20 | – | GROUND (0V) |

**Block Diagram**



## General Description

The SAB 2793B/2797B are N-channel MOS LSI devices performing the functions of a Floppy Disk Formatter/Controller in a single-chip implementation. The SAB 2793B/2797B is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The SAB 2793B/2797B contains all the features of its predecessor, the SAB 179X, plus a high-performance phase-lock-loop data separator as well as write precompensation logic. In double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the SAB 179X and SAB 2793B/2797B designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical in each case, the actual pin assignments vary by only a few pins from any one to another.
The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The SAB 2793B/2797B is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 2793B/2797B is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads.
The SAB 2797B has a side select output to control double sided drives.

## Organization

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

**Data Shift Register (DSR)** – This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during read operations and transfers serial data to the Write Data output during write operations.

**Data Register (DR)** – This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel from the Data Shift Register to the Data Register. In disk write operations information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Track Register (TR)** – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Sector Register (SR)** – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)** – This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt command. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)** – This 8-bit register holds device status information. The meaning of the status bits depends on the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

**CRC Logic** – This logic is used to check or to generate the 16-bit Cycle Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$
The CRC includes all information starting with the address mark and up to the CRC character. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)** – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control** – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

**AM Detector** – The address mark detector detects ID, data and index address marks during read and write operations.

**Write Precompensation** – Enables write precompensation to be performed on the Write Data output.

**Data Separator** – A high-performance phase-lock-loop data separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

## Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer data, status, and control words out of or into the SAB 2793B/2797B. The DAL are three-state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.
When data transfer with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a read operation or $\overline{WE}$ during a write operation, are interpreted as selector for the following registers:

| A1 | A0 | READ | WRITE |
|---|---|---|---|
| 0 | 0 | Status Register | Command Register |
| 0 | 1 | Track Register | Track Register |
| 1 | 0 | Sector Register | Sector Register |
| 1 | 1 | Data Register | Data Register |

During direct memory access (DMA) types of data transfers between the Data Register of the SAB 2793B/2797B and the processor, the Data Request (DRQ) output is used for data transfer control. This signal also appears as status bit 1 during read and write operations.
In disk read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters have been lost by having transferred new data into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.

In disk write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.
Upon completion of every command an INTRQ is generated. INTRQ is reset either by reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.
The SAB 2793B/2797B has two modes of operation depending on the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or at 1 MHz for 5¼" drives.
On the SAB 2793B the $\overline{ENMF}$ input (Pin 25) can be used for controlling both, 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal divide by 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both, 5¼" and 8" configurations.
The internal VCO frequency must also be set to the proper value. The $\overline{5}/8$ input (Pin 17) is used to select data separator operation by internally dividing the read clock. When $\overline{5}/8 = 0$, 5¼" drive data separation is selected; when $\overline{5}/8 = 1$, 8" drive data separation is selected.

| Clock (24) | $\overline{ENMF}$ (25) | $\overline{5}/8$ (17) | Drive |
|---|---|---|---|
| 2 MHz | 1 | 1 | 8" |
| 2 MHz | 0 | 0 | 5¼" |
| 1 MHz | 1 | 0 | 5¼" |

All other conditions are invalid.

## Functional Description

The SAB 2793B/2797B is software-compatible with the SAB 179X series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the SAB 179X can be transferred to a SAB 2793B/2797B system without modification.
In addition to the SAB 179X, the SAB 2793B/2797B contains an internal data separator and write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both, data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp single shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second single shot tracks the precomp setting at approximately 3:1 to ensure adequate Write Data pulse widths to meet drive specifications.
Similarly, data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data single shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the read clock output (500 kHz for 8" drives). The VCO trimming capacitor (Pin 26) is adjusted to center frequency.
Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in operation. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the SAB 179X.
Other pins on the device also include pull-up resistors and may be left open to satisfy a logic 1 condition. These are: ENP, $\overline{5}/8$, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, $\overline{TEST}$, and $\overline{MR}$.

### General Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable either in FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logic 1. For MFM formats, $\overline{DDEN}$ should be placed to a logic 0. Sector lengths are determined at format time by the fourth byte in the ID field.

Sector Length Table*

| Sector Length Field (hex) | Number of Bytes in Sector (decimal) |
|---|---|
| 00 | 128 |
| 01 | 256 |
| 02 | 512 |
| 03 | 1024 |

* SAB 2797B may vary – see command summary.

The number of sectors per track as far as the SAB 2793B/2797B is concerned can vary between 1 and 255 sectors. The number of tracks as far as the SAB 2793B/2797B is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 byte with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 byte/sector with 26 sectors/track; or lengths of 1024 byte/sector with 8 sectors/track.

### General Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 2793B/2797B before the Write Gate signal can be activated. Writing is inhibited when the Write Protect input is logic low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.
For write operations, the SAB 2793B/2797B provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write Data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

### Ready

Whenever a read or write command (Type II or III) is received the SAB 2793B/2797B samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44–76.

### Write Precompensation

When operating in double density mode ($\overline{DDEN}$ = 0), the SAB 2793B/2797B has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10k) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.
Setting the write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since the Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

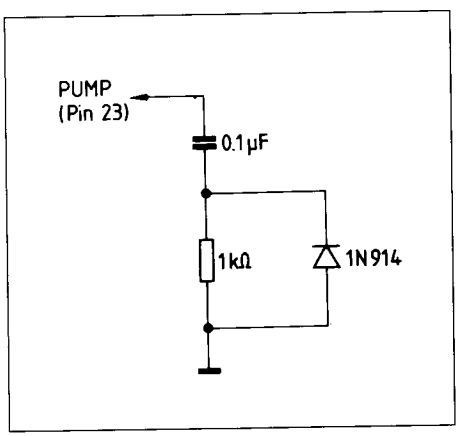
### Data Separation

The SAB 2793B/2797B can operate with either an external data separator or its own internal recovery circuit. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.
To program the SAB 2793B/2797B for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g. 4.0 MHz for 8" double density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the PUMP output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.
For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a logic 0 for the adjustment procedure.
A 50k Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external, variable capacitor of typically 5 to 60 pF is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate data rate (500 kHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the $\overline{5/8}$ line is held high or the adjustment times above will be doubled.

### VCO Operation

After adjustments have been made, the $\overline{TEST}$ pin is returned to a logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.
The PUMP output (Pin 23) consists of positive and negative pulses. Their duration is equivalent to the phase difference of incoming Data versus VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.
The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.
A first-order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as response to normal frequency shift i.e. the lock-up time. A balance must be accomplished between the two conditions to inhibit overresponsiveness to jitter and to prevent an extremely wide lock-up response leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:




Since 5¼" Drives operate at exactly one-half the data rate (250 Kbyte/s) the above capacitor should be doubled to 0.2 or 0.22 µF.

## Command Summary

| | | Commands for SAB 2793B | | | | | | | | Commands for SAB 2797B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bits | | | | | | | | Bits | | | | | | | |
| Type | Command | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I | Restore | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| I | Seek | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| I | Step | 0 | 0 | 1 | T | h | V | $r_1$ | $r_0$ | 0 | 0 | 1 | T | h | V | $r_1$ | $r_0$ |
| I | Step-in | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ |
| I | Step-out | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ |
| II | Read sector | 1 | 0 | 0 | m | S | E | C | 0 | 1 | 0 | 0 | m | L | E | U | 0 |
| II | Write Sector | 1 | 0 | 1 | m | S | E | C | $a_0$ | 1 | 0 | 1 | m | L | E | U | $a_0$ |
| III | Read Address | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 | 1 | 1 | 0 | 0 | 0 | E | U | 0 |
| III | Read Track | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 | 1 | 1 | 1 | 0 | 0 | E | U | 0 |
| III | Write Track | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 | 1 | 1 | 1 | 1 | 0 | E | U | 0 |
| IV | Force Interrupt | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

## Flag Summary

| Command Type | Bit | Description |
|---|---|---|
| I | $r_1$, $r_0$ = Stepping Motor Rate | See page 13 for details |
| I | V = Track Number Verify Flag | V = 0, No verify<br>V = 1, Verify on destination track |
| I | h = Head Load Flag | h = 0, Unload head at beginning<br>h = 1, Load head at beginning |
| I | T = Track Update Flag | T = 0, No update<br>T = 1, Update track register |
| II & III | $a_0$ = Data Address Mark | $a_0$ = 0, FB (DAM)<br>$a_0$ = 1, F8 (deleted DAM) |
| II | C = Side Compare Flag | C = 0, Disable side compare<br>C = 1, Enable side compare |
| II & III | U = Update SSO | U = 0, Update SSO to 0<br>U = 1, Update SSO to 1 |
| II & III | E = 15 ms Delay | E = 0, No 15 ms delay<br>E = 1, 15 ms delay (30 ms for 1 MHz clock) |
| II | S = Side Compare Flag | S = 0, Compare for side 0<br>S = 1, Compare for side 1 |
| II | L = Sector Length Flag<br>L = 1 (implicit) for SAB 2793B | |
| II | m = Multiple Record Flag | m = 0, Single record<br>m = 1, Multiple records |
| IV | Ix = Interrupt Conditions Flags<br>I0 = 1: Interrupt on Not Ready to Ready Transition<br>I1 = 1: Interrupt on Ready to Not Ready Transition<br>I2 = 1: Interrupt on Next Index Pulse<br>I3 = 1: Immediate Interrupt Requires a Reset *<br>I3–I0 = 0: Terminate with No interrupt (INTRQ) | |

| | LSB's Sector Length in ID Field | | | |
|---|---|---|---|---|
| | 00 | 01 | 10 | 11 |
| L = 0 | 256 | 512 | 1024 | 128 |
| L = 1 | 128 | 256 | 512 | 1024 |

* See Type IV command description for further information.

## Status Register Summary

| Bit | All Type I Commands | Read Address | Read Sector | Read Track | Write Sector | Write Track |
|---|---|---|---|---|---|---|
| S7 | NOT READY | NOT READY | NOT READY | NOT READY | NOT READY | NOT READY |
| S6 | WRITE PROTECT | 0 | 0 | 0 | WRITE PROTECT | WRITE PROTECT |
| S5 | HEAD LOADED | 0 | RECORD TYPE | 0 | 0 | 0 |
| S4 | SEEK ERROR | RNF | RNF | 0 | RNF | 0 |
| S3 | CRC ERROR | CRC ERROR | CRC ERROR | 0 | CRC ERROR | 0 |
| S2 | TRACK 00 | LOST DATA | LOST DATA | LOST DATA | LOST DATA | LOST DATA |
| S1 | INDEX | DRQ | DRQ | DRQ | DRQ | DRQ |
| S0 | BUSY | BUSY | BUSY | BUSY | BUSY | BUSY |

**Status for Type I Commands**

| Bit | Name | Meaning |
|---|---|---|
| S7 | NOT READY | This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically ORed with $\overline{MR}$. |
| S6 | WRITE PROTECT | When set, indicates that Write Protect in activated. This bit is an inverted copy of $\overline{WPRT}$ input. |
| S5 | HEAD LOADED | When set, it indicates that the head is loaded and engaged. This bit is a logical AND of HLD and HLT signals. |
| S4 | SEEK ERROR | When set, the desired track was not verified. This bit is reset to 0 when updated. |
| S3 | CRC ERROR | CRC encountered in ID field. |
| S2 | TRACK 00 | When set, indicates that Read/Write head is positioned to Track 00. This bit is an inverted copy of the $\overline{TR00}$ input. |
| S1 | INDEX | When set, indicates that index mark is detected from drive. This bit is an inverted copy of the $\overline{IP}$ input. |
| S0 | BUSY | When set, command is in progress. When reset, no command is in progress. |

**Status for Type II and III Commands**

| Bit | Name | Meaning |
|---|---|---|
| S7 | NOT READY | This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and ORed with $\overline{MR}$. The Type II and III Commands will not execute unless the drive is ready. |
| S6 | WRITE PROTECT | For Read Record: not used. For Read Track: not used. On any Write: It indicates a Write Protect. This bit is reset, when updated. |
| S5 | RECORD TYPE | For Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. For any Write: forced to a zero. |
| S4 | RECORD NOT FOUND (RNF) | When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated. |
| S3 | CRC ERROR | If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated. |
| S2 | LOST DATA | When set, it indicates that the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. |
| S1 | DATA REQUEST | This bit is a copy of the DRQ output. When set, it indicates that the DR is full on a read operation or the DR is empty on a write operation. This bit is reset to zero when updated. |
| S0 | BUSY | When set, command is under execution. When reset, no command is under execution. |

## Summary of Adjustment Procedures

**Write Precompensation**

1) Set $\overline{TEST}$ (Pin 22) to a logic high.
2) Strobe $\overline{MR}$ (Pin 19).
3) Set $\overline{TEST}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{TEST}$ (Pin 22) to a logic high.

**Data Separator**

1) Set $\overline{TEST}$ (Pin 22) to a logic high.
2) Strobe $\overline{MR}$ (Pin 19). Ensure that $\overline{5}/8$, and $\overline{DDEN}$ are set properly.
3) Set $\overline{TEST}$ (Pin 22) to a logic low.
4) Observe pulse width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250 ns for 8" DD, 500 ns for 5¼" DD, etc.).
6) Observe frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for data rate (500 kHz for 8" DD, 250 kHz for 5¼" DD, etc.).
8) Set $\overline{TEST}$ (Pin 22) to a logic high.
NOTE: To maintain internal VCO operation, insure that $\overline{TEST}$ = 1 whenever a master reset pulse is applied.

## Status Register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits is updated or cleared for the new command. If the Force Interrupt command is received while a current command is under execution, the Busy status bit is reset, and the rest of the status bits is left unchanged. If the Force Interrupt command is received while there is no current command under execution, the Busy Status bit is reset and the rest of the status bits is updated or cleared as after a Type I command.
The user can optionally read the Status Register through program control or by using the DRQ line with DMA or interrupt methods. When the Data Register is read, the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes the reset of both DRQs. The Busy bit in the status may be monitored by a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because reading the Status Register to determine the condition of Busy will reset the INTRQ line.

The format of the Status Register is shown below:

| (BITS) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

Status varies according to the type of command executed as shown on page 11.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

| Operation | Next Operation | Delay Req'd. | |
|---|---|---|---|
| | | FM | MFM |
| Write to Command Reg. | Read Busy Bit (Status Bit 0) | 12 µs | 6 µs |
| Write to Command Reg. | Read Status Bits 1-7 | 28 µs | 14 µs |
| Write to Any Register | Read from Diff. Register | 0 | 0 |

Times double when clock = 1 MHz

## Command Description

The SAB 2793B/2797B will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The only exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized on page 10.

## Type I Commands

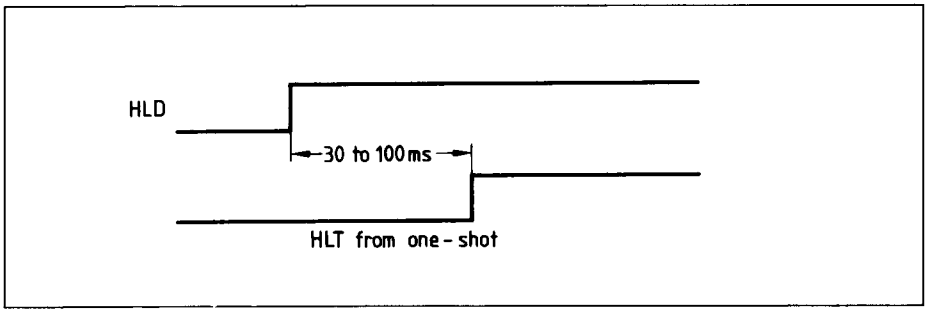
The Type I commands include the Restore, Seek, Step, Step-In and Step-Out commands. Each of the Type I commands contains a rate field ($r_0$, $r_1$) which determines the stepping motor rate.
A 2 µs (MFM) or 4 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the Direction output. The chip steps the drive in the same direction it has been stepped previously, unless the command changes direction. The Direction signal is active high when stepping in and low when stepping out. The Direction signal has been valid 12 µs before the first stepping pulse is generated. The rates can be applied to a Step-Direction motor through the device interface.

**Stepping Rates**

| CLK | | 2 MHz | 1 MHz |
|---|---|---|---|
| r1 | r0 | $\overline{TEST}$ = 1 | $\overline{TEST}$ = 1 |
| 0 | 0 | 3 ms | 6 ms |
| 0 | 1 | 6 ms | 12 ms |
| 1 | 0 | 10 ms | 20 ms |
| 1 | 1 | 15 ms | 30 ms |

After the last directional step, additional 15 milliseconds of head settling time are generated if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head setting time if the E flag is set in any Type II or III command.
When a Seek, Step or Restore command is executed an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond setting time after the head is loaded against the media. The track number from the first encountered ID field is compared against the contents of the Track Register. If the track numbers correspond and the ID field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. The SAB 2793B/2797B must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the Seek Error is set and an INTRQ is generated. If V = 0, no verification is performed. The Head Load (HLD) output controls the movement of the Read/Write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the Verify flag is set (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with h = 0 and V = 0, or if the SAB 2793B/2797B is in an idle state (non-busy) and 15 index pulses have occurred.
Head Load timing (HLT) is an input to the SAB 2793B/2797B which is used for the head engage time.
When HLT= 1, the SAB 2793B/2797B assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a single shot. The output of the single shot is then used for HLT and supplied as an input to the SAB 2793B/2797B.

**Head Load Timing**




When both HLD and HLT are true, the SAB 2793B/2797B will read from or write to the media. The "AND" of HLD and HLT appears as status bit 5 in Type I status.

Summary of the Type I commands:
If h = 0 and V = 0, HLD is reset.
If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay.
If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms delay occurs, and the SAB 2793B/2797B waits for HLT to be true.
If h = 1 and V = 1, HLD is set at the beginning of the command.
Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 2793B/2797B waits for HLT to occur.
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

**Restore (Seek Track 0)**

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeros and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the $r_1$ $r_0$ field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeros and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the SAB 2793B/2797B terminates operation, interrupts and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is always executed when $\overline{MR}$ goes from an active to an inactive state.

**Seek**

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The SAB 2793B/2797B will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command. Note: When using multiple drives, the Track Register must be updated for the drive selected before seek commands are issued.

**Step**

Upon receipt of this command, the SAB 2793B/2797B issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous Step command. After a delay determined by the $r_1$ $r_0$ field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

**Step-In**

Upon receipt of this command, the SAB 2793B/2797B issues one stepping pulse towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the $r_1$ $r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

**Step-Out**

Upon receipt of this command, the SAB 2793B/2797B issues one stepping pulse towards track 0. If the T flag is on, the Track Register is decremented by

one. After a delay determined by the $r_1$ $r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

## Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading a Type II command into the Command Register the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag is 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 ms delay. If the E flag is 0, the head is loaded and HLT is sampled without a 15 ms delay.
When an ID field is located on the disk, the SAB 2793B/2797B compares the track number on the ID field with the Track Register. If they do not match, the next encountered ID field is read and a comparison is again made. If there has been a match, the Sector Number of the ID field is compared with the Sector Register. If there is no sector match, the next encountered ID field is read off the disk and again compared. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The SAB 2793B/2797B must find an ID field with a track number, sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record-Not-Found status bit is set (Status bit 4) and the command is terminated with an interrupt. Each of the Type II commands contains an m flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the termination of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The SAB 2793B/2797B will continue to read or write multiple records and update the Sector Register in numerical ascending sequence until the Sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.
For example: If the SAB 2793B/2797B is instructed to read sector 27 and there are only 26 sectors on the track, the Sector Register exceeds the number available. The SAB 2793B/2797B will search for 5 disk revolutions, interrupt out, reset Busy, and set the Record-Not-Found status bit.

The Type II commands for the SAB 2793B also contain Side Select Compare flags. When C = 0 (bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the S flag (bit 3). If the S flag corresponds to the side number recorded in the ID field, the SAB 2793B/2797B continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.
The Type II and III commands for the SAB 2797B contains a Side Select flag (bit 1). When U = 0, SSO is updated to 0. Similary, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not correspond within 5 revolutions the interrupt line is made active and the RNF status bit is set.
The SAB 2797B Read Sector and Write Sector commands include an L flag. The L flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the L flag should be set to a one.

### Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 byte in single density and 43 byte in double density after the last ID field CRC byte; if not, the ID field search is repeated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the read operation, the type of Data Address Mark encountered in the field is recorded in the Status Register (bit 5) as shown:

| Status Bit 5 | |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

**Write Sector**

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The SAB 2793B/2797B counts off 11 bytes in single density and 22 bytes in double density from the CRC field, and the Write Gate (WG) output is made active if the DRQ is serviced (i.e. the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is written on the disk as determined by the $a_0$ field of the command as shown below:

| $a_0$ | Data Address Mark (Bit 0) |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

The SAB 2793B/2797B then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of hex FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ is set between 8 and 12 µs after the last CRC byte has been written. For partial sector writing, the proper method is to write the data and fill the balance with zeros. By letting the chip fill the zeros, errors may be masked by the Lost Data status and improper CRC bytes.

## Types III Commands

**Read Address**

Upon receipt of the Read Address command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read from the disk, and the six data bytes of the ID field are assembled and transferred to the DR. And DRQ is generated for each byte. The six bytes of the ID field are shown below:

| Track Address | Side number | Sector address | Sector length | CRC 1 | CRC 2 |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

Although the CRC characters are transferred to the computer, the SAB 2793B/2797B checks for validity and the CRC Error status bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy status bit is reset.

**Read Track**

Upon receipt of the Read Track command, the head is loaded, and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All gap, header, and data bytes are assembled and transferred to the Data Register. DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the termination of the command.
This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM. If an address mark does not appear on schedule with the Lost Data status flag being set, the ID AM, ID field, ID CRC bytes, DAM, data and data CRC bytes for each sector will be correct. The gap bytes may be read incorrectly during write splice time because of synchronization.

**Write Track Formatting the Disk**

Formatting the disk is a comparatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished

by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The data request is activated immediately upon receipt of command, but writing will not start before the first byte is loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated by making the device not busy. The Lost Data status bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted.

This sequence continues from one index mark to the next. Normally, whatever data pattern appears in the Data Register, it is written on the disk with a normal clock pattern. However, if the SAB 2793B/2797B detects a data pattern of F5 thru FE in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 byte.

**Control Bytes for Initialization**

| Data Pattern in DR (hex) | SAB 2793B/2797B Interpretation in FM ($\overline{DDEN}$ = 1) | SAB 2793B/2797B Interpretation in MFM ($\overline{DDEN}$ = 0) |
|---|---|---|
| 00 thru F4 | Write 00 thru F4 with CLK = FF | Write 00 thru F4, in MFM |
| F5 | Not Allowed | Write A1[1] in MFM, Preset CRC |
| F6 | Not Allowed | Write C2[2] in MFM |
| F7 | Generate 2 CRC Bytes | Generate 2 CRC Bytes |
| F8 thru FB | Write F8 thru FB, CLK = C7, Preset CRC | Write F8 thru FB, in MFM |
| FC | Write FC with CLK = D7 | Write FC in MFM |
| FD | Write FD with CLK = FF | Write FD in MFM |
| FE | Write FE, CLK = C7, Preset CRC | Write FE in MFM |
| FF | Write FF with CLK = FF | Write FF in MFM |

[1] Missing clock transition between bits 4 and 5
[2] Missing clock transition between bits 3 and 4

## Type IV Commands

The Force Interrupt command is generally used to terminate a multiple sector Read or Write command or to ensure Type I status in the Status Register. This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit set) the command will be terminated and the Busy status bit reset. The lower four bits of the command determine the conditional interrupt as follows:
I0: Not-Ready to Ready Transition
I1: Ready to Not-Ready Transition
I2: Every Index Pulse
I3: Immediate Interrupt
The conditional interrupt is enabled when the corresponding bit positions of the command (I3–I0) are set to a1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.
If I3–I0 are all set to zero (hex D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status register or writing to the Command Register will not automatically clear the interrupt. The hex D0 is the only command that will enable the immediate interrupt (hex D8) to clear on a subsequent load Command Register or read Status Register operation. Follow a hex D8 with a D0 command. Wait 8 µs (double density) or 16 µs (single density) before issuing a new command after a Force Interrupt command has been issued (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt. Forced interrupt stops any command at the end of an internal microinstruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are completed (CRC calculations, comparisons, etc.). More than one condition may be set at a time. If, for example, the Ready to Not-Ready condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command will be hex DA. The OR function is performed so that either a Ready to Not-Ready or the next Index Pulse will cause an interrupt condition.

## Formats

**IBM 3740 Format – 128 Byte/Sector (8")**

Shown below is the IBM single-density format with 128 byte/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

| Number of Bytes | Hex Value of Byte Written |
|---|---|
| 40 | FF (or 00)[3] |
| 6 | 00 |
| 1 | FC (Index Mark) |
| 26 | FF (or 00) |
| [1] 6 | 00 |
| 1 | FE (ID Address Mark) |
| 1 | Track Number |
| 1 | Side Number (00 or 01) |
| 1 | Sector Number (1 thru 1A) |
| 1 | 00 |
| 1 | F7 (2 CRCs Written) |
| 11 | FF (or 00) |
| 6 | 00 |
| 1 | FB (Data Address Mark) |
| 128 | Data (E5) |
| 1 | F7 (2 CRCs Written) |
| 27 | FF (or 00) |
| 247[2] | FF (or 00) |

**IBM System 34 Format – 256 Byte/Sector (8")**

Shown in the following table is the IBM double-density format with 256 byte/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

| Number of Bytes | Hex Value of Byte Written |
|---|---|
| 80 | 4E |
| 12 | 00 |
| 3 | F6 (Writes C2) |
| 1 | FC (Index Mark) |
| 50 | 4E |
| [1] 12 | 00 |
| 3 | F5 (Writes A1) |
| 1 | FE (ID Address Mark) |
| 1 | Track Number (0 through 4C) |
| 1 | Side Number (0 or 1) |
| 1 | Sector Number (1 through 1A) |
| 1 | 01 (Sector Length) |
| 1 | F7 (2 CRCs Written) |
| 22 | 4E |
| 12 | 00 |
| 3 | F5 (Writes A1) |
| 1 | FB (Data Address Mark) |
| 256 | Data (E5) |
| 1 | F7 (2 CRCs Written) |
| 54 | 4E |
| 598[2] | 4E |

[1] Write bracketed field 26 times.
[2] Continue writing until SAB 2793B/2797B interrupts out. Approx. 247 (598) byte.
[3] Optional '00' on SAB 2797B only is allowed.

**Recommended – 128 Byte/Sector (Minidiskette)**

Shown below is the recommended single-density format with 128 byte/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

| Number of Bytes | Hex Value of Byte Written |
|---|---|
| 40 | FF (or 00) |
| [1] 6 | 00 |
| 1 | FE (ID Address Mark) |
| 1 | Track Number |
| 1 | Side Number (00 or 01) |
| 1 | Sector Number (1 through 10) |
| 1 | 00 (Sector Length) |
| 1 | F7 (2 CRCs Written) |
| 11 | FF (or 00) |
| 6 | 00 |
| 1 | FB (Data Address Mark) |
| 128 | Data (E5) |
| 1 | F7 (2 CRCs Written) |
| 10 | FF (or 00) |
| 349[2] | FF (or 00) |

**Recommended – 256 Byte/Sector (Minidiskette)**

Shown below is the recommended double-density format with 256 byte/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

| Number of Bytes | Hex Value of Byte Written |
|---|---|
| 60 | 4E |
| [1] 12 | 00 |
| 3 | F5 (Writes A1) |
| 1 | FE (ID Address Mark) |
| 1 | Track Number (0 through 4C) |
| 1 | Side Number (0 or 1) |
| 1 | Sector Number (1 through 10) |
| 1 | 01 (Sector Length) |
| 1 | F7 (2 CRCs Written) |
| 22 | 4E |
| 12 | 00 |
| 3 | F5 (Write A1) |
| 1 | FB (Data Address Mark) |
| 256 | Data (E5) |
| 1 | F7 (2 CRCs Written) |
| 24 | 4E |
| 718[2] | 4E |

**Non-Standard Formats**

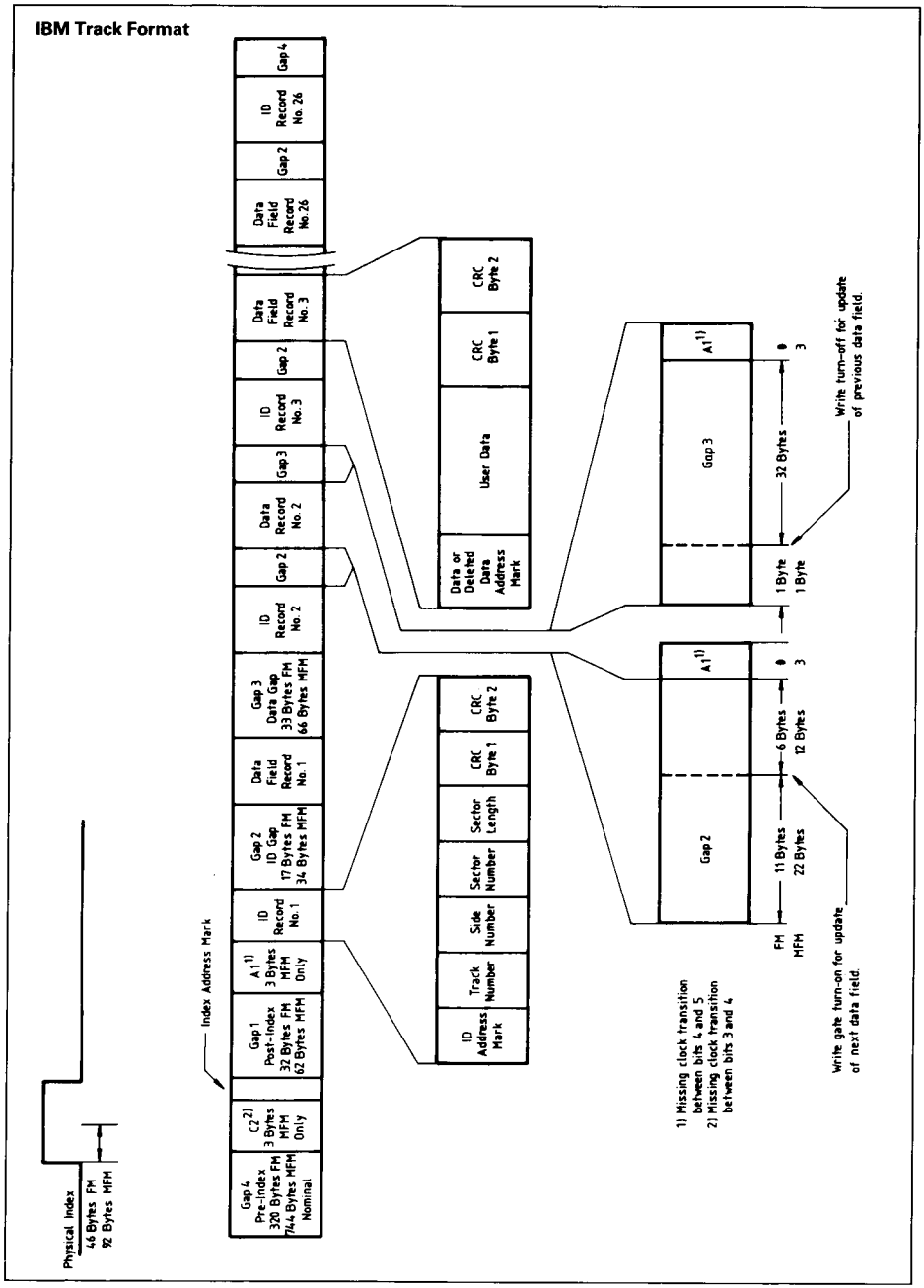
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1. Sector size must be 128, 256, 512 or 1024 byte.
2. Gap 2 cannot be varied from the recommended format.
3. 3 bytes of A1 must be used in MFM.

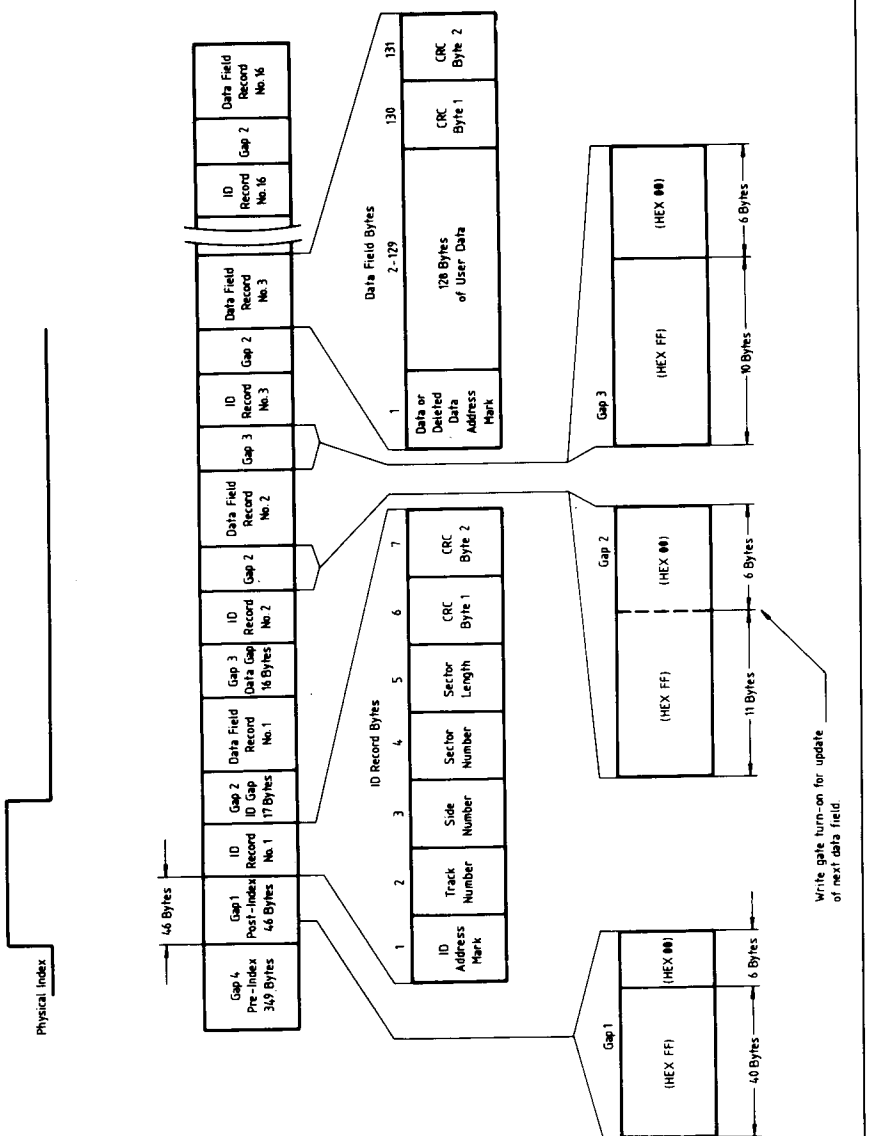
In addition, the Index Address Mark is not required for operation by the SAB 2793B/2797B. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 2793B/2797B operation, however, PLL lock-up time, motor speed variation, write-splice area, etc., will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format should be used for highest system reliability.

| | FM | MFM |
|---|---|---|
| Gap I | 16 Byte FF | 32 Byte 4E |
| Gap II | 11 Byte FF | 22 Byte 4E |
| [3] | 6 Byte 00 | 12 Byte 00 |
| | | 3 Byte A1 |
| Gap III | 10 Byte FF | 24 Byte 4E |
| [4] | 4 Byte 00 | 8 Byte 00 |
| | | 3 Byte A1 |
| Gap IV | 16 Byte FF | 16 Byte 4E |

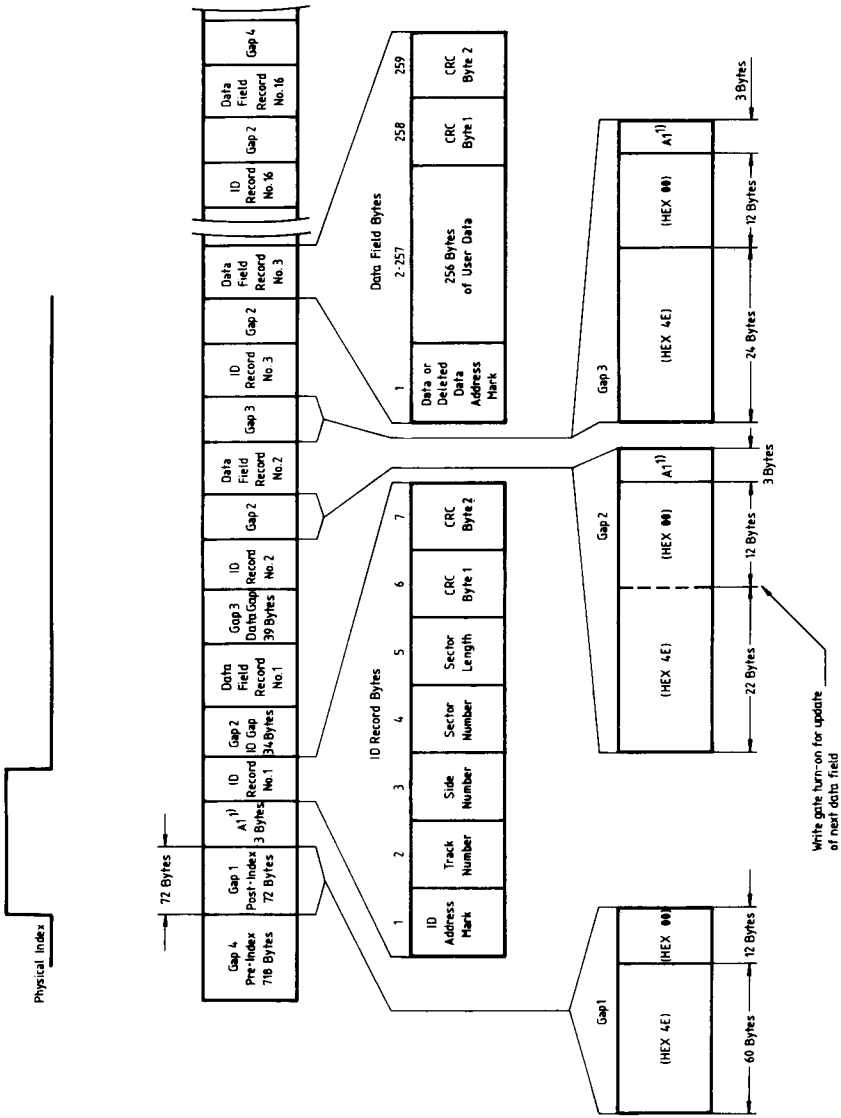
[1] Write bracketed field 16 times.
[2] Continue writing until SAB 2793B/2797B interrupts out. Approx. 349 (718) byte.
[3] Byte counts must be exact.
[4] Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.


IBM Track Format
Physical Index
46 Bytes FM
92 Bytes MFM
Gap 4 Pre-Index 320 Bytes FM 744 Bytes MFM Nominal
C2) 3 Bytes MFM Only
Gap 1 Post-Index 32 Bytes FM 62 Bytes MFM
A1) 3 Bytes MFM Only
ID Record No. 1
Gap 2 ID Gap 17 Bytes FM 34 Bytes MFM
Data Field Record No. 1
Gap 3 Data Gap 33 Bytes FM 66 Bytes MFM
ID Record No. 2
Gap 2
Data Record No. 2
Gap 3
ID Record No. 3
Gap 2
Data Field Record No. 3
Data Field Record No. 26
Gap 2
ID Record No. 26
Gap 4
Index Address Mark
ID Address Mark
Track Number
Side Number
Sector Number
Sector Length
CRC Byte 1
CRC Byte 2
Data or Deleted Data Address Mark
User Data
CRC Byte 1
CRC Byte 2
A1)
Gap 2
A1)
Gap 3
1 Byte
1 Byte
0
3
6 Bytes
12 Bytes
32 Bytes
0
3
11 Bytes
22 Bytes
FM
MFM
Write turn-off for update of previous data field.
Write gate turn-on for update of next data field.
1) Missing clock transition between bits 4 and 5
2) Missing clock transition between bits 3 and 4

**Recommended Single-Density Format (Minidiskette)**



**Recommended Double-Density Format (Minidiskette)**




1) FD writes A1 in MFM with missing clocks between bits 4 and 5.

## Absolut Maximum Ratings[1]

| | |
|---|---|
| Ambient Temperature Under Bias | 0 to + 70°C |
| Storage Temperature | −65 to +150°C |
| Voltage on Any Pin with Respect to Ground (VSS) | −0.5 to +7V |
| Power Dissipation | 2W |

## DC Characteristics

TA = 0 to 70°C; VCC = +5%; VSS = 0V

| Symbol | Parameter | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| IIL 1 | Input Leakage Current[2] | – | – | 10 | µA | VIN = VCC |
| IIL 2 | Internal Leakage Current[2] | 100 | – | 1700 | µA | VIN = 0V |
| IOL | Output Leakage Current | – | – | 10 | µA | VOUT = VCC |
| VIH | Input High Voltage | 2.0 | – | – | V | – |
| VIL | Input Low Voltage | – | – | 0.8 | V | – |
| VOH | Output High Voltage | 2.4 | – | – | V | IOH = −100 µA |
| VOL | Output Low Voltage | – | – | 0.45 | V | IOL = 1.6 mA |
| VOHP | Output High PUMP | 2.2 | – | – | V | IOHP = −1.0 mA |
| VOLP | Output Low PUMP | – | – | 0.2 | V | IOLP = +1.0 mA |
| ICC | Supply Current | – | 70 | 150 | mA | All outputs open |

## Capacitance[3]

| Symbol | Parameter | Limit Value (max.) | Unit | Test Condition |
|---|---|---|---|---|
| CIN | Input Capacitance | 15 | pF | Unmeasured pins returned to GND |
| COUT | Output Capacitance | 15 | pF | |

[1] Stresses above those listed under „Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] IIL 1 applies to normal inputs, IIL 2 to inputs with internal pull-up resistors on pins 1, 17, 19, 22, 36, 37, and 40. Also pin 25 on SAB 2793B.

[3] This parameter is periodically sampled and not 100% tested.

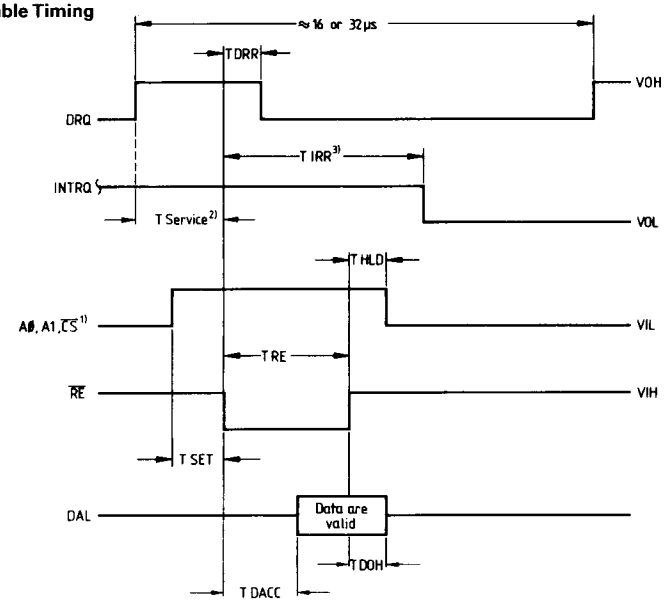
## AC Characteristics

TA = 0 to 70°C; VCC = +5V ±5%; VSS = 0V.
All timing readings at VOL = 0.8 V and VOH = 2.0 V.

**Read Enable Timing**

| Symbol | Parameter | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TSET | Setup Addr. and $\overline{CS}$ to $\overline{RE}$ | 50 | – | – | ns | – |
| THLD | Hold Addr. and $\overline{CS}$ from $\overline{RE}$ | 10 | – | – | ns | – |
| TRE | $\overline{RE}$ Pulse Width | 200 | – | – | ns | CL = 50 pF |
| TDRR | DRQ Reset from $\overline{RE}$ | – | 100 | 200 | ns | – |
| TIRR | INTRQ Reset from $\overline{RE}$ | – | 500 | 3000 | ns | – |
| TDACC | Data Valid from $\overline{RE}$ | – | 100 | 200 | ns | CL = 50 pF |
| TDOH | Data Hold from $\overline{RE}$ | 20 | – | 150 | ns | CL = 50 pF |

**Read Enable Timing**




DRQ rising edge: Indicates that the data register has assembled data.
DRQ falling edge: Indicates that the data register was read.
INTRQ rising edge: Occurs at end of command.
INTRQ falling edge: Indicates that the status register was read.

1) $\overline{CS}$ may be permanently tied low if desired.

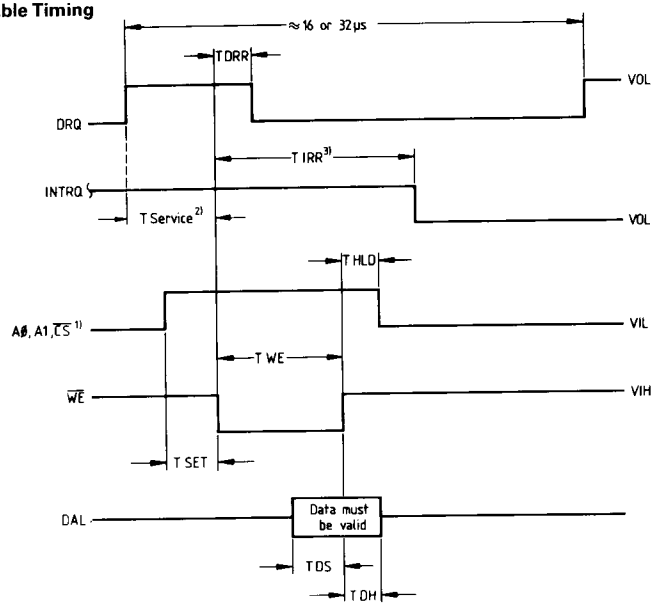
2) T Service (worst case)
– FM = 27.5 µs
– MFM = 13.5 µs

3) Time doubles when CLK = 1 MHz.

**Write Enable Timing**

| Symbol | Parameter | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TSET | Setup Addr. and $\overline{CS}$ to $\overline{WE}$ | 50 | – | – | ns | – |
| THLD | Hold Addr. and $\overline{CS}$ from $\overline{WE}$ | 10 | – | – | ns | – |
| TWE | $\overline{WE}$ Pulse Width | 200 | – | – | ns | – |
| TDRR | DRQ Reset from $\overline{WE}$ | – | 100 | 200 | ns | – |
| TIRR | INTRQ Reset from $\overline{WE}$ | – | 500 | 3000 | ns | – |
| TDS | Data Setup to $\overline{WE}$ | 150 | – | – | ns | – |
| TDH | Data Hold from $\overline{WE}$ | 50 | – | – | ns | – |

**Write Enable Timing**




DRQ rising edge: Indicates that the data register is empty.
DRQ falling edge: Indicates that the data register is loaded.
INTRQ rising edge: Indicates the end of a command.
INTRQ falling edge: Indicates that the command register is written to.

1) $\overline{CS}$ may be permanently tied low if desired. When writing Data into Sector, Track or Data Register, the User cannot read this register until at least 4 µs in MFM after the rising edge of $\overline{WE}$. When writing into the Command Register status is not valid until some 28 µs in FM/14 µs in MFM later. These times double when CLK = 1 MHz.

2) T Service (worst case); FM = 23.5 µs; MFM = 11.5 µs.

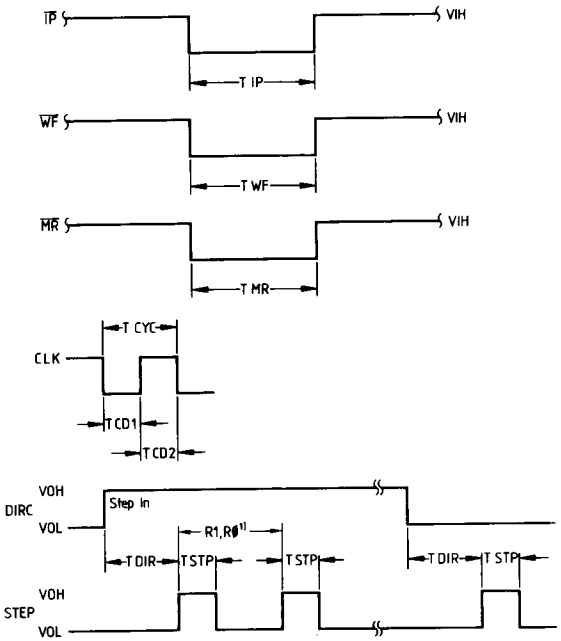
3) Time doubles when CLK = 1 MHz.

**Miscellaneous Timings**

| Symbol | Parameter | Limit Values | | | Unit | Test Condition | |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| TCD 1 | Clock Duty (low) | 230 | 250 | 20000 | ns | – | |
| TCD 2 | Clock Duty (high) | 230 | 250 | 20000 | ns | – | |
| TSTP [1] | Step Pulse Output | 2 or 4 | – | – | µs | – | |
| TDIR | DIRC Setup to Step | – | 12 | – | µs | ±CLK Error | |
| TMR | Master Reset Pulse Width | 50 | – | – | ns | – | |
| TIP | Index Pulse Width | 10 | – | – | µs | – | |
| RPW | Read Window Pulse Width | 120<br>240 | –<br>– | 700<br>1400 | ns<br>ns | MFM<br>FM ±15% | Input 0–5V |
| | Precomp Adjust | 100 | – | 300 | ns | MFM | |
| WPW | Write Data Pulse Width | 200 | 300 | 400 | ns | Precomp = 100 ns MFM | |
| | | 600 | 900 | 1200 | ns | Precomp = 300 ns MFM | |
| VCO | Free-Running Voltage-Controlled Oscillator | 6.0 | – | – | MHz | Cext = 0 | |
| | Adjustable by Ext. Capacitor on Pin 26 | – | 4.0 | – | MHz | Cext = 35 pF typ. | |
| | PUMP Up +25% | 5.0 | – | – | MHz | PU = 2.4 V, Cext = 35 pF | |
| | PUMP Down −25% | – | – | 3.0 | MHz | $\overline{PD}$ = 1.4 V, Cext = 35 pF | |
| | VCO frequency variation with VCC | – | 4.2 | – | MHz | VCC=5.25V | VCO=4MHz |
| | | – | 3.8 | – | MHz | VCC=4.75V | at VCC = 5 V |
| | VCO frequency variation over temperature | – | 4.15 | – | MHz | TA = 0°C | TA = 25% |
| | | – | 3.75 | – | MHz | TA = 70°C | |
| | Adjustable External Capacitor | 15 | 35 | 60 | pF | VCO = 4.0 MHz rated | |
| PLL | Lock-up Response | – | – | 384 | µs | $\overline{5}$/8 = 0 | Over specified |
| | | – | – | 192 | µs | $\overline{5}$/8 = 1 | capture range |
| | Capture Range | 0.9 | – | 1.1 | *RCLK | – | |
| RCLK | Derived Read Clock = VCO: 8, 16, 32 | – | 500 | – | kHz | $\overline{DDEN}$ = 0<br>$\overline{5}$/8 = 1 | VCO = 4.0 MHz |
| | | – | 250 | – | kHz | $\overline{DDEN}$ = 0<br>$\overline{5}$/8 = 0 | |
| | | – | 250 | – | kHz | $\overline{DDEN}$ = 1<br>$\overline{5}$/8 = 1 | |
| | | – | 125 | – | kHz | $\overline{DDEN}$ = 1<br>$\overline{5}$/8 = 0 | |
| PU/ DON | PU/$\overline{PD}$ Time On (Pulse Width) | – | – | 250 | ns | MFM | |
| | | – | – | 500 | ns | FM | |

[1] See stepping rates on page 51.

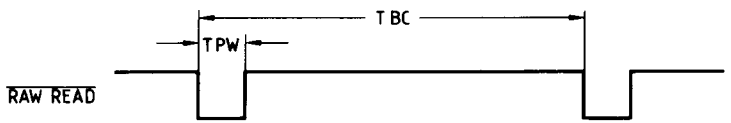
**Miscellaneous Timings**



**Read Data Timing**

| Symbol | Parameter | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TPW | $\overline{\text{RAW READ}}$ Pulse Width | 100 | 200 | – | ns | – |
| TBC | $\overline{\text{RAW READ}}$ Cycle Time | 1500 | 2000 | – | ns | – |

**Read Data Timing**

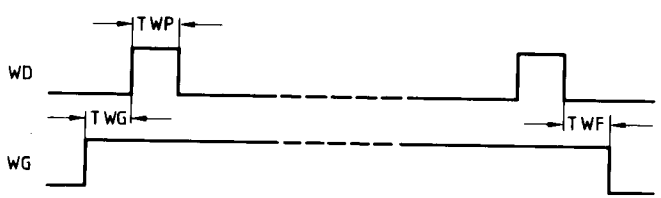



**Write Data Timing**

| Symbol | Parameter | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TWP | Write Data Pulse Width | 400 | 500 | 600 | ns | FM |
| | | 200 | 250 | 300 | ns | MFM |
| TWG | Write Gate to Write Data | – | 2 | – | µs | FM |
| | | – | 1 | – | µs | MFM |
| TWF | Write Gate from WD | – | 2 | – | µs | FM |
| | | – | 1 | – | µs | MFM |

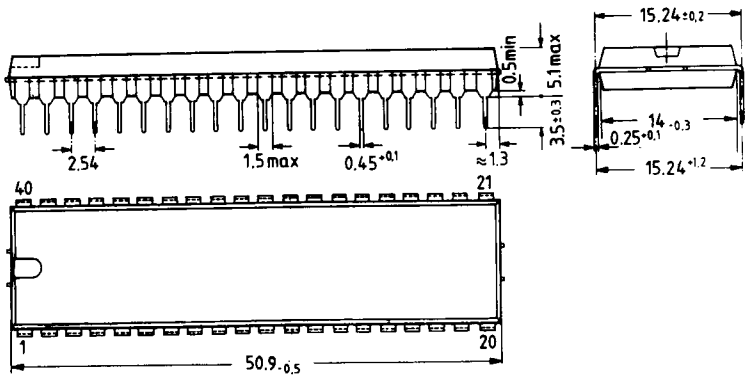
All times double when CLK = 1 MHz; no Write precompensation.

**Write Data Timing**



## Package Outline

**Plastic Package, P-DIP, 40 pins**




Dimensions in mm

## Ordering Information

| Type | Ordering code | Function |
|---|---|---|
| SAB 2793B-P | Q67120-Y82 | Floppy disk controller;<br>true data bus, single-sided operation |
| SAB 2797B-P | Q67120-Y84 | Floppy disk controller;<br>true data bus, double-sided operation |