# CH32V20x_30x Datasheet

*FOR CH32V203/303/305/307/208xx V0.9*

## Overview

The CH32Vx series of industrial-grade general-purpose microcontrollers based on 32-bit RISC-V architecture have formed diversified product models through the combination of different cores, peripherals and storage resources. All CH32Vx series are equipped with hardware stack area and fast interrupt entry, which greatly improves the interrupt response speed on the basis of standard RISC-V. CH32V208x is integrated with V4C core, adding memory protection function, and reducing the hardware division cycle at the same time. CH32V303/305/307 is integrated with V4F core, adding single-precision floating-point instruction set, expanding hardware stack area, and having higher computing performance. Product resources: the clock speed can reach 144MHz, independent GPIO voltage (separate from the system power supply). It has up to 8 groups of extended Serial Interface U(S)ART, 4 groups of motor timers, and it supports 1 group of 32-bit general-purpose timer. The CH32Vx contains USB2.0 high-speed interface (480Mbps) and built-in PHY transceiver. Its Ethernet MAC upgrades to Gigabit and is integrated with 10M-PHY module. It also supports Bluetooth BLE5.1 and so on.

## Features

- **Core：**
  - 32-bit RISC-V core, support multiple instruction set
  - Fast programmable interrupt controller + hardware interrupt stack
  - Branch prediction, conflict handling
  - Single cycle multiplication, hardware division, hardware FPU
  - Up to 144MHz clock speed
- **Memory：**
  - 64KB SRAM
  - 256KB user application CodeFlash
  - 28KB BootLoader
  - 128B non-volatile system configuration memory
  - 128B user-defined memory
- **Power management and low-power mode：**
  - System power supply VDD: 2.5V or 3.3V
  - Independent power supply for GPIO unit VIO: 2.5V or 3.3V
  - Low-power mode: sleep, stop, standby
  - VBAT independently powers RTC and backup register
- **Clock & Reset**
  - Built-in factory-calibrated 8MHz RC oscillator
  - Built-in 40KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 144MHz
  - External support 3～25MHz high-speed oscillator
  - External support 32.768KHz low-speed oscillator
  - Power on/off reset, programmable voltage monitor
- **Real-time clock (RTC):** 32-bit independent RTC timer
- **2 groups of 18-channels general purpose DMA controllers**
  - 18 channels, support ring buffer
  - Support TIMx/ADC/DAC/USART/I2C/SPI/I2S/SDIO
- **4 groups of OPAs and comparators:** connected with ADC and TIMx
- **12-bit DAC × 2**
- **12-bit ADC × 2**
  - Analog input range: $V_{SSA}$～$V_{DDA}$
  - 16 external signals + 2 internal signals
  - On-chip temperature sensor
  - Dual conversion mode
- **16-channels TouchKey detection**
- **Timers**
  - Four 16-bit advanced timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - Three 16-bit general-purpose timers input capture/output comparison/PWM/pulse counting/incremental encoder input
  - One 32-bit or 16-bit general-purpose timer

- Two basic timers
- Two watchdog timers (independent and window type)
- SysTick: 64-bit counter

- **Communication interfaces:**
- 8 × USART interfaces (including 5 UARTs)
- 2× I²C interfaces (support SMBus/PMBus)
- 3× SPI interfaces (SPI2, SPI3 for I²S2, I²S3)
- USB2.0 full-speed device interface (full-speed and low-speed)
- USB2.0 full-speed host/device interface
- USB2.0 full-speed OTG interface
- USB2.0 high-speed host/device interface (built-in PHY)
- 2 groups of CAN interfaces (2.0B active)
- SDIO host interface (MMC, SD/SDIO, CE-ATA)
- FSMC memory interface
- Digital image interface DVP
- Gigabit Ethernet controller MAC, 10M PHY transceiver
- Bluetooth Low Energy (BLE) 5.1

- **Fast GPIO port**
- 80 GPIO ports, with 16 external interrupts

- **Security features:** CRC unit, 96-bit unique chip ID
- **Debug mode:** serial 2-wire debug interface
- **Package:** LQFP or QFN

# Chapter 1 Series Product Description

CH32Vx series products are industrial-grade general-purpose enhanced MCUs based on 32-bit RISC-V instruction set and architecture. Its products are divided by function resources into categories such as general purpose, connectivity, and wireless. They are extended to each other in terms of package types, peripheral resources and quantities, pin numbers, and device characteristics, but they are compatible with each other in software, functions, and hardware pin configurations. The product iterations and rapid applications provide freedom and convenience for users in product development.

For the features of this series of products, please refer to the data manual "CH32V20x 30xDS0".

For the peripheral function description, usage and register configuration, please refer to "CH32xRM".

The data manuals and reference manuals can be downloaded on the official website of WCH: http://www.wch.cn/

Information about the RISC-V instruction set architecture can be downloaded from: https://riscv.org/

This manual is the data manual of CH32V20x and CH32V30x series.

Table 1-1 Series overview

| Small-and-medium-capacity general type(V203) | | Large-capacity general type(V303) | | Connection type(V305) | Interconnection type(V307) | Wireless type(V208) |
|---|---|---|---|---|---|---|
| V4B Core | | V4F Core | | | | V4C Core |
| 32K Flash | 64K Flash | 128K Flash | 256K Flash | 128K Flash | 256K Flash | 128K Flash |
| 10K SRAM | 20K SRAM | 32K SRAM | 64K SRAM | 32K SRAM | 64K SRAM | 64K SRAM |
| 2*ADC(TKey)<br>ADTM<br>2*GPTM<br>2*USART<br>SPI<br>I2C<br>USBD<br>USBHD<br>RTC<br>2*WDG<br>2*OPA | 2*ADC(TKey)<br>ADTM<br>3*GPTM<br>4*U(S)ART<br>2*SPI<br>2*I2C<br>USBD<br>USBHD<br>RTC<br>2*WDG<br>2*OPA | 2*ADC(TKey)<br>2*DAC<br>ADTM<br>3*GPTM<br>3*USART<br>2*SPI<br>2*I2C<br>USBHD<br>CAN<br>RTC<br>2*WDG<br>4*OPA | 2*ADC(TKey)<br>2*DAC<br>4*ADTM<br>4*GPTM<br>2*BCTM<br>8*U(S)ART<br>3*SPI(2*I2S)<br>2*I2C<br>USBHD<br>CAN<br>RTC<br>2*WDG<br>4*OPA<br>TRNG<br>SDIO<br>FSMC | 2*ADC(TKey)<br>2*DAC<br>4*ADTM<br>4*GPTM<br>2*BCTM<br>5*U(S)ART<br>3*SPI(2*I2S)<br>2*I2C<br>USB-OTG<br>USBHS(+PHY)<br>2*CAN<br>RTC<br>2*WDG<br>4*OPA<br>TRNG<br>SDIO | 2*ADC(TKey)<br>2*DAC<br>4*ADTM<br>4*GPTM<br>2*BCTM<br>8*U(S)ART<br>3*SPI(2*I2S)<br>2*I2C<br>USB-OTG<br>USBHS(+PHY)<br>2*CAN<br>RTC<br>2*WDG<br>4*OPA<br>TRNG<br>SDIO<br>FSMC<br>DVP<br>ETH-1000MAC<br>10M-PHY | ADC(TKey)<br>ADTM<br>3*GPTM<br>GPTM(32)<br>4*U(S)ART<br>2*SPI<br>2*I2C<br>USBD<br>USBHD<br>CAN<br>RTC<br>2*WDG<br>2*OPA<br>ETH-10M(+PHY)<br>BLE5.1 |

*Note: The number or functions of some peripherals of the same type of product may be restricted by the package. Please confirm the package when selecting.*

Abbreviation

ADTM：Advanced Timer
GPTM：General Purpose Timer
GPTM(32)：32-bit General-purpose Timer
BCTM：Basic Timer
TKey：Touch Key
OPA：Operational Amplifier, Comparator
TRNG：True Random Number Generator
USBD：Universal Serial Bus Device
USBHD：Universal Serial Bus Hold Device
USBHS：Universal Serial Bus Host Device

Table 1-2 Overview of Cores

| Feature / Core Version | Instruction Set | Hardware Stack Level | Interrupt Nesting Level | Number of Fast Interrupt Channels | Integer Division Period | Vector table mode | Extended instruction | Memory protection |
|---|---|---|---|---|---|---|---|---|
| V4B | IMAC | 2 | 2 | 4 | 9 | Address or instruction | Support | No |
| V4C | IMAC | 2 | 2 | 4 | 5 | Address or instruction | Support | Standard |
| V4F | IMAFC | 3 | 8 | 4 | 5 | Address or instruction | Support | Standard |

# Chapter 2 Specification

The CH32Vx series is a 32-bit RISC MCU based on the RISC-V instruction set architecture (ISA), with a maximum clock speed of 144MHz, and built-in high-speed memory. It has multiple buses working synchronously, and provides a wealth of peripheral functions and enhanced I/O ports. This series of products has built-in two 12-bit ADC modules, two 12-bit DAC modules, multiple timers, multi-channel capacitance touch key detection (TKey) and other functions. It also contains standard and dedicated communication interfaces: I²C, I²S, SPI, USART, SDIO, CAN controller, USB2.0 full-speed host/device controller, USB2.0 high-speed host/device controller (built-in PHY transceiver), digital image interface, Gigabit Ethernet controller, Bluetooth Low Energy (BLE), etc. .

The rated working voltage of the product is 2.5V or 3.3V, and the working temperature range is -40℃～85℃ in industrial grade. It supports a variety of power-saving operating modes to meet the product's low-power application requirements.

Various models in the series are different in terms of resource allocation, number of peripherals, peripheral functions, etc., and can be selected as needed.

Available in LQFP48/QFN48/LQFP64M/LQFP100 packages. CH32Vx series can be widely used in motor drive and application control, medical and handheld devices, PC game peripherals, GPS platforms, programmable controllers, inverters, printers, scanners, alarm systems, video intercoms, heating, ventilation and air conditioning systems, etc.

## 2.1 Model comparison

Table 2-1 CH32V general product resource allocation

| Part No. / Differences | | CH32V203x | | | | CH32V303x | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | C6T6 | K8T6 | C8T6 | C8U6 | CBT6 | RBT6 | RCT6 | VCT6 |
| Pin number | | 48 | 32 | 48 | 48 | 48 | 64 | 64 | 100 |
| Flash (bytes) | | 32K | 64K | 64K | 64K | 128K | 128K | 256K | 256K |
| SRAM (bytes) | | 10K | 20K | 20K | 20K | 32K | 32K | 64K | 64K |
| Number of GPIO ports | | 37 | 27 | 37 | 37 | 37 | 51 | 51 | 80 |
| GPIO power supply | | Shared with $V_{DD}$ | | | | | Independent power supply $V_{IO}$ | | |
| Timer | Advanced (16 bits) | 1 | 1 | 1 | 1 | 1 | 1 | 4 | 4 |
| | General (16 bits) | 2 | 3 | 3 | 3 | 3 | 3 | 4 | 4 |
| | Basic (16 bits) | - | | | | | | 2 | 2 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SysTick (24 bits) | support | | | | | | | |
| RTC | | support | | | | | | | |
| ADC/TKey (Number of units/channels) | | 2/10 | 2/10 | 2/10 | 2/10 | 2/10 | 2/16 | 2/16 | 2/16 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DAC（Unit） | | - | | | | 2 | 2 | 2 | 2 |
| OPA, comparator | | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 4 |
| Random number generator | | - | | | | - | | 1 | 1 |
| Communication Interface | U(S)ART | 2 | 3 | 3 | 3 | 3 | 3 | 8 | 8 |
| | SPI | 1 | 2 | 2 | 2 | 2 | 2 | 3 | 3 |
| | I2S | - | | | | - | | 2 | 2 |
| | I2C | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | CAN | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | SDIO | - | | | | - | | 1 | 1 |
| | USB(FS) | 2 | 1(USBD) | 2(USBD+USBHD) | | 1(USBHD) | | | |
| | FSMC | - | | | | - | | | 1 |
| CPU clock speed | | Max：144MHz | | | | | | | |
| Rated voltage | | 2.5V or 3.3V | | | | | | | |
| Operating temperature | | Industrial grade: -40℃～85℃ | | | | | | | |
| Package | | LQFP48 | LQFP32 | LQFP48 | QFN48 | LQFP48 | LQFP64M | | LQFP100 |

Table 2-2 CH32V connection/interconnection/wireless product resource allocation

| Part No. / Differences | | CH32V305 | CH32V307 | | CH32V208 | | | |
|---|---|---|---|---|---|---|---|---|
| | | RBT6 | RCT6 | VCT6 | GBU6 | CBU6 | RBT6 | WBU6 |
| Pin number | | 64 | 64 | 100 | 28 | 48 | 64 | 68 |
| Flash (bytes) | | 128K | 256K | 256K | 128K | 128K | 128K | 128K |
| SRAM (bytes) | | 32K | 64K | 64K | 64K | 64K | 64K | 64K |
| Number of GPIO ports | | 51 | 51 | 80 | 21 | 37 | 49 | 53 |
| GPIO power supply | | Independent power supply $V_{IO}$ | | | Shared with $V_{DD}$ | | | Independent $V_{IO}$ |
| Timer Timer | Advanced (16 bits) | 4 | 4 | 4 | 1 | 1 | 1 | 1 |
| | General (16 bits) | 4 | 4 | 4 | 3 | 3 | 3 | 3 |
| | Basic (16 bits) | - | | | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | - | | | |
| | SysTick (24 bits) | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Advanced (16 bits) | support | | | | | | |
| ADC/TKey (Number of units/channels) | | support | | | | | | |
| DAC（Unit） | | 2/16 | 2/16 | 2/16 | 1/8 | 1/16 | 1/16 | 1/16 |
| OPA, comparator | | 2 | 2 | 2 | - | | | |
| Random number generator | | 4 | 4 | 4 | 1 | 2 | 2 | 2 |
| ADC/TKey (Number of units/channels) | | 1 | 1 | 1 | - | | | |
| Communication | U(S)ART | 5 | 8 | 8 | 2 | 4 | 4 | 4 |

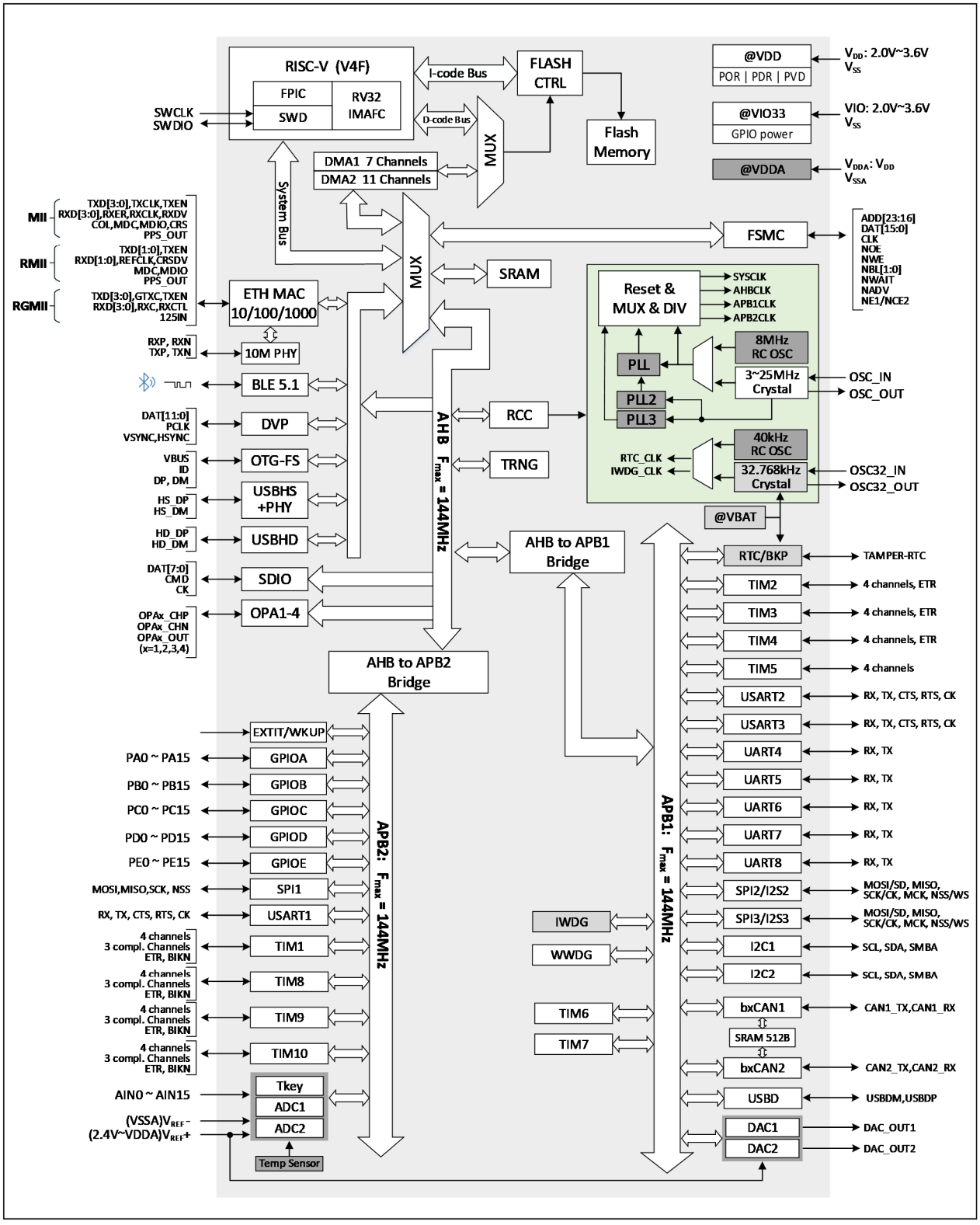
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Interface | SPI | 3 | 3 | 3 | 1 | 2 | 2 | 2 |
| | I2S | 2 | 2 | 2 | - | | | |
| | I2C | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| | CAN | 2 | 2 | 2 | 1 | 1 | 1 | 1 |
| | SDIO | 1 | 1 | 1 | - | | | |
| | DVP | - | - | 1 | - | | | |
| | USB(FS) | OTG | | | 2 (USBD+USBHD) | | | |
| | USB(HS) | 1 | | | - | | | |
| | Ethernet | - | 1G MAC+10M PHY | | 10M | | | |
| | FSMC | - | - | 1 | - | | | |
| | BLE 5.1 | - | | | support | | | |
| CPU clock speed | | Max：144MHz | | | | | | |
| Rated voltage | | 2.5V or 3.3V | | | | | | |
| Operating temperature | | Industrial grade: -40℃～85℃ | | | | | | |
| Package | | LQFP64M | LQFP64M | LQFP100 | QFN28 | QFN48 | LQFP64M | QFN68 |

*Note: The 256K FLASH+64K SRAM product supports one of several combinations of (192K FLASH+128K SRAM), (224K FLASH+96K SRAM), (256K FLASH+64K SRAM), (288K FLASH+32K SRAM).*

## 2.2 System Architecture

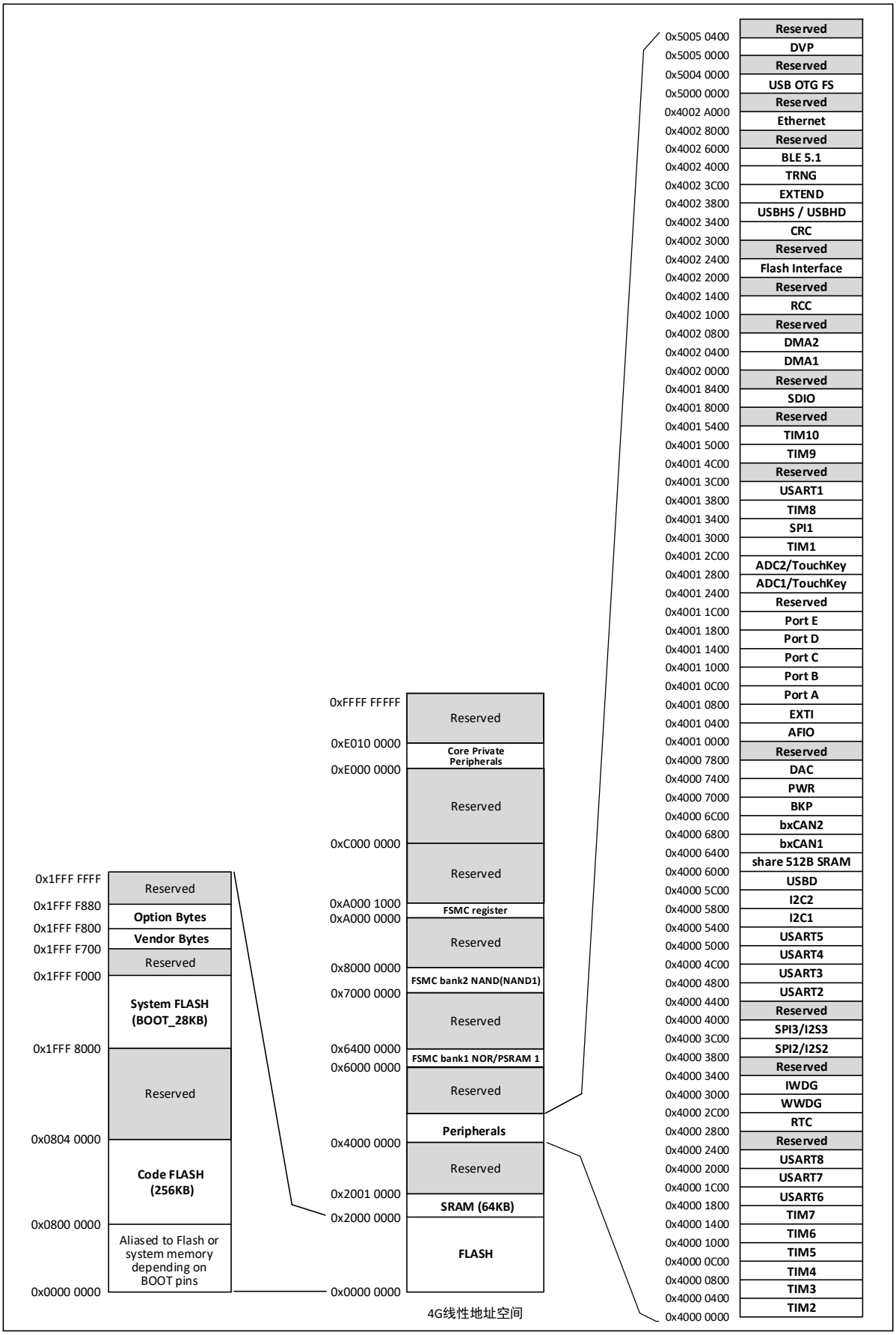
The microcontroller is designed based on the RISC-V instruction set architecture (ISA) in which the core, arbitration unit, DMA module, SRAM storage and other parts are interacted through multiple sets of buses. A general-purpose DMA controller is integrated in the chip to reduce the burden on the CPU and improve access efficiency. The application of a multi-level clock management mechanism reduces the operating power consumption of peripherals. At the same time, it has a data protection mechanism and measures such as automatic clock switching protection to increase system stability. The following figure is a block diagram of the overall internal structure of the series of products.

Figure 2-1 System block diagram



## 2.3 Memory Map

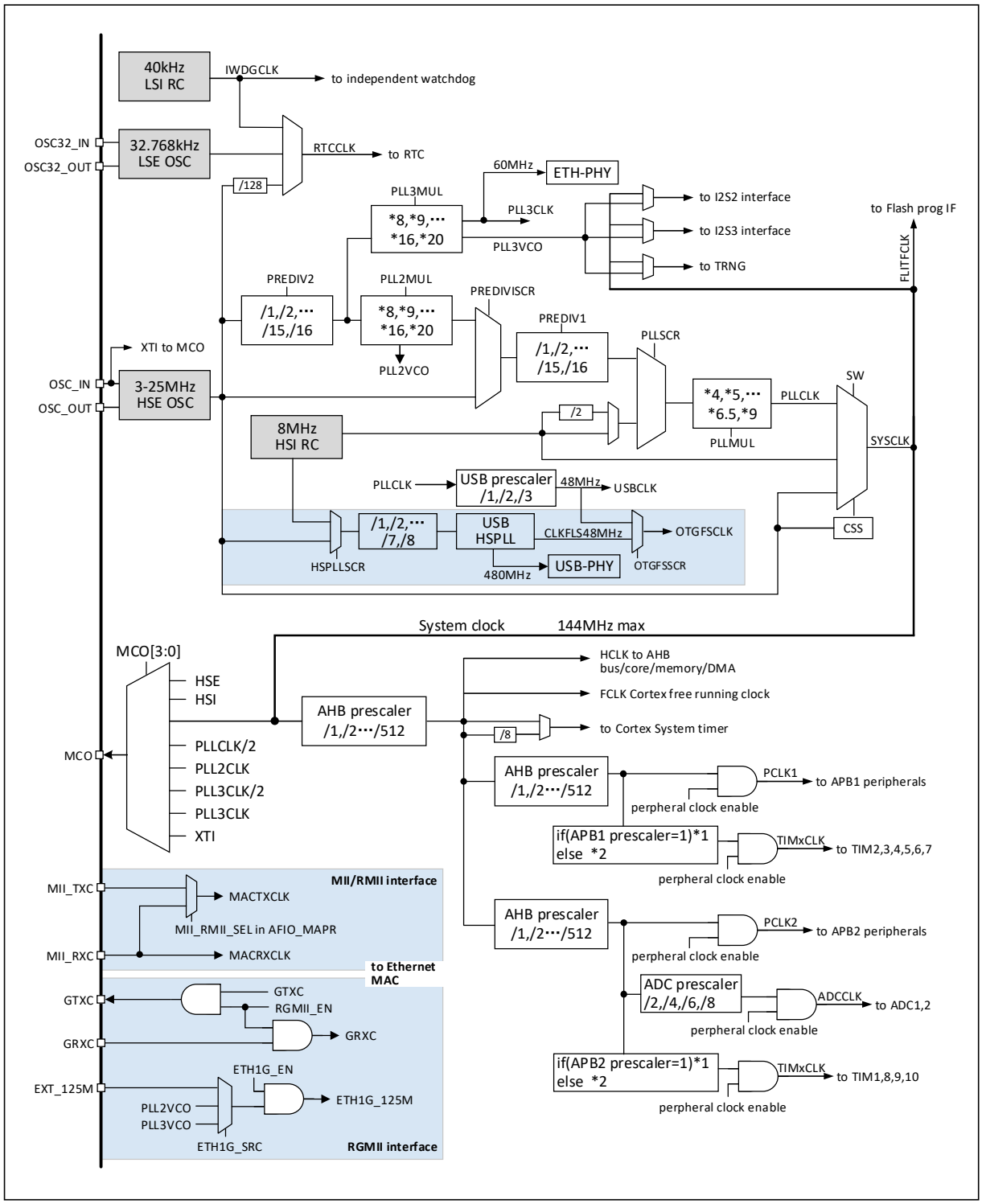
Figure 2-2 Memory address mapping



## 2.4 Clock tree

Four groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by the PLL and output as the system clock (SYSCLK). The system clock is then provided by each prescaler to provide the AHB domain, APB1 domain, APB2 domain peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

Figure 2-3 Clock tree block diagram



*Note: When using USB, the CPU clock speed must be 48MHz or 96MHz or 144MHz. When the system wakes up from sleep mode, the system will automatically switch to HSI as the main frequency.*

## 2.5 Function overview

### 2.5.1 RISC-V4B/4C/4F processor

The product is designed based on the RSIC-V organization specification for cores V4B, V4C, V4F. V4B and V4C support the RISC-V instruction set IMAC subset, and V4F supports the RISC-V instruction set IMAFC subset, which increases the single-precision floating-point budget. The processor internals is managed in a modular way and contains fast programmable interrupt controller (FPIC), memory protection, branch prediction mode, extended instruction support and other units. The external multiple sets of buses are connected with the external unit modules to implement the interaction between the external function modules and the core. Externally, the processor has multiple sets of buses connected to peripherals for interaction.

The processor can be flexibly applied in different scenarios, such as small-area low-power embedded scenarios, high-performance application operating system scenarios, etc., due to its minimal instruction set, multiple working modes, and modular customization extensions.

- Support machine and user privilege mode
- Fast Programmable Interrupt Controller (FPIC)
- Multi-level hardware interrupt stack
- Serial 2-wire debugging interface
- Standard memory protection design
- Static or dynamic branch prediction, efficient jump, conflict detection
- Custom extended instructions

### 2.5.2 On-chip memory and boot mode

Built-in 32K or 64K bytes SRAM area, used to store data, data will be lost after power failure.

Built-in 128K or 256K bytes program Flash memory (Code FLASH), used for user's application and constant data storage.

Among them, 256K FLASH+64K SRAM products supports one of several combinations (192K FLASH+128K SRAM), (224K FLASH+96K SRAM),(256K FLASH+64K SRAM) and (288K FLASH+32K SRAM).

Built-in 28K byte system memory (System FLASH), used for system boot program storage (manufacturer curing boot loader).128 bytes are used for manufacturer configuration word storage, and 128 bytes are used for user selection word storage.

At startup, one of three boot modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from program flash
- Boot from system memory
- Boot from internal SRAM

The bootloader is stored in the system memory, and the contents of the program Flash can be reprogrammed through the USART1 and USB interface.

### 2.5.3 Power supply scheme

- $V_{DD}$ = 2.3～3.6V：Power supply for some I/O pins and internal voltage regulator.
- $V_{IO}$ = 2.3～3.6V：It supplies power to most of the I/O pins and the Ethernet module, which

determines the pin output high voltage amplitude. Normal work during operation, the VIO voltage cannot be higher than the VDD voltage.

- $V_{DDA}$ = 2.3～3.6V：It supplies power to the analog part of the high-frequency RC oscillator, ADC, temperature sensor, DAC and PLL. The VDDA voltage must be the same as the VIO voltage (If VDD is powered down and VIO is live, Then VDDA must be live and consistent with VIO). When using ADC ,VDDA must not be less than 2.4V。
- $V_{BAT}$ = 1.8～3.6V：When VDD is turned off, (through the internal power switch) independently powers the RTC, external low-frequency oscillator and backup registers. (Pay attention to VBAT power supply)

### 2.5.4 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in working condition to ensure that the system is in supply. It works when the power exceeds 2.3V; when $V_{DD}$ is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without using an external reset circuit.

In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of $V_{DD}$ power supply with the set threshold VPVD

Turn on the corresponding edge interrupt of PVD, and you can receive interrupt notification when $V_{DD}$ drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.5.5 Voltage regulator

After reset, the regulator is automatically turned on, and there are three operation modes according to the application mode.

- Open mode: normal operation, providing stable core power.
- Low-power mode: When the CPU enters the stop mode, the regulator can be selected to run with low power consumption.
- Shutdown mode: When the CPU enters the standby mode, it automatically switches the regulator to this mode, the voltage regulator output is in a high-impedance state, and the core power.

The voltage regulator is always in the on mode after reset, and is turned off in the off mode in the standby mode. At this time, it is a high-impedance output.

### 2.5.6 Low-power mode

The system supports three low-power modes, which can be selected for low power consumption, short start-up time and multiple wake-up events to achieve the best balance.

- Sleep mode

In sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in a working state. This mode is the most shallow Low power mode, but it is the fastest mode to wake-up the system.
Exit condition: any interrupt or wake-up event.

- Stop mode

In this mode, the FLASH enters low power mode, and the PLL, HSI RC oscillator and HSE crystal oscillator are turned off. In the case of keeping the contents of SRAM and registers not lost, the stop mode can achieve the lowest power consumption.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST,

IWDG reset, among which EXTI signal includes one of 16 external I/O ports, PVD output, RTC alarm clock, Ethernet wake-up signal or USB wake-up signal.

- Standby mode

In this mode, the main LDO of the system is turned off, the low-power LDO supplies power to the wake-up circuit, all other digital circuits are powered off, and the FLASH is powered off. The system wakes up from standby mode will generate a reset, and SBF (PWR_CSR) will be set at the same time. After waking up, check the SBF status to know the low-power mode before waking up. SBF is cleared by the CSBF (PWR_CR) bit. In the standby mode, the contents of 32KB of SRAM can be kept (depending on the planning and configuration before going to bed), and the contents of the backup registers are kept.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where EXTI signal includes one of 16 external I/O ports, RTC alarm clock, Ethernet Wake-up signal, USB.

### 2.5.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, a means of detecting flash errors is provided. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

### 2.5.8 Fast Programmable Interrupt Controller (FPIC)

The product has a built-in Fast Programmable Interrupt Controller (FPIC), which supports up to 255 interrupt vectors, and provides flexible interrupt management functions with minimal interrupt latency. The current product manages 8 core private interrupts and 88 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in user and machine privileged modes.

- 88+3 individual maskable interrupts
- a non-maskable interrupt NMI
- Support hardware interrupt stack without instruction overhead
- 4 programmable fast interrupt channels, custom interrupt vector address
- Support vector table mode of address or instruction module
- Interrupt nesting level 2 or 8
- Support interrupt tail link

### 2.5.9 External interrupt/event controller (EXTI)

The external interrupt/event controller contains a total of 19 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is smaller than the clock period of the internal APB2. Up to 80 general-purpose I/O ports can be connected to 16 external interrupt lines.

### 2.5.10 Genral DMAController

The system has built-in 2 groups of general-purpose DMA controllers, manages 18 channels in total, and flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source

address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general/advanced/basic timers TIMx, ADC, DAC, I²S, USART, I²C, SPI, SDIO.

*Note: DMA1, DMA2 and CPU access the system SRAM after arbitration by the arbiter.*

### 2.5.11 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 3～25MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; In power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of AHB. The high-speed APB (APB2) and low-speed APB (APB1) regions provide peripheral clocks with a maximum frequency of 144MHz. Refer to the clock tree block diagram in Figure 2-3. The clock source of the I²S unit is another dedicated PLL (PLL3), so that the I²S master clock can generate all standard sampling frequencies between 8kHz and 192kHz.

### 2.5.12 RTC (Real Time Clock) and backup registers

The RTC and the backup register are in the backup power supply area inside the system. When $V_{DD}$ is valid, it is powered by $V_{DD}$, and when $V_{DD}$ is invalid, the internal power is automatically switched to the $V_{BAT}$ pin.

The RTC real-time clock is a set of 32-bit programmable counters, and the time base supports 20-bit prescaler for measurement in a longer period of time. The clock reference source is a high-speed external clock divided by 128 (HSE/128), external crystal low-frequency oscillator (LSE) or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the RTC setting and time can remain unchanged after the system resets or wakes up from standby mode.

The backup register contains 42 16-bit registers, which can be used to store 84 bytes of user application data. This data can continue to be maintained after wake-up from standby, or system reset or power reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

### 2.5.13 ADC (analog/digital converter) and touch key capacitance detection (TKey)

The product is embedded with two 12-bit analog/digital converters (ADC), sharing up to 16 external channels and 2 internal channels for sampling. The programmable channel sampling time can realize single, continuous, scanning or discontinuous conversion. And supports dual ADC conversion mode. The analog watchdog function is provided to allow very precise monitoring of one or more selected channels for monitoring the signal voltage of the channel. It supports external event trigger conversion, the trigger source includes the internal signal and external pin of the on-chip timer; it also supports the use of DMA operations.

ADC internal channel sampling includes one channel of built-in temperature sensor sampling and one channel of internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the IN16 input channel, which is used to convert the output of the sensor to a digital value.

The capacitance touch key detection unit provides up to 16 detection channels, multiplexing the external channels of the ADC module. The detection result is converted and output by the ADC module, and the state of the touch key is recognized by the user software.

### 2.5.14 DAC (digital/analog converter)

The product is embedded with two 12-bit voltage output digital/analog converters (DAC), converts 2 digital signals into 2 analog voltage signals and outputs them, supports dual DAC channel independent or synchronous conversion, supports external event trigger conversion, trigger sources include Internal signals and external pins of the on-chip timer (EXTI line 9). Triangular wave and noise generation can be realized. It supports the use of DMA operations.

### 2.5.15 Timer and watchdog

The timers in the system include advanced timers, general timers, basic timers, watchdog timers, and system time base timers. The number of timers included in different products in the series is different, please refer to Table 2-2 for details.

Table 2-2 Timer comparison

| Timer | | Resolution | Count Type | Time Base | DMA | Function |
|---|---|---|---|---|---|---|
| Advanced timer | TIM1 | 16 bits | Upward<br>Down<br>Up/down | APB2 time domain 16-bit divider | Support | PWM complementary output, single pulse output<br>Input capture<br>Output comparison<br>Timer counting |
| | TIM8 | | | | | |
| | TIM9 | | | | | |
| | TIM10 | | | | | |
| General Timer | TIM2 | 16 bits | Upward<br>Down<br>Up/down | APB1 time domain 16-bit divider | Support | Input capture<br>Output comparison<br>Timer counting |
| | TIM3 | | | | | |
| | TIM4 | | | | | |
| | TIM5[1] | 16/32 bits | | | | |
| Basic Timer | TIM6 | 16 bits | Up | APB1 time domain 16-bit divider | Support | Timer counting |
| | TIM7 | | | | | |
| Window watchdog | | 7 bits | Down | APB1 time domain 4 frequency divisions | Not support | Timing<br>Reset the system (normal work) |
| Independent watchdog | | 12 bits | Down | APB1 time domain 7 frequency divisions | Not support | Timing<br>Reset the system (normal work) |
| SysTick Timer | | 64 bits | Up/down | SYSCLK or SYSCLK/8 | Not support | Timing |

*Note 1: TIM5 is a 32-bit general-purpose timer in CH32V208 (wireless type).*

- Advanced control timer

The advanced control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead zone insertion, allowing the

timer to be updated after a specified number of counter cycles to repeat Counting cycle, braking function, etc. Many functions of the advanced control timer are the same as the general timer, and the internal structure is also the same. Therefore, the advanced control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link functions.

- General timer

The general timer is a 16-bit or 32-bit auto-loading up/down counter with a programmable 16-bit prescaler and 4 independent channels. Each channel supports input capture, output comparison, and PWM generation and single pulse mode output. It can also work with advanced control timers through the timer link function to provide synchronization or event link functions. In debug mode, the counter can be frozen while the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

- Basic timer

The basic timer is a 16-bit auto-load counter that supports a 16-bit programmable prescaler. Digital-to-analog conversion (DAC) can provide a clock and trigger the synchronization circuit of the DAC. The basic timers are independent of each other and do not share any resources with each other.

- Independent watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent 40KHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in stop and standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In debug mode, the counter can be frozen.

- Window watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in the debug mode, the counter can be frozen.

- SysTick timer

This is a 64-bit optional increment or decrement counter that comes with the core controller. It is used to generate SYSTICK anomalies (exception number: 15). It can be dedicated to the real-time operating system (RTOS) to provide a "heartbeat" tick for the system, or it can be used as a standard 64-bit counter. It has an automatic reload function and a programmable clock source.

### 2.5.16 Communication Interface

#### 2.5.16.1Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 3 groups of Universal Synchronous/Asynchronous Receiver Transmitters (USART1, USART2, USART3), and 5 groups of Universal Asynchronous Receiver Transmitters (UART4, UART5, UART6, UART7, UART8). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a

fractional baud rate generator system and supports DMA operation continuous communication.

#### 2.5.16.2 Serial Peripheral Interface (SPI)

Up to 3 groups of serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, reliable communication hardware CRC generation/check, and supports DMA operation continuous communication.

#### 2.5.16.3 I²S (audio) port

The highest two groups of standard I²S interfaces (multiplexed with SPI2 and SPI3) work in master or slave mode. The software can be configured as a 16/32-bit data packet transmission frame, supports audio sampling frequencies from 8kHz to 192kHz, and supports 4 audio standards. In master mode, its master clock can be output to an external DAC or CODEC (decoder) at a fixed 256 times audio sampling frequency, and supports DMA.

#### 2.5.16.4 I²C Bus

Up to 2 I²C bus interfaces can work in multi-master mode or slave mode, perform all I²C Bus specific timing, protocol, arbitration, etc. It supports both standard and fast speed, and is compatible with SMBus2.0.

The I²C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0 / PMBus bus.

#### 2.5.16.5 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbits/s, and it supports time-triggered communication. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and 2 3-level deep receiving FIFOs.

Products with 2 CAN controllers share 28 configurable filters and 512 bytes of SRAM memory resources.

With 1 set of CAN controller products, there are only 14 configurable filters, and share a dedicated 512-byte SRAM memory with the USBD module for data transmission and reception. When USBD and CAN are used at the same time, in order to prevent access to SRAM conflicts, USBD can only use the lower 384 bytes.

#### 2.5.16.6 Universal Serial Bus Device (USBD)

The product is embedded with a USB2.0 full-speed controller, which complies with the USB2.0 Fullspeed standard. USBD provides 16 configurable USB device endpoints, supports low-speed devices and full-speed devices, supports control/batch/synchronization/interrupt transmission, double buffer mechanism, USB suspend/resume operations, and has standby/wake-up functions. The USB dedicated 48MHz clock is directly generated by the internal main PLL frequency division.

#### 2.5.16.7 Universal Serial Bus USB2.0 Full Speed Host/Device Controller (USBHD)

The USB2.0 full-speed host controller and device controller (USBHD) follow the USB2.0 Fullspeed standard. It provides 16 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronization/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up functions. The 48MHz clock dedicated to the USBHD module is

directly generated by the internal main PLL frequency division (the PLL must be 144MHz or 96MHz or 48MHz).

#### 2.5.16.8 Universal Serial Bus USB2.0 Full Speed OTG (OTG-FS)

OTG_FS is a dual-role USB controller that supports the functions of the host side and the device side, and is compatible with the On-The-Go Supplement to the USB2.0 specification. At the same time, the controller can also be configured as a controller that only supports host-side or device-side functions, and is compatible with the USB2.0 full-speed specification. The controller uses a 48MHz clock derived from the PLL frequency division. The main features include:

- Support (the physical layer of the OTG_FS controller) USB On-The-Go Supplement, defined as an optional item OTG protocol in the Revision1.3 specification
- Configure USB full-speed host, USB full-speed/low-speed device, USB dual-role device through software
- Provide power saving function
- Support control transmission, batch transmission, interrupt transmission, real-time/synchronous transmission
- Provide bus reset, suspend, wake up and resume functions

#### 2.5.16.9 Universal Serial Bus USB2.0 High Speed Host/Device Controller (USBHS)

The USB2.0 high-speed controller has the dual roles of a host controller and a device controller, and has an embedded USB-PHY transceiver unit. When used as a host controller, it can support low-speed, full-speed, and high-speed USB devices. When used as a device controller, it can be flexibly set to low-speed, full-speed or high-speed mode to adapt to various applications. The main features include:

- Support for USB 2.0, USB 1.1, USB 1.0 protocol specifications
- Support for control transmission, batch transmission, interrupt transmission, real-time/synchronous transmission
- bus reset, suspend, wake up and resume functions
- Support for high-speed HUB
- 8 groups of upper and lower transmission channels in device mode, and support the configuration of 16 endpoint numbers
- Except for device endpoint 0, all other endpoints support data packets up to 1024 bytes, and double buffering can be used

#### 2.5.16.10 Digital Visual Interface (DVP)

DVP (Digital Video Port) is used to connect the camera module to receive the image data stream. It provides 8/10/12bit parallel interface communication. It supports image data organized in original line and frame formats, such as YUV, RGB, etc., and also supports compressed image data streams such as JPEG format. When receiving, it mainly relies on VSYNC and HSYNC signal synchronization. It also supports image cropping.

#### 2.5.16.11 SDIO host controller

The SDIO host interface provides operation interfaces for multimedia cards (MMC), SD memory cards, SDIO cards, and CE-ATA devices. It supports 3 different data bus modes: 1-bit (default), 4-bit and 8-bit. In 8-bit mode, the interface can make the data transfer rate up to 48MHz. This interface is fully compatible with Multimedia Card System Specification 4.2 (forward compatible), SD I/O Card Specification 2.0, SD Memory Card Specification 2.0, and CE-ATA Digital Protocol Specification 1.1.

#### 2.5.16.12 Flexible Static Memory Controller (FSMC)

The FSMC interface mainly provides a synchronous or asynchronous memory interface, and supports devices such as SRAM, PSRAM, NOR, and NAND. The internal AHB transmission signal is converted into a suitable external communication protocol, allowing continuous access to 8/16/32-bit data. And the sampling delay time can be flexibly configured to meet the timing of different devices.

In addition, FSMC can also be used for most graphics LCD controller interfaces. It supports Intel 8080 and Motorola 6800 modes, making it easy to build a simple graphics application environment or a high-performance solution for dedicated acceleration controllers.

#### 2.5.16.13 Gigabit Ethernet Controller (MAC, +10M PHY)

The product provides a Gigabit Ethernet Media Access Controller (MAC) that meets the IEEE 802.3-2002 standard, which acts as the data link layer. Its Link supports up to 1Gbps, and provides MII/RMII/RGMII interfaces to connect to external PHY (Gigabit /100M/speed self-adaptive, built-in 10M PHY transceiver). The application is combined with TCP/IP protocol stack interface to realize the development of network products. The main features include:

- Complying with IEEE.802.3 standard
- RGMII, RMII, MII interface, connect external Ethernet PHY transceiver
- Support for full-duplex operation, support 10/100/1000Mbps data transmission rate
- The hardware automatically completes IPv4 and IPv6 packet integrity check, IP/ICMP/UDP/TCP packet check and computer frame length filling
- Multiple MAC address filtering modes
- SMI configuring and managing external PHY

### 2.5.17 General-purpose input and output (GPIO)

The system provides 5 groups of GPIO ports with a total of 80 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the IO configuration to avoid accidental writing to the I/O register.

Most of the IO pins in the system are provided by $V_{IO}$. Changing the $V_{IO}$ power supply will change the high value of the IO pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

### 2.5.18 True Random Number Generator (TRNG)

The product is integrated with a true random number generator, which provides a 32-bit true random number through the internal analog circuit.

### 2.5.19 Operational Amplifier/Comparator (OPA)

The product has built-in 4 groups of operational amplifiers/comparators, and the internal selection is linked to the ADC and TIMx peripherals. Its input and output can be selected by changing the configuration to select multiple channels. It supports to amplify the external analog small signal and send it to the ADC to realize the small signal ADC conversion. It can also complete the signal comparator function. The comparison result is output by GPIO or directly connected to the input channel of TIMx.

### 2.5.20 Serial 2-wire debug interface (SWD)

The core comes with a serial 2-wire debugging interface, including SWDIO and SWCLK pins. After the system is powered on or reset, the debug interface pin function is enabled by default.

# Chapter 3 Pin

## 3.1 General/connection/interconnection types

Figure 3-1 100-pin LQFP100

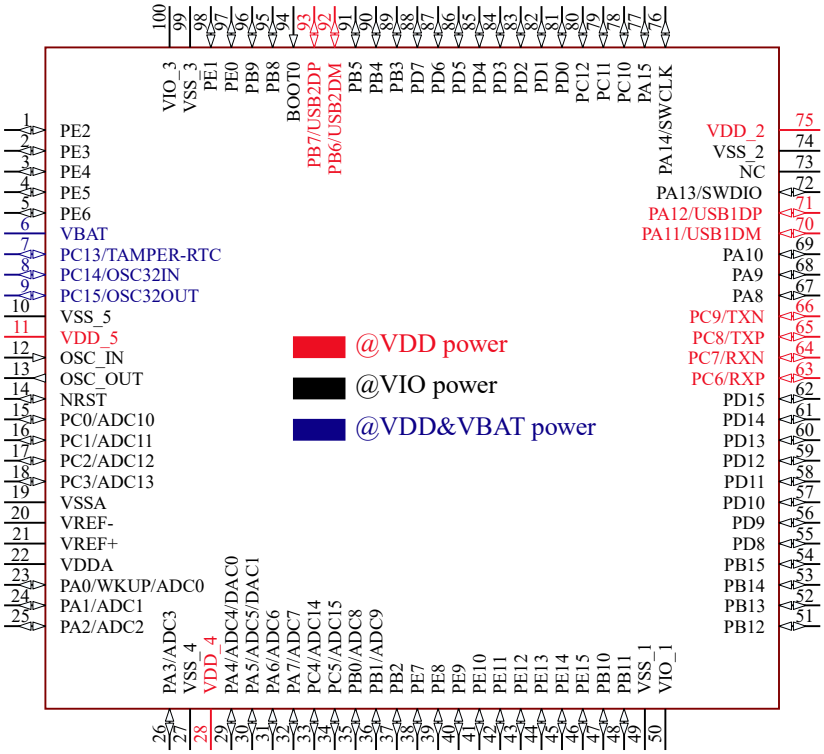



Figure 3-2 64-pin LQFP64

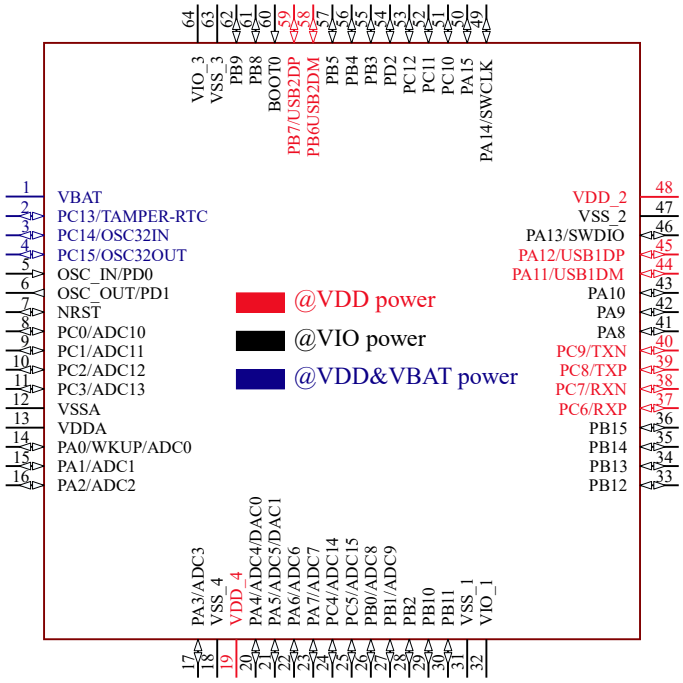


Figure 3-3 48-pin LQFP48

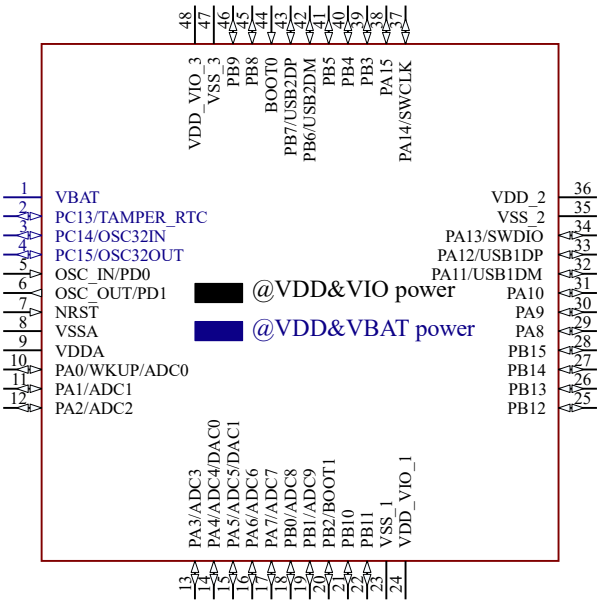
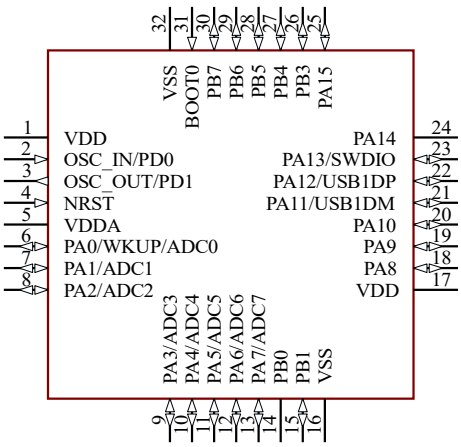



Figure 3-4 32-pin LQFP32



## 3.2 Wireless type

Figure 3-4 68-pin QFN68 X 8

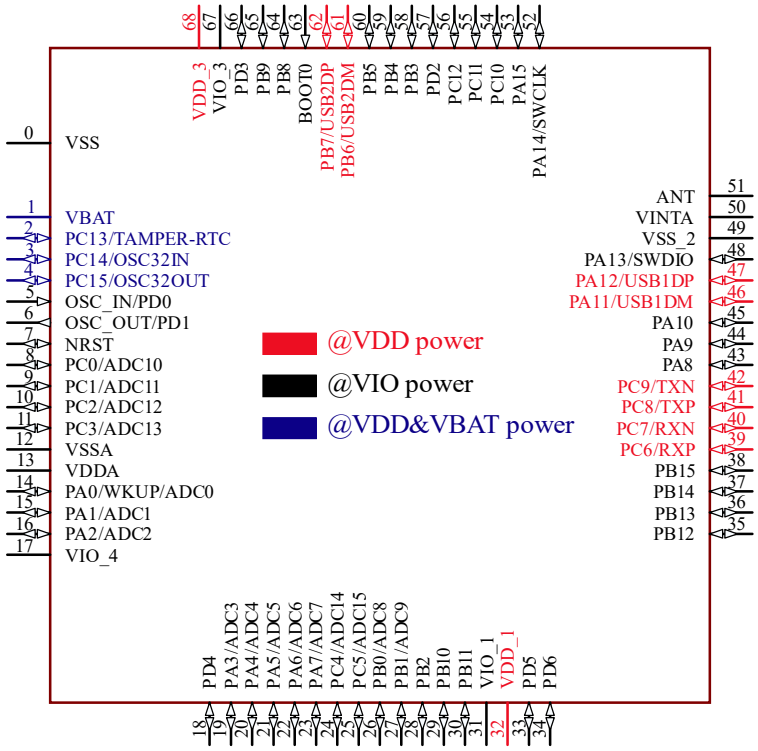



Figure 3-5 64-pin LQFP64M

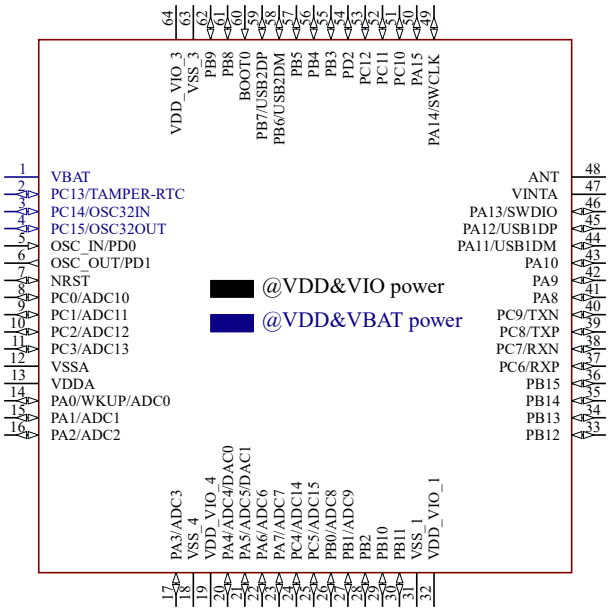


Figure 3-6 48-pin QFN48×5

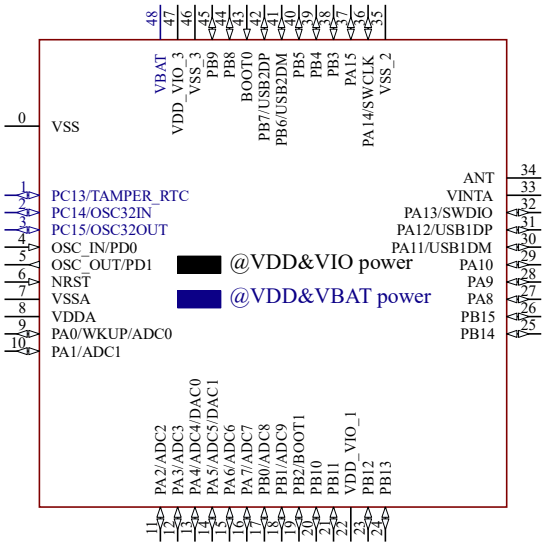
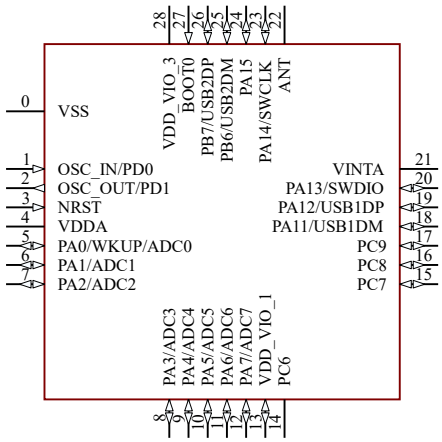



Figure 3-7 28-pin QFN28×4



## 3.3 Pin description

Table 3-1 CH32V303_305_307xx pin definition

*Note: The pin function in the table below refer to all functions and do not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.*

| Pin number | | | Pin name | Pin type (1) | I/O Voltage Level | Main function (After reset) | Default multiplexing function | Remapping function |
|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64M | LQFP100 | | | | | | |
| - | - | 1 | PE2 | I/O | FT | PE2 | FSMC_A23 | TIM10_BKIN |
| - | - | 2 | PE3 | I/O | FT | PE3 | FSMC_A19 | TIM10_CH1N |
| - | - | 3 | PE4 | I/O | FT | PE4 | FSMC_A20 | TIM10_CH2N |
| - | - | 4 | PE5 | I/O | FT | PE5 | FSMC_A21 | TIM10_CH3N |
| - | - | 5 | PE6 | I/O | FT | PE5 | FSMC_A22 | |
| 1 | 1 | 6 | $V_{BAT}$ | P | - | $V_{BAT}$ | | |
| 2 | 2 | 7 | PC13-TAMPER-RTC(2) | I/O | - | PC13(3) | TAMPER-RTC | TIM8_CH4 |
| 3 | 3 | 8 | PC14-OSC32_IN(2) | I/O/A | - | PC14(3) | OSC32_IN | TIM9_CH4 |
| 4 | 4 | 9 | PC15-OSC32_OUT(2) | I/O/A | - | PC15(3) | OSC32_OUT | TIM10_CH4 |
| - | - | 10 | $V_{SS\_5}$ | P | - | $V_{SS\_5}$ | | |
| - | - | 11 | $V_{DD\_5}$ | P | - | $V_{DD\_5}$ | | |
| 5 | 5 | 12 | OSC_IN | I/A | - | OSC_IN | | PD0(4) |
| 6 | 6 | 13 | OSC_OUT | O/A | - | OSC_OUT | | PD1(4) |
| 7 | 7 | 14 | NRST | I/O | - | NRST | | |
| - | 8 | 15 | PC0 | I/O/A | - | PC0 | ADC_IN10/TIM9_CH1N<br>UART6_TX<br>ETH_RGMII_RXC | |
| - | 9 | 16 | PC1 | I/O/A | - | PC1 | ADC_IN11/TIM9_CH2N<br>UART6_RX<br>ETH_MII_MDC<br>ETH_RMII_MDC<br>ETH_RGMII_RXCTL | |
| - | 10 | 17 | PC2 | I/O/A | - | PC2 | ADC_IN12/TIM9_CH3N<br>UART7_TX/OPA3_CH1N<br>ETH_MII_TXD2<br>ETH_RGMII_RXD0 | |
| - | 11 | 18 | PC3 | I/O/A | - | PC3 | ADC_IN13/TIM10_CH3<br>UART7_RX/OPA4_CH1N | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | ETH_MII_TX_CLK<br>ETH_RGMII_RXD1 | |
| 8 | 12 | 19 | $V_{SSA}$ | P | - | $V_{SSA}$ | | |
| - | - | 20 | $V_{REF-}$ | P | - | $V_{REF-}$ | | |
| - | - | 21 | $V_{REF+}$ | P | - | $V_{REF+}$ | | |
| 9 | 13 | 22 | $V_{DDA}$ | P | - | $V_{DDA}$ | | |
| 10 | 14 | 23 | PA0-WKUP | I/O/A | - | PA0 | WKUP/USART2_CTS<br>ADC_IN0/TIM2_CH1<br>TIM2_ETR/TIM5_CH1<br>TIM8_ETR/OPA4_OUT0<br>ETH_MII_CRS_WKUP<br>ETH_RGMII_RXD2 | |
| 11 | 15 | 24 | PA1 | I/O/A | - | PA1 | USART2_RTS/ADC_IN1<br>TIM5_CH2/TIM2_CH2<br>OPA3_OUT0<br>ETH_MII_RX_CLK<br>ETH_RMII_REF_CLK<br>ETH_RGMII_RXD3 | TIM9_BKIN |
| 12 | 16 | 25 | PA2 | I/O/A | - | PA2 | USART2_TX/TIM5_CH3<br>ADC_IN2/TIM2_CH3<br>TIM9_CH1/TIM9_ETR<br>OPA2_OUT0<br>ETH_MII_MDIO<br>ETH_RMII_MDIO<br>ETH_RGMII_GTXC | |
| 13 | 17 | 26 | PA3 | I/O/A | - | PA3 | USART2_RX/TIM5_CH4<br>ADC_IN3/TIM2_CH4<br>TIM9_CH2/OPA1_OUT0<br>ETH_MII_COL<br>ETH_RGMII_TXEN | |
| - | 18 | 27 | $V_{SS\_4}$ | P | - | $V_{SS\_4}$ | | |
| - | 19 | 28 | $V_{DD\_4}$ | P | - | $V_{DD\_4}$ | | |
| 14 | 20 | 29 | PA4 | I/O/A | - | PA4 | SPI1_NSS/USART2_CK<br>ADC_IN4/DAC_OUT1<br>TIM9_CH3/DVP_HSYNC | SPI3_NSS<br>I2S3_WS |
| 15 | 21 | 30 | PA5 | I/O/A | - | PA5 | SPI1_SCK/ADC_IN5<br>DAC_OUT2/OPA2_CH1N<br>DVP_VSYNC | TIM10_CH1N<br>USART1_CK |
| 16 | 22 | 31 | PA6 | I/O/A | - | PA6 | SPI1_MISO/TIM8_BKIN<br>ADC_IN6/TIM3_CH1<br>OPA1_CH1N/DVP_PCLK | TIM1_BKIN<br>UART7_TX<br>TIM10_CH2N |
| 17 | 23 | 32 | PA7 | I/O/A | - | PA7 | SPI1_MOSI/TIM8_CH1N<br>ADC_IN7/TIM3_CH2<br>OPA2_CH1P | TIM1_CH1N<br>UART7_RX<br>TIM10_CH3N |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | ETH_MII_RX_DV<br>ETH_RMII_CRS_DV<br>ETH_RGMII_TXD0 | |
| - | 24 | 33 | PC4 | I/O/A | - | PC4 | ADC_IN14/TIM9_CH4<br>UART8_TX/OPA4_CH1P<br>ETH_MII_RXD0<br>ETH_RMII_RXD0<br>ETH_RGMII_TXD1 | |
| - | 25 | 34 | PC5 | I/O/A | - | PC5 | ADC_IN15/TIM9_BKIN<br>UART8_RX/OPA3_CH1P<br>ETH_MII_RXD1<br>ETH_RMII_RXD1<br>ETH_RGMII_TXD2 | USART1_RTS |
| 18 | 26 | 35 | PB0 | I/O/A | - | PB0 | ADC_IN8/TIM3_CH3<br>TIM8_CH2N/OPA1_CH1P<br>ETH_MII_RXD2<br>ETH_RGMII_TXD3 | TIM1_CH2N<br>TIM9_CH1N<br>UART4_TX |
| 19 | 27 | 36 | PB1 | I/O/A | - | PB1 | ADC_IN9/TIM3_CH4<br>TIM8_CH3N/OPA4_CH0N<br>ETH_MII_RXD3<br>ETH_RGMII_125IN | TIM1_CH3N<br>TIM9_CH2N<br>UART4_RX |
| 20 | 28 | 37 | PB2 | I/O | FT | PB2/BOOT1 | OPA3_CH0N | TIM9_CH3N |
| - | - | 38 | PE7 | I/O/A | FT | PE7 | FSMC_D4/OPA3_OUT1 | TIM1_ETR |
| - | - | 39 | PE8 | I/O/A | FT | PE8 | FSMC_D5/OPA4_OUT1 | TIM1_CH1N/UART5_TX |
| - | - | 40 | PE9 | I/O | FT | PE9 | FSMC_D6 | TIM1_CH1/UART5_RX |
| - | - | 41 | PE10 | I/O | FT | PE10 | FSMC_D7 | TIM1_CH2N/UART6_TX |
| - | - | 42 | PE11 | I/O | FT | PE11 | FSMC_D8 | TIM1_CH2/UART6_RX |
| - | - | 43 | PE12 | I/O | FT | PE12 | FSMC_D9 | TIM1_CH3N/UART7_TX |
| - | - | 44 | PE13 | I/O | FT | PE13 | FSMC_D10 | TIM1_CH3/UART7_RX |
| - | - | 45 | PE14 | I/O/A | FT | PE14 | FSMC_D11/OPA2_OUT1 | TIM1_CH4/UART8_TX |
| - | - | 46 | PE15 | I/O/A | FT | PE15 | FSMC_D12/OPA1_OUT1 | TIM1_BKIN/UART8_RX |
| 21 | 29 | 47 | PB10 | I/O/A | FT | PB10 | I2C2_SCL/USART3_TX<br>OPA2_CH0N<br>ETH_MII_RX_ER | TIM2_CH3<br>TIM10_BKIN |
| 22 | 30 | 48 | PB11 | I/O/A | FT | PB11 | I2C2_SDA/USART3_RX<br>OPA1_CH0N | TIM2_CH4<br>TIM10_ETR |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | ETH_MII_TX_EN<br>ETH_RMII_TX_EN | |
| 23 | 31 | 49 | $V_{SS\_1}$ | P | | $V_{SS\_1}$ | | |
| - | 32 | 50 | $V_{IO\_1}$ | P | | $V_{IO\_1}$ | | |
| 24 | - | - | $V_{DD\_IO\_1}$ | P | | $V_{DD\_IO\_1}$ | | |
| 25 | 33 | 51 | PB12 | I/O/A | FT | PB12 | SPI2_NSS/I2S2_WS<br>I2C2_SMBA/USART3_CK<br>TIM1_BKIN/OPA4_CH0P<br>CAN2_RX/ETH_MII_TXD0<br>ETH_RMII_TXD0 | |
| 26 | 34 | 52 | PB13 | I/O/A | FT | PB13 | SPI2_SCK/I2S2_CK<br>USART3_CTS/TIM1_CH1N<br>OPA3_CH0P/CAN2_TX<br>ETH_MII_TXD1<br>ETH_RMII_TXD1 | |
| 27 | 35 | 53 | PB14 | I/O/A | FT | PB14 | SPI2_MISO/TIM1_CH2N<br>USART3_RTS/OPA2_CH0P | |
| 28 | 36 | 54 | PB15 | I/O/A | FT | PB15 | SPI2_MOSI/I2S2_SD<br>TIM1_CH3N/OPA1_CH0P | USART1_TX |
| - | - | 55 | PD8 | I/O | FT | PD8 | FSMC_D13 | USART3_TX/TIM9_CH1N<br>ETH_MII_RX_DV<br>ETH_RMII_CRS_DV |
| - | - | 56 | PD9 | I/O | FT | PD9 | FSMC_D14 | USART3_RX<br>TIM9_CH1/TIM9_ETR<br>ETH_MII_RXD0<br>ETH_RMII_RXD0 |
| - | - | 57 | PD10 | I/O | FT | PD10 | FSMC_D15 | USART3_CK/TIM9_CH2N<br>ETH_MII_RXD1<br>ETH_RMII_RXD1 |
| - | - | 58 | PD11 | I/O | FT | PD11 | FSMC_A16 | USART3_CTS/TIM9_CH2<br>ETH_MII_RXD2 |
| - | - | 59 | PD12 | I/O | FT | PD12 | FSMC_A17 | TIM4_CH1/TIM9_CH3N<br>USART3_RTS<br>ETH_MII_RXD3 |
| - | - | 60 | PD13 | I/O | FT | PD13 | FSMC_A18 | TIM4_CH2/TIM9_CH3 |
| - | - | 61 | PD14 | I/O | FT | PD14 | FSMC_D0 | TIM4_CH3/TIM9_BKIN |
| - | - | 62 | PD15 | I/O | FT | PD15 | FSMC_D1 | TIM4_CH4/TIM9_CH4 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | 37 | 63 | PC6 | I/O | FT | PC6 | I2S2_MCK/TIM8_CH1<br>SDIO_D6/ETH_RXP | TIM3_CH1 |
| - | 38 | 64 | PC7 | I/O | FT | PC7 | I2S3_MCK/TIM8_CH2<br>SDIO_D7/ETH_RXN | TIM3_CH2 |
| - | 39 | 65 | PC8 | I/O | FT | PC8 | TIM8_CH3/SDIO_D0<br>ETH_TXP/DVP_D2 | TIM3_CH3 |
| - | 40 | 66 | PC9 | I/O | FT | PC9 | TIM8_CH4/SDIO_D1<br>ETH_TXN/DVP_D3 | TIM3_CH4 |
| 29 | 41 | 67 | PA8 | I/O | FT | PA8 | USART1_CK<br>TIM1_CH1/MCO | |
| 30 | 42 | 68 | PA9 | I/O | FT | PA9 | USART1_TX/TIM1_CH2<br>OTG_FS_VBUS/DVP_D0 | USART1_RTS |
| 31 | 43 | 69 | PA10 | I/O | FT | PA10 | USART1_RX/TIM1_CH3<br>OTG_FS_ID/DVP_D1 | USART1_CK |
| 32 | 44 | 70 | PA11 | I/O/<br>A | FT | PA11 | USART1_CTS/USBDM<br>CAN1_RX/TIM1_CH4<br>OTG_FS_DM | |
| 33 | 45 | 71 | PA12 | I/O/<br>A | FT | PA12 | USART1_RTS/USBDP<br>CAN1_TX/TIM1_ETR<br>TIM10_CH1N<br>OTG_FS_DP | |
| 34 | 46 | 72 | PA13 | I/O | FT | SWDIO | TIM10_CH2N | PA13/TIM8_CH1N |
| - | - | 73 | Unused | | | | | |
| 35 | 47 | 74 | $V_{SS\_2}$ | P | - | $V_{SS\_2}$ | | |
| 36 | 48 | 75 | $V_{DD\_2}$ | P | - | $V_{DD\_2}$ | | |
| 37 | 49 | 76 | PA14 | I/O | FT | SWCLK | TIM10_CH3N | TIM8_CH2N/UART8_TX<br>PA14 |
| 38 | 50 | 77 | PA15 | I/O | FT | PA15 | SPI3_NSS<br>I2S3_WS | TIM2_CH1/TIM2_ETR<br>PA15/SPI1_NSS<br>TIM8_CH3N/UART8_RX |
| - | 51 | 78 | PC10 | I/O | FT | PC10 | UART4_TX/SDIO_D2<br>TIM10_ETR/DVP_D8 | USART3_TX<br>SPI3_SCK/I2S3_CK |
| - | 52 | 79 | PC11 | I/O | FT | PC11 | UART4_RX/SDIO_D3<br>TIM10_CH4/DVP_D4 | USART3_RX<br>SPI3_MISO |
| - | 53 | 80 | PC12 | I/O | FT | PC12 | UART5_TX/SDIO_CK<br>TIM10_BKIN/DVP_D9 | USART3_CK<br>SPI3_MOSI/I2S3_SD |
| - | - | 81 | PD0 | I/O/<br>A | FT | PD0 | FSMC_D2 | CAN1_RX/TIM10_ETR |
| - | - | 82 | PD1 | I/O/<br>A | FT | PD1 | FSMC_D3 | CAN1_TX/TIM10_CH1 |
| - | 54 | 83 | PD2 | I/O | FT | PD2 | TIM3_ETR/UART5_RX<br>SDIO_CMD/DVP_D11 | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | 84 | PD3 | I/O | FT | PD3 | FSMC_CLK | USART2_CTS<br>TIM10_CH2 |
| - | - | 85 | PD4 | I/O | FT | PD4 | FSMC_NOE | USART2_RTS |
| - | - | 86 | PD5 | I/O | FT | PD5 | FSMC_NWE | USART2_TX<br>TIM10_CH3 |
| - | - | 87 | PD6 | I/O | FT | PD6 | FSMC_NWAIT/DVP_D10 | USART2_RX |
| - | - | 88 | PD7 | I/O | FT | PD7 | FSMC_NE1<br>FSMC_NCE2 | USART2_CK<br>TIM10_CH4 |
| 39 | 55 | 89 | PB3 | I/O | FT | PB3 | SPI3_SCK<br>I2S3_CK | TIM2_CH2/SPI1_SCK<br>TIM10_CH1 |
| 40 | 56 | 90 | PB4 | I/O | FT | PB4 | SPI3_MISO | TIM3_CH1<br>SPI1_MISO/UART5_TX<br>TIM10_CH2 |
| 41 | 57 | 91 | PB5 | I/O | - | PB5 | I2C1_SMBA/SPI3_MOSI<br>I2S3_SD<br>ETH_MII_PPS_OUT<br>ETH_RMII_PPS_OUT | TIM3_CH2/SPI1_MOSI<br>CAN2_RX<br>TIM10_CH3<br>UART5_RX |
| 42 | 58 | 92 | PB6 | I/O | FT | PB6 | I2C1_SCL/TIM4_CH1<br>USBHD_DM/DVP_D5<br>USBHS_DM | USART1_TX<br>CAN2_TX<br>TIM8_CH1 |
| 43 | 59 | 93 | PB7 | I/O | FT | PB7 | I2C1_SDA/FSMC_NADV<br>TIM4_CH2/USBHD_DP<br>USBHS_DP | USART1_RX<br>TIM8_CH2 |
| 44 | 60 | 94 | BOOT0 | I | - | BOOT0 | | |
| 45 | 61 | 95 | PB8 | I/O/A | FT | PB8 | TIM4_CH3/SDIO_D4<br>TIM10_CH1/DVP_D6<br>ETH_MII_TXD3 | I2C1_SCL/CAN1_RX<br>UART6_TX<br>TIM8_CH3 |
| 46 | 62 | 96 | PB9 | I/O/A | FT | PB9 | TIM4_CH4/SDIO_D5<br>TIM10_CH2/DVP_D7 | I2C1_SDA/CAN1_TX<br>UART6_RX |
| - | - | 97 | PE0 | I/O | FT | PE0 | TIM4_ETR/FSMC_NBL0 | UART4_TX |
| - | - | 98 | PE1 | I/O | FT | PE1 | FSMC_NBL1 | UART4_RX |
| 47 | 63 | 99 | $V_{SS\_3}$ | P | - | $V_{SS\_3}$ | | |
| | 64 | 100 | $V_{IO\_3}$ | P | - | $V_{IO\_3}$ | | |
| 48 | - | - | $V_{DD\_IO\_3}$ | P | | $V_{DD\_IO\_3}$ | | |

Table 3-2 CH32V203xx pin definition

*Note: The pin function in the table below refer to all functions and do not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.*

| Pin number | | | Pin name | Pin type (1) | I/O voltage Level | Main function (After reset) | Default multiplexing function | Remapping function |
|---|---|---|---|---|---|---|---|---|
| LQFP32 | QFN48 | LQFP48 | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | 0 | - | | | | | | |
| - | 1 | 1 | $V_{BAT}$ | P | - | $V_{BAT}$ | | |
| - | 2 | 2 | PC13-TAMPER-RTC(2) | I/O | - | PC13(3) | TAMPER-RTC | |
| - | 3 | 3 | PC14-OSC32_IN(2) | I/O/A | - | PC14(3) | OSC32_IN | |
| - | 4 | 4 | PC15-OSC32_OUT(2) | I/O/A | - | PC15(3) | OSC32_OUT | |
| 2 | 5 | 5 | OSC_IN | I/A | - | OSC_IN | | PD0(4) |
| 3 | 6 | 6 | OSC_OUT | O/A | - | OSC_OUT | | PD1(4) |
| 4 | 7 | 7 | NRST | I/O | - | NRST | | |
| | 8 | 8 | $V_{SSA}$ | P | - | $V_{SSA}$ | | |
| 5 | 9 | 9 | $V_{DDA}$ | P | - | $V_{DDA}$ | | |
| 6 | 10 | 10 | PA0-WKUP | I/O/A | - | PA0 | WKUP/USART2_CTS ADC_IN0/TIM2_CH1 TIM2_ETR | |
| 7 | 11 | 11 | PA1 | I/O/A | - | PA1 | USART2_RTS/ADC_IN1 TIM2_CH2 | |
| 8 | 12 | 12 | PA2 | I/O/A | - | PA2 | USART2_TX/ADC_IN2 TIM2_CH3/OPA2_OUT0 | |
| 9 | 13 | 13 | PA3 | I/O/A | - | PA3 | USART2_RX/ADC_IN3 TIM2_CH4/OPA1_OUT0 | |
| 10 | 14 | 14 | PA4 | I/O/A | - | PA4 | SPI1_NSS/USART2_CK ADC_IN4/OPA2_OUT1 | |
| 11 | 15 | 15 | PA5 | I/O/A | - | PA5 | SPI1_SCK/ADC_IN5 OPA2_CH1N | USART1_CK |
| 12 | 16 | 16 | PA6 | I/O/A | - | PA6 | SPI1_MISO/ADC_IN6 TIM3_CH1/OPA1_CH1N | TIM1_BKIN |
| 13 | 17 | 17 | PA7 | I/O/A | - | PA7 | SPI1_MOSI/ADC_IN7 TIM3_CH2/OPA2_CH1P | TIM1_CH1N |
| 14 | 18 | 18 | PB0 | I/O/A | - | PB0 | ADC_IN8/TIM3_CH3 OPA1_CH1P | TIM1_CH2N |
| 15 | 19 | 19 | PB1 | I/O/A | - | PB1 | ADC_IN9/TIM3_CH4 OPA1_OUT1 | TIM1_CH3N |
| - | 20 | 20 | PB2 | I/O | FT | PB2/BOOT1 | | |
| - | 21 | 21 | PB10 | I/O/A | FT | PB10 | I2C2_SCL/USART3_TX | TIM2_CH3 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | OPA2_CH0N | |
| - | 22 | 22 | PB11 | I/O/A | FT | PB11 | I2C2_SDA/USART3_RX<br>OPA1_CH0N | TIM2_CH4 |
| 16 | 23 | 23 | $V_{SS\_1}$ | P | | $V_{SS\_1}$ | | |
| 17 | 24 | 24 | $V_{DD\_IO\_1}$ | P | | $V_{DD\_IO\_1}$ | | |
| - | 25 | 25 | PB12 | I/O/A | FT | PB12 | SPI2_NSS/I2C2_SMBA<br>USART3_CK/TIM1_BKIN | |
| - | 26 | 26 | PB13 | I/O/A | FT | PB13 | SPI2_SCK/USART3_CTS<br>TIM1_CH1N | |
| - | 27 | 27 | PB14 | I/O/A | FT | PB14 | SPI2_MISO/TIM1_CH2N<br>USART3_RTS/OPA2_CH0P | |
| - | 28 | 28 | PB15 | I/O/A | FT | PB15 | SPI2_MOSI/TIM1_CH3N<br>OPA1_CH0P | USART1_TX |
| 18 | 29 | 29 | PA8 | I/O | FT | PA8 | USART1_CK<br>TIM1_CH1/MCO | |
| 19 | 30 | 30 | PA9 | I/O | FT | PA9 | USART1_TX/TIM1_CH2 | USART1_RTS |
| 20 | 31 | 31 | PA10 | I/O | FT | PA10 | USART1_RX/TIM1_CH3 | USART1_CK |
| 21 | 32 | 32 | PA11 | I/O/A | FT | PA11 | USART1_CTS/USBDM<br>CAN1_RX/TIM1_CH4 | |
| 22 | 33 | 33 | PA12 | I/O/A | FT | PA12 | USART1_RTS/USBDP<br>CAN1_TX/TIM1_ETR | |
| 23 | 34 | 34 | PA13 | I/O | FT | SWDIO | | PA13 |
| - | 35 | 35 | $V_{SS\_2}$ | P | - | $V_{SS\_2}$ | | |
| - | 36 | 36 | $V_{DD\_2}$ | P | - | $V_{DD\_2}$ | | |
| 24 | 37 | 37 | PA14 | I/O | FT | SWCLK | | PA14 |
| 25 | 38 | 38 | PA15 | I/O | FT | PA15 | | TIM2_CH1/TIM2_ETR<br>PA15/SPI1_NSS |
| 26 | 39 | 39 | PB3 | I/O | FT | PB3 | | TIM2_CH2/SPI1_SCK |
| 27 | 40 | 40 | PB4 | I/O | FT | PB4 | | TIM3_CH1/SPI1_MISO |
| 28 | 41 | 41 | PB5 | I/O | - | PB5 | I2C1_SMBA | TIM3_CH2/SPI1_MOSI |
| 29 | 42 | 42 | PB6 | I/O | FT | PB6 | I2C1_SCL/TIM4_CH1<br>USBHD_DM | USART1_TX |
| 30 | 43 | 43 | PB7 | I/O | FT | PB7 | I2C1_SDA<br>TIM4_CH2/USBHD_DP | USART1_RX |
| 31 | 44 | 44 | BOOT0 | I | - | BOOT0 | | |
| - | 45 | 45 | PB8 | I/O/A | FT | PB8 | TIM4_CH3 | I2C1_SCL/CAN1_RX |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | 46 | 46 | PB9 | I/O/A | FT | PB9 | TIM4_CH4 | I2C1_SDA/CAN1_TX |
| 32 | 47 | 47 | $V_{SS\_3}$ | P | - | $V_{SS\_3}$ | | |
| 1 | 48 | 48 | $V_{DD\_IO\_3}$ | P | - | $V_{DD\_IO\_3}$ | | |

表 3-3 CH32V208xx pin definition

*Note: The pin function in the table below refer to all functions and do not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.*

| Pin number | | | | Pin name | Pin type (1) | I/O voltage Level | Main function (After reset) | Default multiplexing function | Remapping function |
|---|---|---|---|---|---|---|---|---|---|
| QFN28 | QFN48 | LQFP64 | QFN68 | | | | | | |
| 0 | 0 | - | 0 | $V_{SS}$ | P | - | $V_{SS}$ | | |
| 28 | 48 | 1 | 1 | $V_{BAT}$ | P | - | $V_{BAT}$ | | |
| - | 1 | 2 | 2 | PC13-TAMPER-RTC(2) | I/O | - | PC13(3) | TAMPER-RTC | |
| - | 2 | 3 | 3 | PC14-OSC32_IN(2) | I/O/A | - | PC14(3) | OSC32_IN | |
| - | 3 | 4 | 4 | PC15-OSC32_OUT(2) | I/O/A | - | PC15(3) | OSC32_OUT | |
| 1 | 4 | 5 | 5 | OSC_IN | I/A | - | OSC_IN | | |
| 2 | 5 | 6 | 6 | OSC_OUT | O/A | - | OSC_OUT | | |
| 3 | 6 | 7 | 7 | NRST | I/O | - | NRST | | |
| - | - | 8 | 8 | PC0 | I/O/A | - | PC0 | ADC_IN10 | |
| - | - | 9 | 9 | PC1 | I/O/A | - | PC1 | ADC_IN11 | |
| - | - | 10 | 10 | PC2 | I/O/A | - | PC2 | ADC_IN12 | |
| - | - | 11 | 11 | PC3 | I/O/A | - | PC3 | ADC_IN13 | |
| - | 7 | 12 | 12 | $V_{SSA}$ | P | - | $V_{SSA}$ | | |
| 4 | 8 | 13 | 13 | $V_{DDA}$ | P | - | $V_{DDA}$ | | |
| 5 | 9 | 14 | 14 | PA0-WKUP | I/O/A | - | PA0 | WKUP/USART2_CTS ADC_IN0/TIM2_CH1 TIM2_ETR/TIM5_CH1 | |
| 6 | 10 | 15 | 15 | PA1 | I/O/A | - | PA1 | USART2_RTS/ADC_IN1 TIM5_CH2/TIM2_CH2 | |
| 7 | 11 | 16 | 16 | PA2 | I/O/A | - | PA2 | USART2_TX/TIM5_CH3 ADC_IN2/TIM2_CH3 OPA2_OUT0 | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| - | - | - | 17 | $V_{IO\_4}$ | P | - | $V_{IO\_4}$ | | |
| - | - | - | 18 | PD4 | I/O | FT | PD4 | | USART2_RTS |
| 8 | 12 | 17 | 19 | PA3 | I/O/A | - | PA3 | USART2_RX/TIM5_CH4<br>ADC_IN3/TIM2_CH4<br>OPA1_OUT0 | |
| - | - | 18 | | $V_{SS\_4}$ | P | - | $V_{SS\_4}$ | | |
| - | - | 19 | - | $V_{DD\_IO\_4}$ | P | - | $V_{DD\_IO\_4}$ | | |
| 9 | 13 | 20 | 20 | PA4 | I/O/A | - | PA4 | SPI1_NSS/USART2_CK<br>ADC_IN4/OPA2_OUT1 | |
| 10 | 14 | 21 | 21 | PA5 | I/O/A | - | PA5 | SPI1_SCK/ADC_IN5<br>OPA2_CH1N | USART1_CK |
| 11 | 15 | 22 | 22 | PA6 | I/O/A | - | PA6 | SPI1_MISO/ADC_IN6<br>TIM3_CH1/OPA1_CH1N | TIM1_BKIN |
| 12 | 16 | 23 | 23 | PA7 | I/O/A | - | PA7 | SPI1_MOSI/ADC_IN7<br>TIM3_CH2/OPA2_CH1P | TIM1_CH1N |
| - | - | 24 | 24 | PC4 | I/O/A | - | PC4 | ADC_IN14 | |
| - | - | 25 | 25 | PC5 | I/O/A | - | PC5 | ADC_IN15 | USART1_RTS |
| - | 17 | 26 | 26 | PB0 | I/O/A | - | PB0 | ADC_IN8/TIM3_CH3<br>OPA1_CH1P | TIM1_CH2N<br>UART4_TX |
| - | 18 | 27 | 27 | PB1 | I/O/A | - | PB1 | ADC_IN9/TIM3_CH4<br>OPA1_OUT1 | TIM1_CH3N/UART4_RX |
| - | 19 | 28 | 28 | PB2 | I/O | FT | PB2/BOOT1 | | |
| - | 20 | 29 | 29 | PB10 | I/O/A | FT | PB10 | I2C2_SCL/USART3_TX<br>OPA2_CH0N | TIM2_CH3 |
| - | 21 | 30 | 30 | PB11 | I/O/A | FT | PB11 | I2C2_SDA/USART3_RX<br>OPA1_CH0N | TIM2_CH4 |
| - | - | 31 | - | $V_{SS\_1}$ | P | | $V_{SS\_1}$ | | |
| 13 | 22 | 32 | - | $V_{DD\_IO\_1}$ | P | | $V_{DD\_IO\_1}$ | | |
| - | - | - | 31 | $V_{IO\_1}$ | P | | $V_{IO\_1}$ | | |
| - | - | - | 32 | $V_{DD\_1}$ | P | | $V_{DD\_1}$ | | |
| - | - | - | 33 | PD5 | I/O | FT | PD5 | | USART2_TX |
| - | - | - | 34 | PD6 | I/O | FT | PD6 | | USART2_RX |
| - | 23 | 33 | 35 | PB12 | I/O/A | FT | PB12 | SPI2_NSS/I2C2_SMBA<br>USART3_CK<br>TIM1_BKIN | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| - | 24 | 34 | 36 | PB13 | I/O/A | FT | PB13 | SPI2_SCK<br>USART3_CTS<br>TIM1_CH1N | |
| - | 25 | 35 | 37 | PB14 | I/O/A | FT | PB14 | SPI2_MISO<br>TIM1_CH2N<br>USART3_RTS<br>OPA2_CH0P | |
| - | 26 | 36 | 38 | PB15 | I/O/A | FT | PB15 | SPI2_MOSI<br>TIM1_CH3N<br>OPA1_CH0P | USART1_TX |
| 14 | - | 37 | 39 | PC6 | I/O | FT | PC6 | ETH_RXP | TIM3_CH1 |
| 15 | - | 38 | 40 | PC7 | I/O | FT | PC7 | ETH_RXN | TIM3_CH2 |
| 16 | - | 39 | 41 | PC8 | I/O | FT | PC8 | ETH_TXP | TIM3_CH3 |
| 17 | - | 40 | 42 | PC9 | I/O | FT | PC9 | ETH_TXN | TIM3_CH4 |
| - | 27 | 41 | 43 | PA8 | I/O | FT | PA8 | USART1_CK<br>TIM1_CH1/MCO | |
| - | 28 | 42 | 44 | PA9 | I/O | FT | PA9 | USART1_TX/TIM1_CH2 | USART1_RTS |
| - | 29 | 43 | 45 | PA10 | I/O | FT | PA10 | USART1_RX/TIM1_CH3 | USART1_CK |
| 18 | 30 | 44 | 46 | PA11 | I/O/A | FT | PA11 | USART1_CTS/USBDM<br>CAN1_RX/TIM1_CH4 | |
| 19 | 31 | 45 | 47 | PA12 | I/O/A | FT | PA12 | USART1_RTS/USBDP<br>CAN1_TX/TIM1_ETR | |
| 20 | 32 | 46 | 48 | PA13 | I/O | FT | SWDIO | | PA13 |
| - | 35 | - | 49 | $V_{SS\_2}$ | P | - | $V_{SS\_2}$ | | |
| 21 | 33 | 47 | 50 | $V_{INTA}$ | P | - | $V_{INTA}$ | | |
| 22 | 34 | 48 | 51 | ANT | A | - | ANT | | |
| 23 | 36 | 49 | 52 | PA14 | I/O | FT | SWCLK | | PA14 |
| 24 | 37 | 50 | 53 | PA15 | I/O | FT | PA15 | | TIM2_CH1/TIM2_ETR<br>SPI1_NSS |
| - | - | 51 | 54 | PC10 | I/O | FT | PC10 | UART4_TX | USART3_TX |
| - | - | 52 | 55 | PC11 | I/O | FT | PC11 | UART4_RX | USART3_RX |
| - | - | 53 | 56 | PC12 | I/O | FT | PC12 | | USART3_CK |
| - | - | 54 | 57 | PD2 | I/O | FT | PD2 | TIM3_ETR | |
| - | 38 | 55 | 58 | PB3 | I/O | FT | PB3 | | TIM2_CH2/SPI1_SCK |
| - | 39 | 56 | 59 | PB4 | I/O | FT | PB4 | | TIM3_CH1/SPI1_MISO |
| - | 40 | 57 | 60 | PB5 | I/O | - | PB5 | I2C1_SMBA | TIM3_CH2/SPI1_MOSI |
| 25 | 41 | 58 | 61 | PB6 | I/O | FT | PB6 | I2C1_SCL/TIM4_CH1<br>USBHD_DM | USART1_TX |
| 26 | 42 | 59 | 62 | PB7 | I/O | FT | PB7 | I2C1_SDA<br>TIM4_CH2/USBHD_DP | USART1_RX |
| 27 | 43 | 60 | 63 | BOOT0 | I | - | BOOT0 | | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| - | 44 | 61 | 64 | PB8 | I/O/A | FT | PB8 | TIM4_CH3 | I2C1_SCL/CAN1_RX |
| - | 45 | 62 | 65 | PB9 | I/O/A | FT | PB9 | TIM4_CH4 | I2C1_SDA/CAN1_TX |
| - | - | - | 66 | PD3 | I/O | FT | PD3 | | USART2_CTS |
| - | 46 | 63 | - | $V_{SS\_3}$ | P | - | $V_{SS\_3}$ | | |
| 28 | 47 | 64 | - | $V_{DD\_IO\_3}$ | P | - | $V_{DD\_IO\_3}$ | | |
| - | - | - | 67 | $V_{IO\_3}$ | P | - | $V_{IO\_3}$ | | |
| - | - | - | 68 | $V_{DD\_3}$ | P | - | $V_{DD\_3}$ | | |

*Note 1: Abbreviations in the table*

*I = TTL/CMOS level Schmitt input;*

*O = CMOS level tri-state output;*

*A = analog signal input or output;*

*P = power supply;*

*FT = 5V tolerance;*

*ANT = RF signal input and output (antenna);*

*Note 2: The PC13, PC14 and PC15 pins are powered by the power's switch, and this power's switch can only absorb a limited current (3mA). Therefore, when these three pins are used as output pins, there are the following restrictions: only one pin can be used as an output at the same time. When used as an output pin, it can only work in 2MHz mode. The maximum drive load is 30pF and cannot be used as a current source (Such as driving LED).*

*Note 3: These pins are in the main function state when the backup area is powered on for the first time. Even after resetting, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the relevant chapters of the battery backup area and BKP register in the CH32xRM manual.*

*Note 4: Pin 5 and pin 6 of LQFP64M package are configured as OSC_IN and OSC_OUT function pins by default after chip reset. Software can reconfigure these two pins as PD0 and PD1. But for the LQFP100 package, since PD0 and PD1 are inherent functional pins, there is no need to re-image settings by software. For more detailed information, please refer to the Multiplex Function I/O Chapter and Debug Setting Chapter of the CH32xRM manual.*

# Chapter 4 Electrical Specification

## 4.1 Test conditions

Unless otherwise specified and marked, all voltages are based on $V_{SS}$.

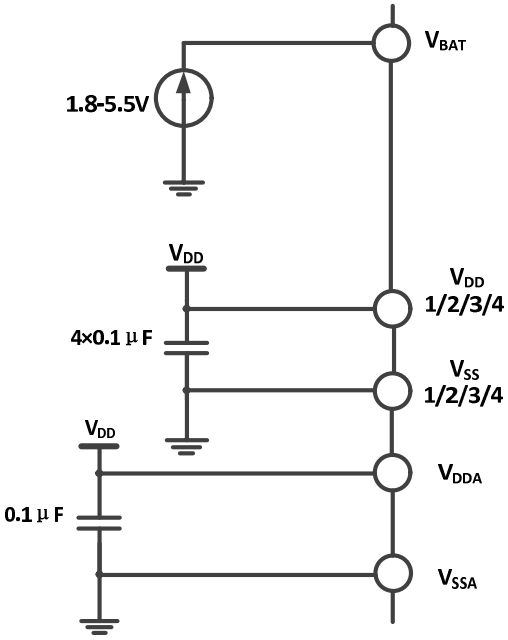
All minimum and maximum values will be guaranteed under the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature and $V_{DD}$ = 3.3 environment, which can be used for design guidance.

The data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested on the production line. On the basis of comprehensive evaluation, the minimum and maximum values are statistically obtained after sample testing. Unless were specifically explained, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Room temperature environment: 25℃

Power supply plan:

Figure 4-1 Typical circuit of power supply




## 4.2 Absolute maximum

Critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Table 4-1 Absolute maximum value parameter table

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient temperature during work | -40 | 85 | ℃ |
| $T_S$ | Ambient temperature during storage | -40 | 125 | ℃ |
| $V_{DD}$-$V_{SS}$ | External main supply voltage (including$V_{DDA}$ and $V_{DD}$) | -0.3 | 4.0 | V |

| | | | | |
|---|---|---|---|---|
| $V_{IO}$-$V_{SS}$ | IO domain side supply voltage | -0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on the FT (5V tolerant) pin | $V_{SS}$-0.3 | 5.5 | V |
| | Input voltage on other pins | $V_{SS}$-0.3 | $V_{DD}$+0.3 | |
| $\|\triangle V_{DD\_x}\|$ | Voltage difference between different main power supply pins | | 50 | mV |
| $\|\triangle V_{IO\_x}\|$ | Voltage difference between power supply pins of different IO terminals | | 50 | mV |
| $\|\triangle V_{SS\_x}\|$ | Voltage difference between different ground pins | | 50 | mV |
| $V_{ESD(HBM)}$ | ESD electrostatic discharge voltage (human body model, non-contact) | 4000 | | V |
| $I_{VDD}$[1] | The total current through the $V_{DD}$/$V_{DDA}$ power line (supply current) | | 50 | mA |
| $I_{Vss}$[1] | The total current (outgoing current) through the $V_{SS}$ ground wire | | 50 | |
| $I_{IO}$ | Sink current on any I/O and control pin | | 25 | |
| | Output current on any I/O and control pin | | -25 | |
| $I_{INJ(PIN)}$ | NRST pin injection current | | +/-5 | |
| | HSE's OSC_IN pin and LSE's OSC_IN pin injected current | | +/-5 | |
| | Injection current of other pins | | +/-5 | |
| $\sum I_{INJ(PIN)}$ | Total injection current of all IO and control pins | | +/-25 | |

*Note: 1. Normal work can reach the maximum current value.*

# 4.3 Electrical parameters

## 4.3.1 Working conditions

Table 4-2 General working conditions

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $F_{HCLK}$ | Internal AHB clock frequency | | | 144 | MHz |
| $F_{PCLK1}$ | Internal APB1 clock frequency | | | 144 | MHz |
| $F_{PCLK2}$ | Internal APB2 clock frequency | | | 144 | MHz |
| $V_{DD}$ | Standard working voltage | | 2.3 | 3.6 | V |
| $V_{IO}$ | Most IO pins output voltage | $V_{IO}$ must be less than $V_{DD}$ | 2.3 | 3.6 | V |
| $V_{DDA}$ | Analog part operating voltage (ADC is not used) | $V_{DDA}$ must be the same as $V_{IO}$, $V_{REF+}$ can not be higher than $V_{DDA}$, $V_{REF-}$ is equal to $V_{SS}$ | 2.3 | 3.6 | V |
| | Analog part of the working voltage (using ADC) | | 2.4 | | |
| $V_{BAT}$[1] | Backup unit operating voltage | Can not be greater than$V_{DD}$ | 1.8 | 3.6 | V |
| $T_A$ | Ambient temperature | | -40 | 85 | ℃ |
| $T_J$ | Junction temperature range | | -40 | 85 | ℃ |

*注：1.电池到 $V_{BAT}$ 连线要尽可能的短。*

表 4-3 上电和掉电条件

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rising rate | | 0 | ∞ | us/V |
| | $V_{DD}$ falling rate | | 30 | ∞ | |

*Note: The connection between the battery and VBAT should be as short as possible.*

### 4.3.2 Features of built-in Reset and Power Control Module

Table 4-4 Reset and voltage monitoring, (PAD_PDR_SEL floats, PDR selects high threshold gear)

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$[1] | Programmable voltage detector level selection | PLS[2:0] = 000 (rising edge) | | 2.39 | | V |
| | | PLS[2:0] = 000 (falling edge) | | 2.31 | | V |
| | | PLS[2:0] = 001 (rising edge) | | 2.56 | | V |
| | | PLS[2:0] = 001 (falling edge) | | 2.48 | | V |
| | | PLS[2:0] = 010 (rising edge) | | 2.65 | | V |
| | | PLS[2:0] = 010 (falling edge) | | 2.57 | | V |
| | | PLS[2:0] = 011 (rising edge) | | 2.78 | | V |
| | | PLS[2:0] = 011 (falling edge) | | 2.69 | | V |
| | | PLS[2:0] = 100 (rising edge) | | 2.89 | | V |
| | | PLS[2:0] = 100 (falling edge) | | 2.81 | | V |
| | | PLS[2:0] = 101 (rising edge) | | 3.05 | | V |
| | | PLS[2:0] = 101 (falling edge) | | 2.96 | | V |
| | | PLS[2:0] = 110 (rising edge) | | 3.17 | | V |
| | | PLS[2:0] = 110 (falling edge) | | 3.08 | | V |
| | | PLS[2:0] = 111 (rising edge) | | 3.31 | | V |
| | | PLS[2:0] = 111 (falling edge) | | 3.21 | | V |
| $V_{PVDhyst}$ | PVD hysteresis | | | 0.1 | | V |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Rising edge | 1.49 | 1.59 | 1.7 | V |
| | | Falling edge | 1.46 | 1.57 | 1.69 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | 40 | | 110 | mV |
| $t_{RSTTEMPO}$ | Reset duration | | 5 | | 100 | mS |

*Note: 1. Normal temperature test value.*

Table 4-5 Reset and voltage monitoring, (PAD_PDR_SEL is grounded, PDR selects the low threshold)

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$[1] | Programmable voltage detector level selection | PLS[2:0] = 000 (rising edge) | | 2.18 | | V |
| | | PLS[2:0] = 000 (falling edge) | | 2.11 | | V |
| | | PLS[2:0] = 001 (rising edge) | | 2.32 | | V |
| | | PLS[2:0] = 001 (falling edge) | | 2.24 | | V |
| | | PLS[2:0] = 010 (rising edge) | | 2.37 | | V |
| | | PLS[2:0] = 010 (falling edge) | | 2.30 | | V |
| | | PLS[2:0] = 011 (rising edge) | | 2.48 | | V |
| | | PLS[2:0] = 011 (falling edge) | | 2.40 | | V |
| | | PLS[2:0] = 100 (rising edge) | | 2.57 | | V |
| | | PLS[2:0] = 100 (falling edge) | | 2.49 | | V |
| | | PLS[2:0] = 101 (rising edge) | | 3.69 | | V |
| | | PLS[2:0] = 101 (falling edge) | | 2.60 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | PLS[2:0] = 110 (rising edge) | | 2.77 | | V |
| | | PLS[2:0] = 110 (falling edge) | | 2.68 | | V |
| | | PLS[2:0] = 111 (rising edge) | | 2.86 | | V |
| | | PLS[2:0] = 111 (falling edge) | | 2.77 | | V |
| $V_{PVDhyst}$ | PVD hysteresis | | | 0.1 | | V |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Rising edge | 1.49 | 1.60 | 1.7 | V |
| | | Falling edge | 1.46 | 1.57 | 1.69 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | 40 | | 110 | mV |
| $t_{RSTTEMPO}$ | Reset duration | | 5 | | 100 | mS |

*Note: 1. Normal temperature test value.*

### 4.3.3 Built-in reference voltage

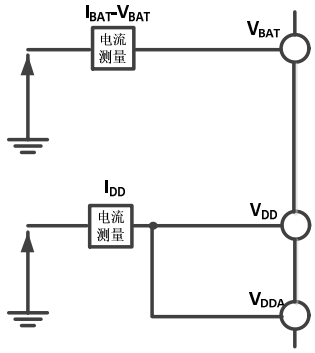
Table 4-6 Built-in reference voltage

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Built-in reference voltage | $T_A$ = -40℃～85℃ | 1.17 | 1.2 | 1.23 | V |
| $T_{S\_vrefint}$ | When reading the internal reference voltage, the ADC sampling time | | | | 17.1 | us |

### 4.3.4 Supply current characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and the executed code, etc. The current consumption measurement method is as follows:

Figure 4-2 Current consumption measurement




The microcontroller is in the following conditions:

Under normal temperature conditions, VDD = 3.3V, all IO ports are configured with pull-up inputs, enabling or disabling the power consumption of all peripheral clocks, without initializing peripheral functions.

Table 4-7 Typical current consumption in run mode, the data processing code runs from the internal Flash

| Symbol | Parameter | Condition | Typical value | Unit |
|---|---|---|---|---|

| | | | | Enable all peripherals | Disable all peripherals | |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in operating mode | External clock | $F_{HCLK}$ = 144MHz | | | mA |
| | | | $F_{HCLK}$ = 72MHz | | | |
| | | | $F_{HCLK}$ = 48MHz | | | |
| | | | $F_{HCLK}$ = 36MHz | | | |
| | | | $F_{HCLK}$ = 24MHz | | | |
| | | | $F_{HCLK}$ = 16MHz | | | |
| | | | $F_{HCLK}$ = 8MHz | | | |
| | | | $F_{HCLK}$ = 4MHz | | | |
| | | | $F_{HCLK}$ = 500KHz | | | |
| | | Runs on the high-speed internal RC oscillator (HSI), using AHB prescaler to reduce the frequency | $F_{HCLK}$ = 144MHz | | | |
| | | | $F_{HCLK}$ = 72MHz | | | |
| | | | $F_{HCLK}$ = 48MHz | | | |
| | | | $F_{HCLK}$ = 36MHz | | | |
| | | | $F_{HCLK}$ = 24MHz | | | |
| | | | $F_{HCLK}$ = 16MHz | | | |
| | | | $F_{HCLK}$ = 8MHz | | | |
| | | | $F_{HCLK}$ = 4MHz | | | |
| | | | $F_{HCLK}$ = 500KHz | | | |

*Note: The above are measured parameters.*

Table 4-8 Typical current consumption in sleep mode, data processing code runs from internal Flash or SRAM

| Symbol | Parameter | Condition | | Typical value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$ | Supply current in sleep mode (At this time, peripheral power supply and clock are maintained) | External clock | $F_{HCLK}$ = 144MHz | | | mA |
| | | | $F_{HCLK}$ = 72MHz | | | |
| | | | $F_{HCLK}$ = 48MHz | | | |
| | | | $F_{HCLK}$ = 36MHz | | | |
| | | | $F_{HCLK}$ = 24MHz | | | |
| | | | $F_{HCLK}$ = 16MHz | | | |
| | | | $F_{HCLK}$ = 8MHz | | | |
| | | | $F_{HCLK}$ = 4MHz | | | |
| | | | $F_{HCLK}$ = 500KHz | | | |
| | | Runs on the high-speed internal RC oscillator (HSI), using AHB prescaler to reduce the frequency | $F_{HCLK}$ = 144MHz | | | |
| | | | $F_{HCLK}$ = 72MHz | | | |
| | | | $F_{HCLK}$ = 48MHz | | | |
| | | | $F_{HCLK}$ = 36MHz | | | |
| | | | $F_{HCLK}$ = 24MHz | | | |
| | | | $F_{HCLK}$ = 16MHz | | | |
| | | | $F_{HCLK}$ = 8MHz | | | |
| | | | $F_{HCLK}$ = 4MHz | | | |
| | | | $F_{HCLK}$ = 500KHz | | | |

*Note: The above are measured parameters*

Table 4-9 Typical current consumption in stop and standby mode

| Symbol | Parameter | Condition | Typical value | Unit |
|---|---|---|---|---|
| $I_{DD}$ | Supply current in stop mode | The voltage regulator is in run mode, and the low-speed and high-speed internal RC oscillator and external oscillator are both off (no independent watchdog) | 85 | uA |
| | | The voltage regulator is in a low-power mode, the low-speed and high-speed internal RC oscillators and external oscillators are both off (no independent watchdog, PVD off) | 39 | |
| | Supply current in standby mode | Low-speed internal RC oscillator and independent watchdog are on | 1.2 | |
| | | The low-speed internal RC oscillator is in the on state, and the independent watchdog is in the off state | 1.1 | |
| | | Low-speed internal RC oscillator and independent watchdog are off, low-speed external oscillator and RTC are off | 0.4 | |
| $I_{DD\_VBAT}$ | Supply current in backup area (Remove $V_{DD}$ and $V_{DDA}$, only powered by $V_{BAT}$ | Low-speed external oscillator and RTC are on | 1.1 | |

*Note: The above are measured parameters.*

### 4.3.5 External clock characteristics

Table 4-10 From external high-speed clock

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{HSE\_ext}$ | External clock frequency | | 3 | 8 | 25 | MHz |
| $V_{HSEH}$[1] | OSC_IN input pin high level voltage | | $0.8V_{IO}$ | | $V_{IO}$ | V |
| $V_{HSEL}$[1] | OSC_IN input pin low-level voltage | | 0 | | $0.2V_{IO}$ | V |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | | 50 | | % |
| $I_L$ | OSC_IN input leakage current | | | | ±1 | uA |

*Note: 1. Failure to meet this condition may cause level recognition error.*

Figure 4-3 External high-frequency clock source circuit

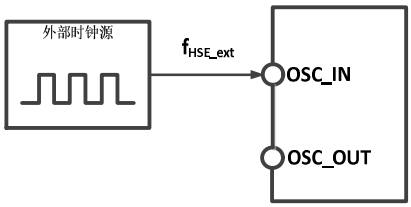



Table 4-11 From external low-speed clock

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{LSE\_ext}$ | User external clock frequency | | | 32.768 | 1000 | KHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(LSE)}$ | OSC32_IN input capacitance | | | 5 | | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | | 50 | | % |
| $I_L$ | OSC32_IN input leakage current | | | | ±1 | uA |

Figure 4-4 External low-frequency clock source circuit

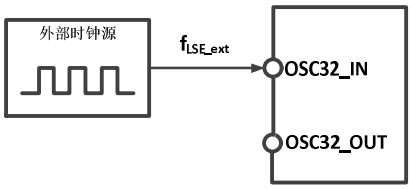



Table 4-12 High-speed external clock using a crystal/ceramic resonator

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{OSC\_IN}$ | Resonator frequency | | 3 | 8 | 25 | MHz |
| $R_F$ | Feedback resistance | | | 250 | | kΩ |
| C | Recommended load capacitance and corresponding crystal series impedance RS | $R_S$=60Ω[1] | | 20 | | pF |
| $I_2$ | HSE drive current | $V_{DD}$ = 3.3V，20p load | | 0.53 | | mA |
| $g_m$ | Transconductance of the oscillator | Start up | | 17.5 | | mA/V |
| $t_{SU(HSE)}$ | Start Time | $V_{DD}$ is stable, 8M crystal | | 2.5 | | ms |

*Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.*

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, $C_{L1}$=$C_{L2}$, generally 10～20pF is recommended.

Figure 4-5 Typical circuit of external 8M crystal

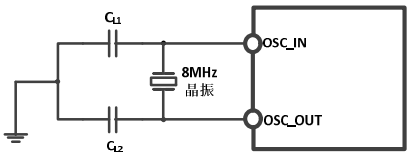


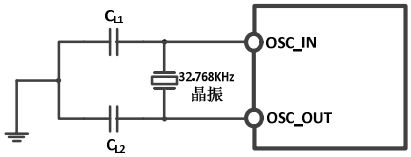

Table 4-13 Use a low-speed external clock generated by a crystal/ceramic resonator (f(LSE)=32.768KHz)

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistance | | | 5 | | MΩ |
| C | Recommended load capacitance and corresponding crystal serial impedance $R_S$ | $R_S$<70KΩ | | | 15 | pF |
| $i_2$ | LSE drive current | VDD = 3.3V | | 0.35 | | uA |
| $g_m$ | Transconductance of the oscillator | start up | | 25.3 | | uA/V |
| $t_{SU(LSE)}$ | Start Time | VDD is stable | | 800 | | mS |

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, CL1=CL2, generally 10～20pF is recommended.

Figure 4-6 Typical circuit of external 32.768K crystal




*Note: The load capacitance CL is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where $C_{stray}$ is the capacitance of the pin and the PCB board or PCB-related capacitance. Its typical value is between 2pF and 7pF between.*

### 4.3.6 Internal clock source characteristics

Table 4-14 Internal high-speed (HSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{HSI}$ | Frequency | | | 8 | | MHz |
| $DuCy_{HSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $ACC_{HSI}$ | Accuracy of HSI oscillator | TA = 0℃～70℃ | -1.6 | | 1.6 | % |
| | | TA = -40℃～85℃ | -2.3 | | 2.3 | % |
| $t_{SU(HSI)}$ | HSI oscillator start time | | | 10 | | us |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 8 | | MHz |

Table 4-15 Internal low-speed (LSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| $F_{LSI}$ | Frequency | | 25 | 39 | 60 | KHz |
| $DuCy_{LSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $t_{SU(LSI)}$ | LSI oscillator start-up time | | | 100 | | us |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | | | 0.6 | | uA |

### 4.3.7 PLL characteristics

Table 4-16 PLL characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{PLL\_IN}$ | PLL input clock | | 3 | 8 | 25 | MHz |
| | PLL input clock duty cycle | | 40 | | 60 | % |
| $F_{PLL\_OUT}$ | PLL multiplier output clock | | 18 | | 144[1] | MHz |
| $t_{LOCK}$ | PLL lock time | | | | 200 | us |

*Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.*

Table 4-17 PLL2 and PLL3 characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{PLL\_IN}$ | PLL input clock | | 3 | | 25 | MHz |
| | PLL input clock duty cycle1 | | 40 | | 60 | % |
| $F_{PLL\_OUT}$ | PLL multiplier output clock | | 30 | | 75[1] | MHz |
| $F_{VCO}$ | VCO output clock | | 60 | | 150 | MHz |
| $t_{LOCK1}$ | PLL lock time | | | | 200 | us |

*Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.*

### 4.3.8 Time to wake up from low power mode

Table 4-18 Low-power mode wake-up time

| Symbol | Parameter | Condition | Typical value | Unit |
|---|---|---|---|---|
| $t_{wusleep}$ | Wake up from sleep mode | Wake up using HSI RC clock | 6.84 | us |
| $t_{wustop}$ | Wake up from stop mode (voltage regulator is in run mode) | Wake on HSI RC clock | 261 | us |
| | Wake up from stop mode (voltage regulator is in low power mode) | Voltage regulator wake-up time from low power mode + HSI RC clock wake up + flash start | 261 | us |
| $t_{WUSTDBY}$ | Wake up from standby mode | Voltage regulator wake-up time from low power mode + HSI RC clock wake up + flash start | 440 | us |

### 4.3.9 Memory characteristics

Table 4-19 Flash characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$ = -40℃～85℃ | | 2 | | ms |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{prog\_page}$ | Page (256 bytes) programming time | $T_A$ = -40℃～85℃ | | 2 | | ms |
| $t_{erase\_page}$ | Page (256 bytes) erasing time | $T_A$ = -40℃～85℃ | | 16 | | ms |
| $t_{erase\_sec}$ | Sector (4K bytes) erasing time | $T_A$ = -40℃～85℃ | | 16 | | ms |
| $V_{prog}$ | Programming voltage | | 2.7 | | 3.6 | V |

Table 4-20 Flash life and data retention period

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Number of erasing and writing | $T_A$ = 25℃ | 10K | 80K[1] | | 次 |
| $t_{RET}$ | Data retention period | | 20 | | | 年 |

*Note: The actual measurement of the number of erasing and writing operations non-guaranteed.*

### 4.3.10 I/O Port characteristics

Table 4-21 General I/O static characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Standard I/O pin, input high level voltage | | 0.41*($V_{DD}$-1.8)+1.3 | | $V_{DD}$+0.3 | V |
| | FT IO pin, input high level voltage | $V_{DD}$ > 2V | 0.42*($V_{DD}$-1.8)+1 | | 5.5 | V |
| | | $V_{DD}$ <= 2V | | | 5.2 | |
| $V_{IL}$ | Standard I/O pin, input low-level voltage | | -0.3 | | 0.28*($V_{DD}$-1.8)+0.6 | V |
| | FT IO pin, input low-level voltage | | -0.3 | | 0.32*($V_{DD}$-1.8)+0.55 | V |
| $V_{hys}$ | Standard I/O pin Schmitt trigger voltage hysteresis | | 200 | | | mV |
| | FT IO pin Schmitt trigger voltage hysteresis | | 5% $V_{DD}$ | | | |
| $I_{lkg}$ | Input leakage current | Standard IO port | | | ±1 | uA |
| | | FT IO port | | | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistance | | 30 | 40 | 55 | KΩ |
| $R_{PD}$ | Weak pull-down equivalent resistance | | 30 | 40 | 55 | KΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

Output drive current characteristics

GPIO (General Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to $V_{OL}$/$V_{OH}$). In user applications, the total driving current of all IO pins cannot exceed the absolute maximum ratings given in section 4.2:

Table 4-22 Output voltage characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level,8 pins sink current | TTL port, $I_{IO}$ = +8mA | | 0.4 | V |
| $V_{OH}$ | Output high level,8 pins sink current | 2.7V< $V_{DD}$ <3.6V | $V_{DD}$-0.4 | | |

| | | | | | |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level,8 pins sink current | CMOS port, $I_{IO}$ = +8mA | | 0.4 | V |
| $V_{OH}$ | Output high level,8 pins sink current | 2.7V< $V_{DD}$ <3.6V | 2.3 | | |
| $V_{OL}$ | Output low level,8 pins sink current | $I_{IO}$ = +20mA | | 1.3 | V |
| $V_{OH}$ | Output high level,8 pins sink current | 2.7V< $V_{DD}$ <3.6V | $V_{DD}$-1.3 | | |
| $V_{OL}$ | Output low level,8 pins sink current | $I_{IO}$ = +6mA | | 0.4 | V |
| $V_{OH}$ | Output high level,8 pins sink current | 2.3V< $V_{DD}$ <2.7V | $V_{DD}$-1.3 | | |

*Note: In the above conditions, if multiple IO pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple IO pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal IO voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.*

Table 4-23 Input and output AC characteristics

| MODEx[1:0] Configuration | Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 （2MHz） | $F_{max(IO)out}$ | Maximum frequency | CL=50pF,$V_{DD}$=2.7-3.6V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low fall time | CL=50pF,$V_{DD}$=2.7-3.6V | | 125 | ns |
| | $t_{r(IO)out}$ | Output low to high rise time | | | 125 | ns |
| 01 （10MHz） | $F_{max(IO)out}$ | Maximum frequency | CL=50pF,$V_{DD}$=2.7-3.6V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low fall time | CL=50pF,$V_{DD}$=2.7-3.6V | | 25 | ns |
| | $t_{r(IO)out}$ | Output low to high rise time | | | 25 | ns |
| 11 （50MHz） | $F_{max(IO)out}$ | Maximum frequency | CL=30pF,$V_{DD}$=2.7-3.6V | | 50 | MHz |
| | | | CL=50pF,$V_{DD}$=2.7-3.6V | | 30 | MHz |
| | $t_{f(IO)out}$ | Output high to low fall time | CL=30pF,$V_{DD}$=2.7-3.6V | | 20 | ns |
| | | | CL=50pF,$V_{DD}$=2.7-3.6V | | 5 | ns |
| | $t_{r(IO)out}$ | Output low to high rise time | CL=30pF,$V_{DD}$=2.7-3.6V | | 8 | ns |
| | | | CL=50pF,$V_{DD}$=2.7-3.6V | | 12 | ns |
| | $t_{EXTIpw}$ | The EXTI controller detects the pulse width of the external signal | | 10 | | ns |

### 4.3.11 NRST pin characteristics

Table 4-24 External reset pin characteristics

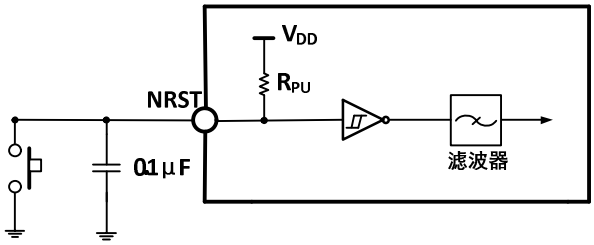
| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low-level voltage | | -0.3 | | 0.28*($V_{DD}$-1.8)+0.6 | V |
| $V_{IH(NRST)}$ | NRST input high level voltage | | 0.41*($V_{DD}$-1.8)+1.3 | | $V_{DD}$+0.3 | V |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | 200 | | | mV |
| $R_{PU}$[1] | Weak pull-up equivalent resistance | | 30 | 40 | 55 | KΩ |
| $V_{F(NRST)}$ | NRST input can be filtered pulse width | | | | 100 | ns |
| $V_{NF(NRST)}$ | NRST input cannot filter | | 300 | | | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| | pulse width | | | | | |

*Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).*

Circuit reference design and requirements:

Figure 4-7 Typical circuit of external reset pin




### 4.3.12 TIM Timer characteristics

Table 4-25 TIMx characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer reference clock | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72MHz | 13.9 | | ns |
| $F_{EXT}$ | Timer external clock frequency of CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 72MHz | 0 | 36 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 16 | 位 |
| $t_{COUNTER}$ | When the internal clock is selected, the 16-bit counter clock cycle | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72MHz | 0.0139 | 910 | us |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65535 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72MHz | | 59.6 | s |

### 4.3.13 I²C Interface characteristics

Figure 4-8 I²C bus timing diagram

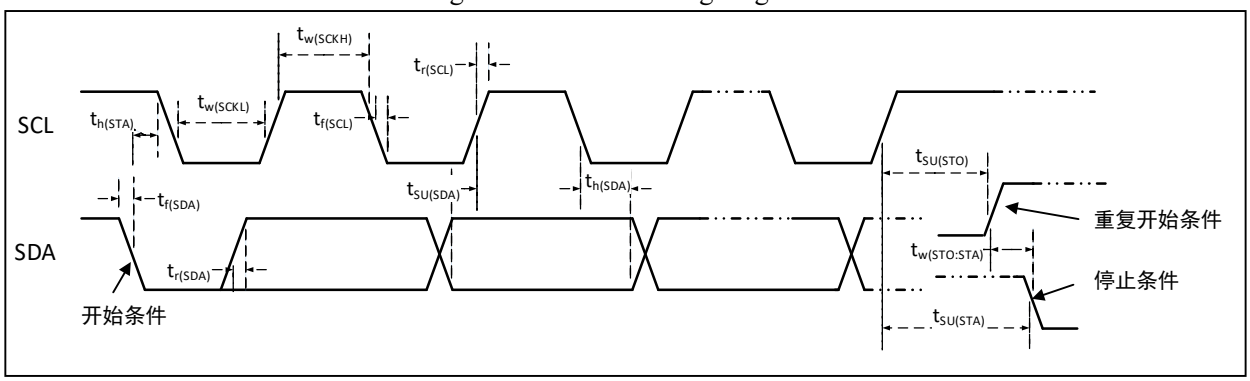



Table 4-26 I²C interface characteristics

| Symbol | Parameter | Standard I²C | | Fast I²C | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCKL)}$ | SCL clock low time | 4.7 | | 1.2 | | us |
| $t_{w(SCKH)}$ | SCL clock high time | 4.0 | | 0.6 | | us |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{SU(SDA)}$ | SDA data establishment time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data retention time | 0 | | 0 | 900 | ns |
| $t_{r(SDA)}/t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 | | ns |
| $t_{f(SDA)}/t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | | ns |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | us |
| $t_{SU(STA)}$ | Repeated start condition establishment time | 4.7 | | 0.6 | | us |
| $t_{SU(STO)}$ | Stop condition establishment time | 4.0 | | 0.6 | | us |
| $t_{w(STO:STA)}$ | Time from stop condition to start condition (bus free) | 4.7 | | 1.2 | | us |
| $C_b$ | Capacitive load of each bus | | 400 | | 400 | pF |

### 4.3.14 SPI interface characteristics

Figure 4-9 Timing diagram of SPI master mode

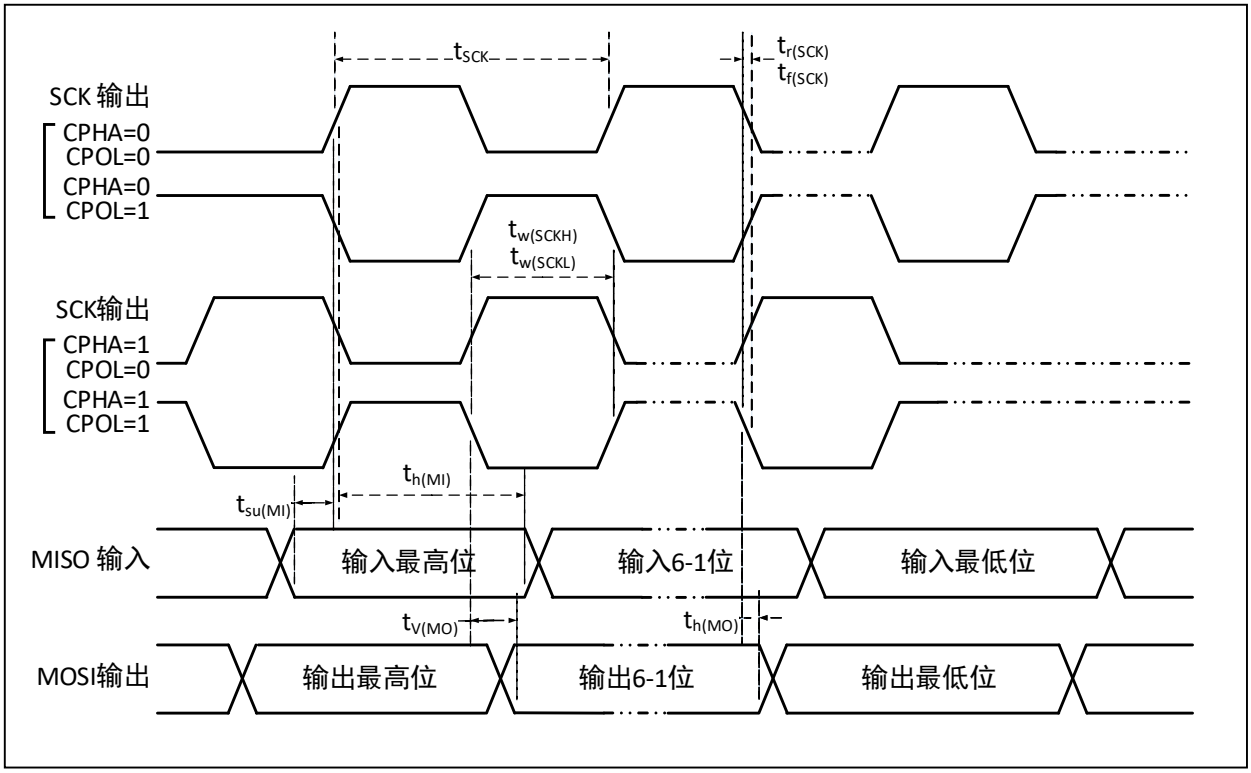


Figure 4-10 Timing diagram of SPI slave mode (CPHA=0)

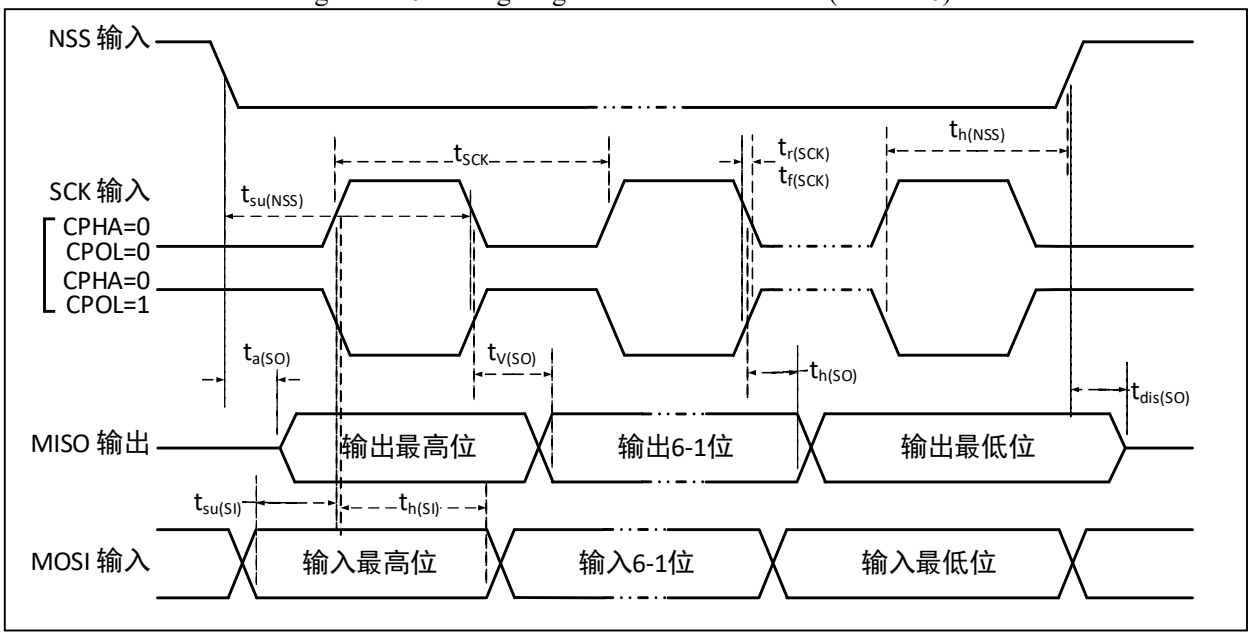



Figure 4-11 Timing diagram of SPI slave mode (CPHA=1)

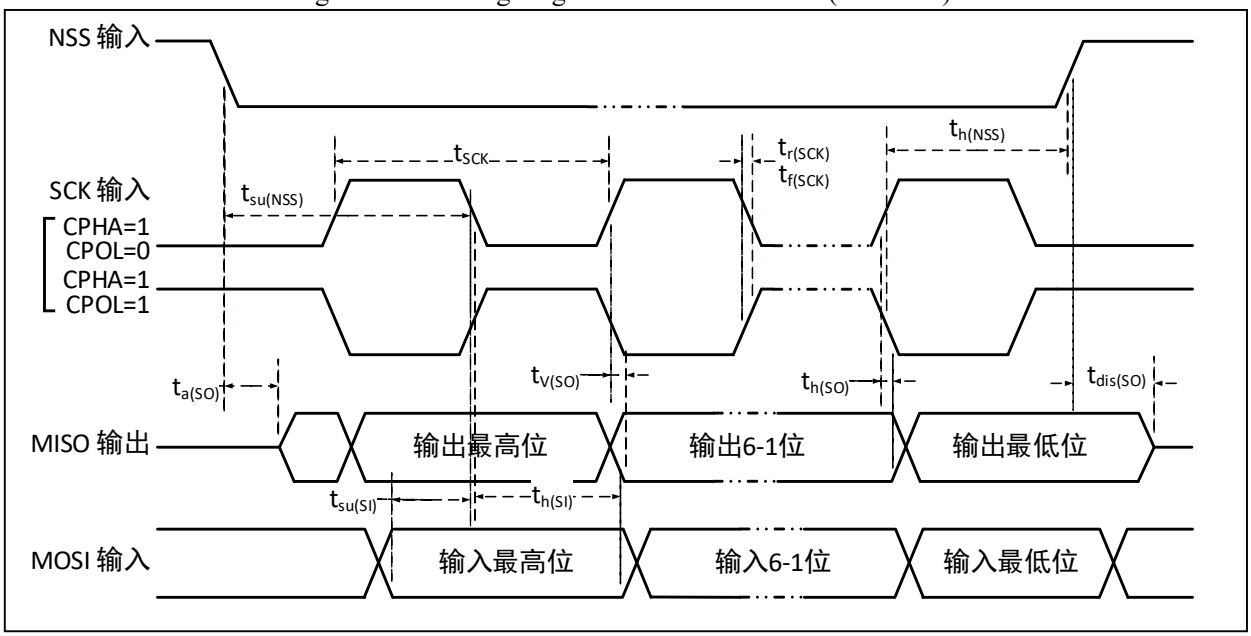



Table 4-27 SPI interface characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}/t_{SCK}$ | SPI clock frequency | Master mode | | 36 | MHz |
| | | Slave mode | | 36 | MHz |
| $t_{r(SCK)}/t_{f(SCK)}$ | SPI clock rise and fall time | Load capacitance:C = 30pF | | 20 | ns |
| $t_{SU(NSS)}$ | NSS establishment time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 36MHz, Prescaler factor = 4 | 40 | 60 | ns |
| $t_{SU(MI)}$ | Data input establishment time | Master mode | 5 | | ns |
| $t_{SU(SI)}$ | | Slave mode | 5 | | ns |

| | | | | | |
|---|---|---|---|---|---|
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | | ns |
| $t_{h(SI)}$ | | Slave mode | 4 | | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 20MHz | 0 | $1t_{PCLK}$ | ns |
| $t_{dis(SO)}$ | Data output inhibit time | Slave mode | 0 | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | Slave mode (After enabling edge) | | 25 | ns |
| $t_{V(MO)}$ | | Master mode (After enabling edge) | | 5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (After enabling edge) | 15 | | ns |
| $t_{h(MO)}$ | | Master mode (After enabling edge) | 0 | | ns |

### 4.3.15 I2S interface features

Figure 4-12 Timing diagram of I²S bus master mode (Philips protocol)

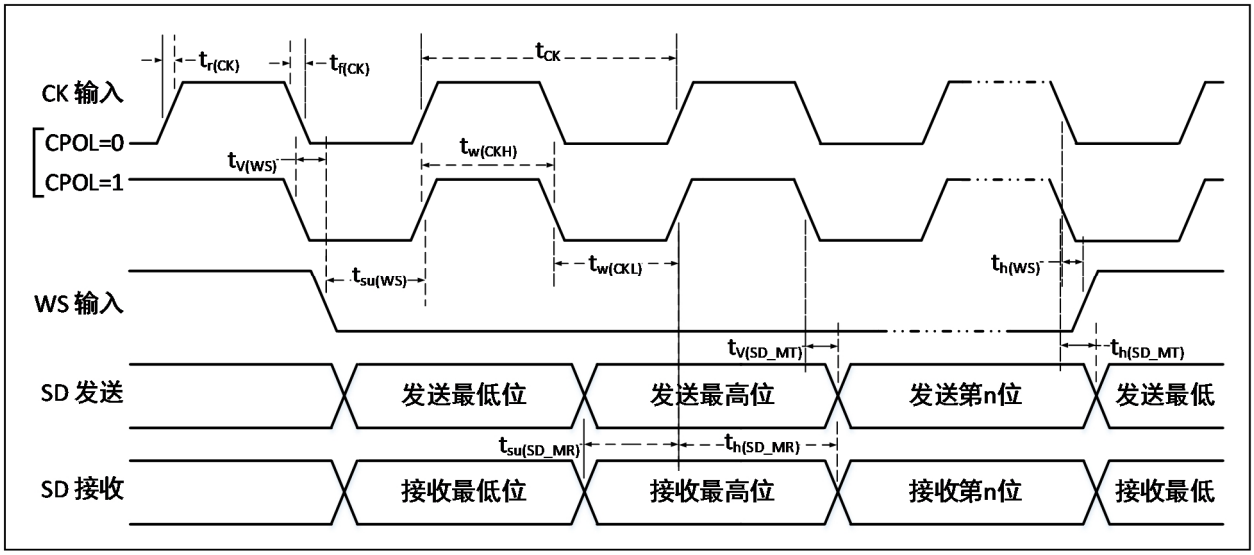



Figure 4-13 Timing diagram of I²S bus slave mode (Philips protocol)

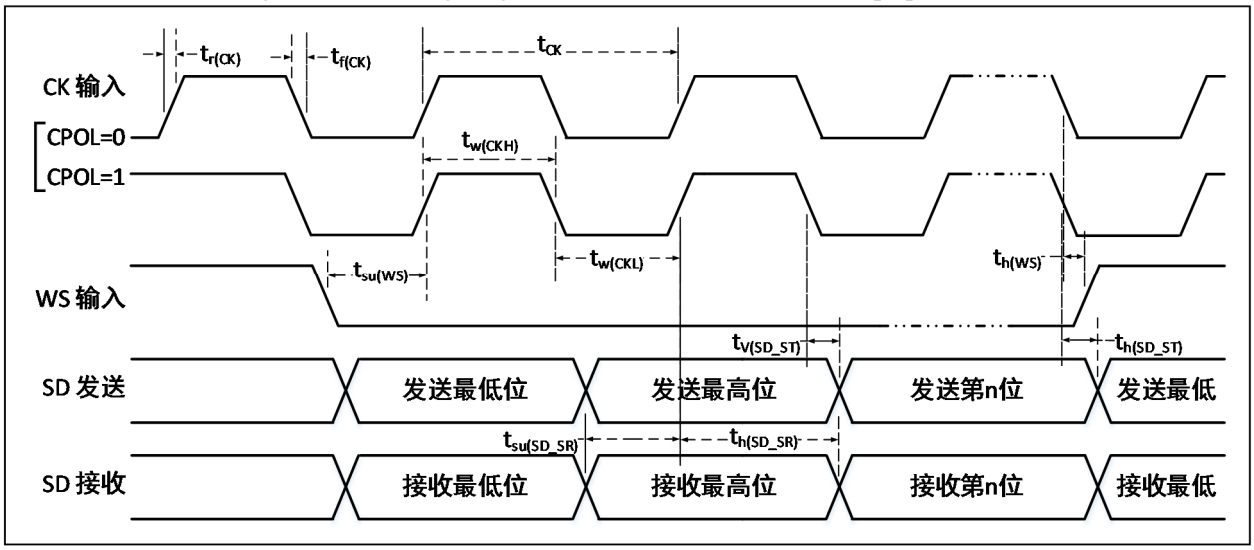


Table 4-28 I²S interface characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CK}/t_{CK}$ | I²S clock frequency | Master mode | | 8 | MHz |
| | | Slave mode | | 8 | MHz |
| $t_{r(CK)}/t_{f(CK)}$ | I²S clock rise and fall time | Load capacitance: C = 30pF | | 20 | ns |
| $t_{V(WS)}$ | WS effective time | Master mode | | 5 | ns |
| $t_{SU(WS)}$ | WS establishment time | Slave mode | 10 | | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | $2t_{PCLK}$ | | ns |
| | | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{w(CKH)}/t_{w(CKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 36MHz, Prescaler factor =4 | 40 | 60 | ns |
| $t_{SU(SD\_MR)}$ $t_{SU(SD\_SR)}$ | Data input establishment time | Master mode | 5 | | ns |
| | | Slave mode | 5 | | ns |
| $t_{h(SD\_MR)}$ $t_{h(SD\_SR)}$ | Data input hold time | Master mode | 5 | | ns |
| | | Slave mode | 4 | | ns |
| $t_{h(SD\_MT)}$ | Data output hold time | Master mode (After enabling edge) | | 5 | ns |
| $t_{h(SD\_ST)}$ | | Slave mode (After enabling edge) | | 5 | ns |
| $t_{V(SD\_MT)}$ | Data output valid time | Master mode (After enabling edge)) | | 5 | ns |
| $t_{v(SD\_ST)}$ | | Slave mode (After enabling edge) | | 4 | ns |

### 4.3.16 USB interface characteristics

Table 4-29 USB module characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | USB operating voltage | | 3.0 | 3.6 | V |
| $V_{SE}$ | Single-ended receiver threshold | $V_{DD}$ = 3.3V | 1.2 | 1.9 | V |
| $V_{OL}$ | Static output low level | | | 0.3 | V |
| $V_{OH}$ | Static output high level | | 2.8 | 3.6 | V |
| $V_{HSSQ}$ | High-speed suppression information detection threshold | | 100 | 150 | mV |
| $V_{HSDSC}$ | High-speed disconnection detection threshold | | 500 | 625 | mV |
| $V_{HSOI}$ | High-speed idle level | | -10 | 10 | mV |
| $V_{HSOH}$ | High-speed data high level | | 360 | 440 | mV |
| $V_{HSOL}$ | High-speed data low level | | -10 | 10 | mV |

### 4.3.17 SD/MMC Interface characteristics

Figure 4-14 Timing diagram of SD high-speed mode

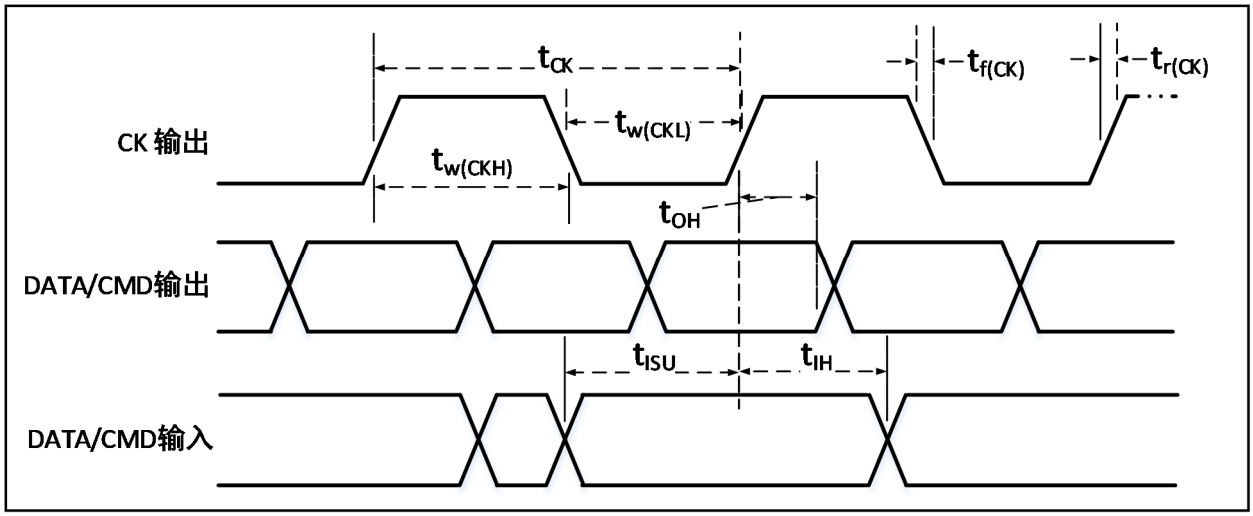



Figure 4-15 Timing diagram of SD default mode

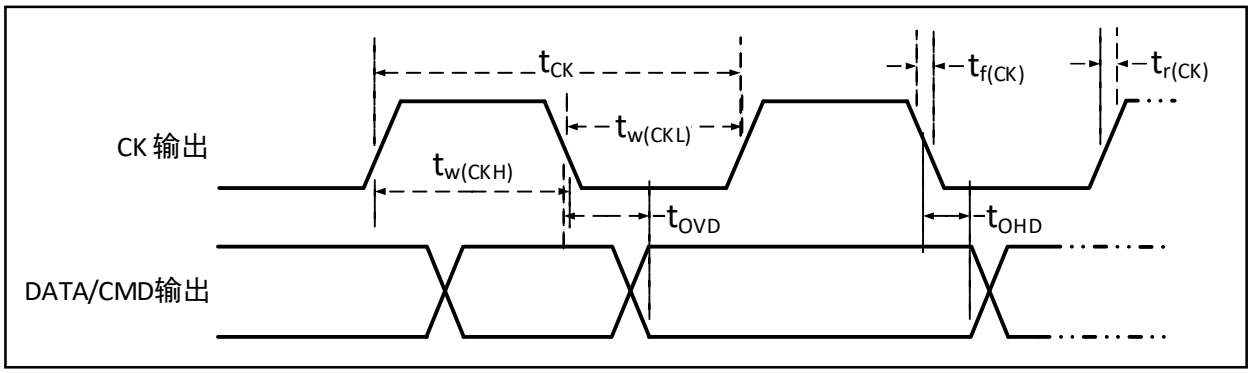



Table 4-30 SD/MMC interface characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CK}/t_{CK}$ | Clock frequency in data transfer mode | CL≤30pF | 0 | 48 | MHz |
| $t_{W(CKL)}$ | Clock low time | CL≤30pF | 6 | | ns |
| $t_{W(CKH)}$ | Clock high time | CL≤30pF | 6 | | |
| $t_{r(CK)}$ | Rise Time | CL≤30pF | | 4 | |
| $t_{f(CK)}$ | Fall time | CL≤30pF | | 4 | |
| CMD/DAT Input (refer to CK) | | | | | |
| $t_{ISU}$ | Enter the build time | CL≤30pF | 7 | | ns |
| $t_{IH}$ | Enter hold time | CL≤30pF | | 3 | |
| CMD/DAT output in MMC and SD high-speed mode (refer to CK) | | | | | |
| $t_{OV}$ | Output valid time | CL≤30pF | | 5 | ns |
| $t_{OH}$ | Output hold time | CL≤30pF | 4 | | |
| CMD/DAT output in SD default mode (refer to CK) | | | | | |
| $t_{OVD}$ | Output valid default time | CL≤30pF | | 8 | ns |
| $t_{OHD}$ | Output hold default time | CL≤30pF | 6 | | |

### 4.3.18 FSMC characteristic

Figure 4-16 Asynchronous bus multiplexing PSRAM/NOR read operation waveform

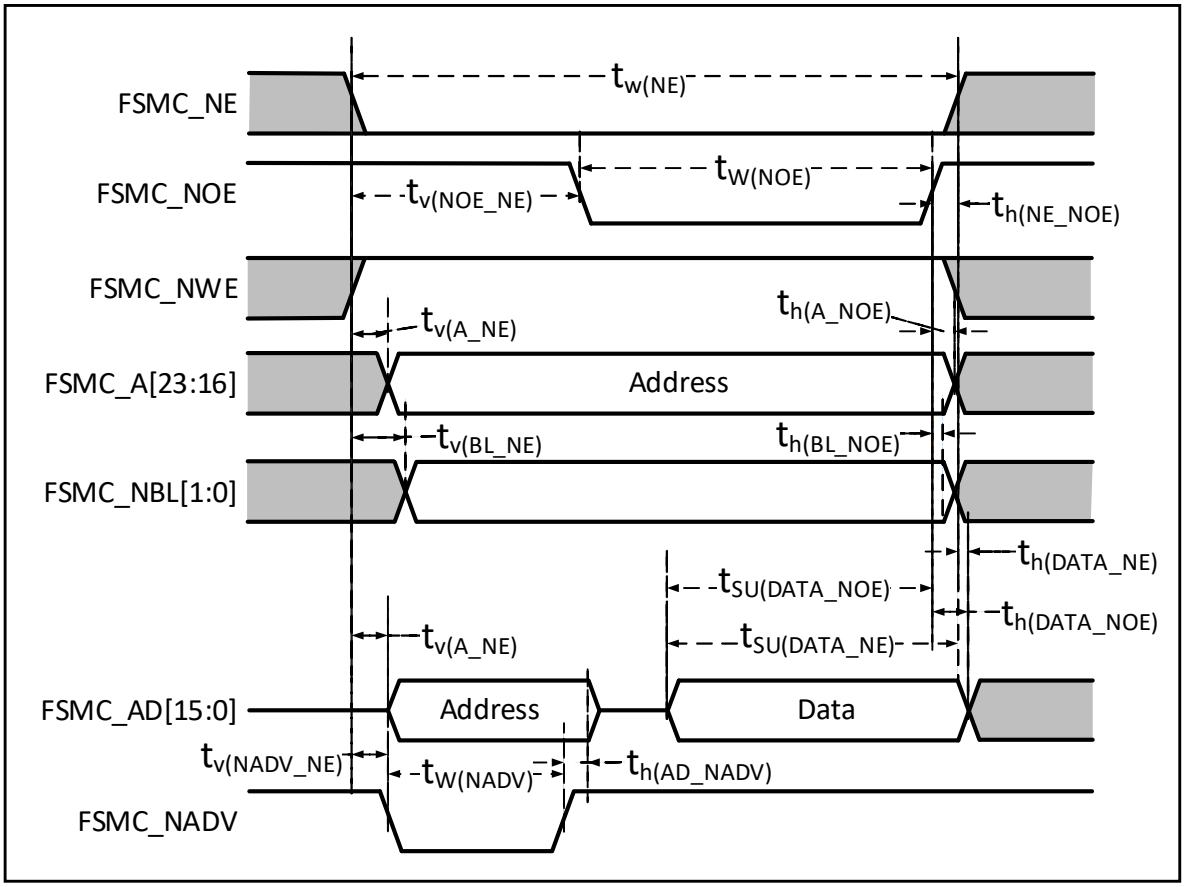



Table 4-31 PSRAM/NOR read operation timing of asynchronous bus multiplexing

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(NE)}$ | FSMC_NE low time | $7t_{HCLK}$ | | ns |
| $t_{V(NOE\_NE)}$ | FSMC_NE as low as FSMC_NOE as low | 0 | | |
| $t_{W(NOE)}$ | FSMC_NOE low time | $7t_{HCLK}$ | | |
| $t_{h(NE\_NOE)}$ | FSMC_NOE up to FSMC_NE high hold time | 0 | | |
| $t_{V(A\_NE)}$ | FSMC_NE as low as FSMC_A valid | 0 | 5 | |
| $t_{V(NADV\_NE)}$ | FSMC_NE as low as FSMC_NADV | 0 | 5 | |
| $t_{W(NADV)}$ | FSMC_NADV low time | $t_{HCLK}$ | | |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV is high | $2t_{HCLK}$ | | |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | 0 | | |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE is high | 0 | | |
| $t_{V(BL\_NE)}$ | FSMC_NE as low as FSMC_BL valid | 0 | 5 | |
| $t_{SU(DATA\_NE)}$ | Settling time from data to FSMC_NE high | $3t_{HCLK}$ | | |
| $t_{SU(DATA\_NOE)}$ | Data to FSMC_NOE high establishment time | $3t_{HCLK}$ | | |
| $t_{h(DATA\_NE)}$ | Data retention time after FSMC_NE is high | 0 | | |
| $t_{h(DATA\_NOE)}$ | Data retention time after FSMC_NOE is high | 0 | | |

Figure 4-17 Asynchronous bus multiplexing PARAM/NOR write operation waveform

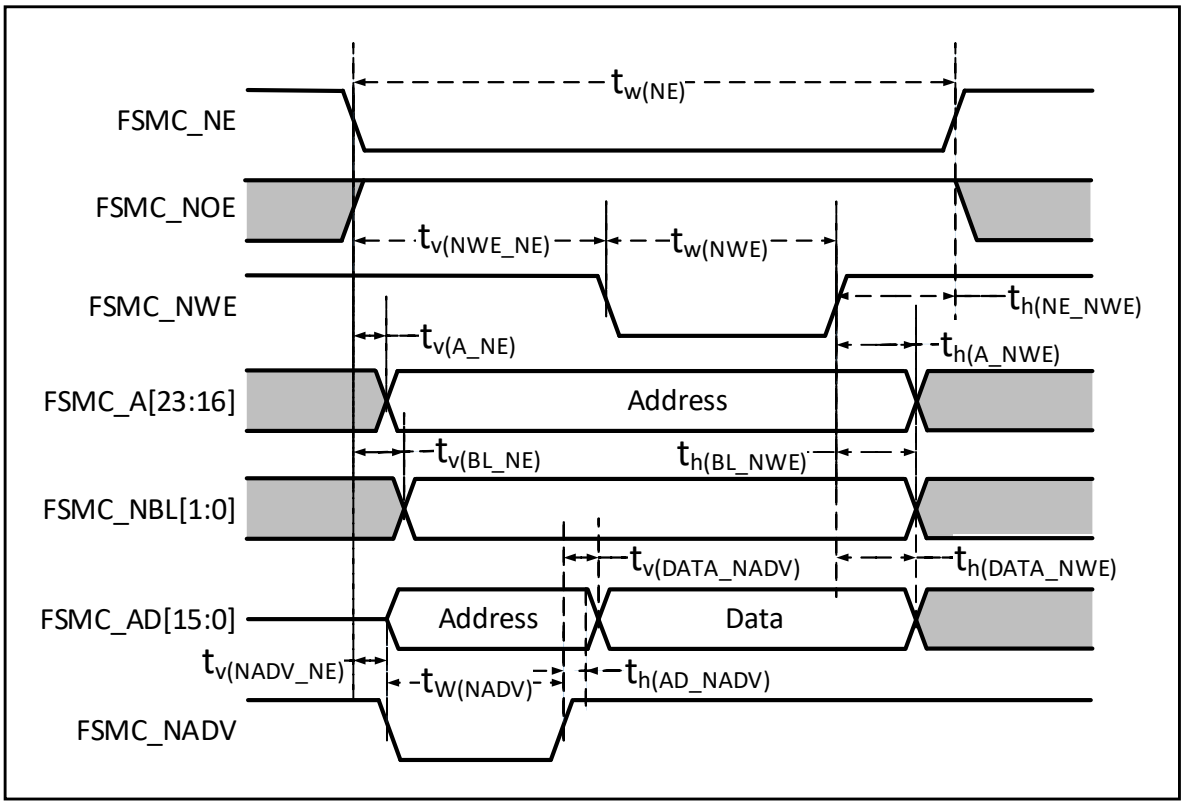



Table 4-32 PARAM/NOR write operation timing of asynchronous bus multiplexing

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(NE)}$ | FSMC_NE low time | $5t_{HCLK}$ | | ns |
| $t_{V(NEW\_NE)}$ | FSMC_NE low to FSMC_NWE low | $3t_{HCLK}$ | | |
| $t_{W(NWE)}$ | FSMC_NWE low time | $2t_{HCLK}$ | | |
| $t_{h(NE\_NWE)}$ | FSMC_NWE up to FSMC_NE high hold time | $t_{HCLK}$ | | |
| $t_{V(A\_NE)}$ | FSMC_NE as low as FSMC_A valid | 0 | 5 | |
| $t_{V(NADV\_NE)}$ | FSMC_NE as low as FSMC_NADV | 0 | 5 | |
| $t_{W(NADV)}$ | FSMC_NADV low time | $t_{HCLK}$ | | |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV is high | $2t_{HCLK}$ | | |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | $t_{HCLK}$ | | |
| $t_{V(BL\_NE)}$ | FSMC_NE as low as FSMC_BL valid | 0 | 5 | |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE is high | $t_{HCLK}$ | | |
| $t_{V(DATA\_NADV)}$ | FSMC_NADV up to data hold time | $2t_{HCLK}$ | | |
| $t_{h(DATA\_NWE)}$ | Data retention time after FSMC_NWE high | $t_{HCLK}$ | | |

Figure 4-18 Synchronous bus multiplexing NOR/PARAM read waveform

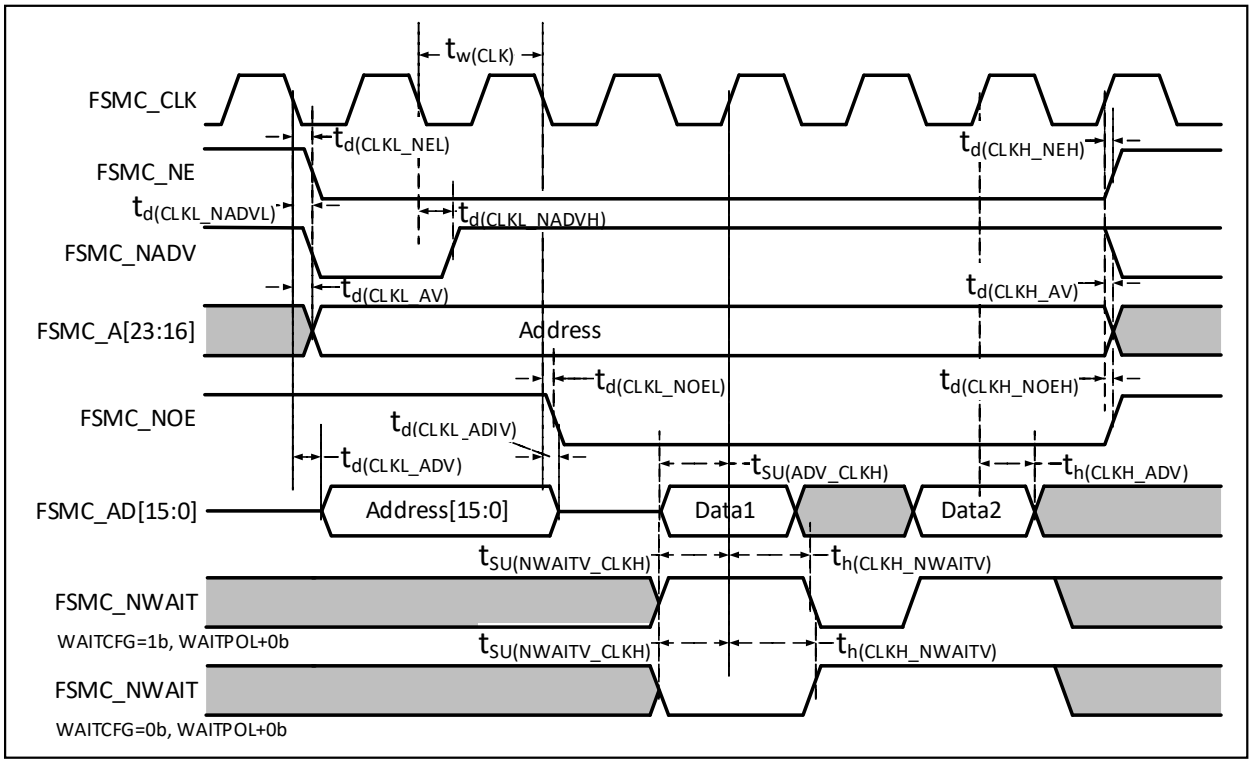



Table 4-33 Synchronous bus multiplexing NOR/PSRAM read timing

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(CLK)}$ | FSMC_CLK period | $2t_{HCLK}$ | | ns |
| $t_{d(CLKL\_NEL)}$ | FSMC_CLK as low as FSMC_NE | 0 | 5 | |
| $t_{d(CLKH\_NEH)}$ | FSMC_CLK is as high as FSMC_NE | $0.5t_{HCLK}$ | $0.5t_{HCLK}$ | |
| $t_{d(CLKL\_NADVL)}$ | FSMC_CLK as low as FSMC_NADV as low | 0 | 5 | |
| $t_{d(CLKL\_NADVH)}$ | FSMC_CLK as low as FSMC_NADV as high | 0 | 5 | |
| $t_{d(CLKL\_AV)}$ | FSMC_CLK is as low as FSMC_Ax valid (x = 16…23) | 0 | 5 | |
| $t_{d(CLKH\_AIV)}$ | FSMC_CLK as high as FSMC_Ax is invalid (x = 16…23) | 0 | 5 | |
| $t_{d(CLKL\_NOEL)}$ | FSMC_CLK as low as FSMC_NOE | $2t_{HCLK}$ | | |
| $t_{d(CLKH\_NOEH)}$ | FSMC_CLK as high as FSMC_NOE | $t_{HCLK}$ | | |
| $t_{d(CLKL\_ADV)}$ | FSMC_CLK as low as FSMC_AD[15:0] is valid | 0 | 5 | |
| $t_{d(CLKL\_ADIV)}$ | FSMC_CLK as low as FSMC_AD[15:0] is invalid | 0 | 5 | |
| $t_{SU(ADV\_CLKH)}$ | FSMC_AD[15:0] valid data before FSMC_CLK is high | 8 | | |
| $t_{h(CLKH\_ADV)}$ | FSMC_AD[15:0] valid data after FSMC_CLK is high | 8 | | |
| $t_{SU(NWAITV\_CLKH)}$ | FSMC_NWAIT is valid before FSMC_CLK is high | 6 | | |
| $t_{h(CLKH\_NWAITV)}$ | FSMC_NWAIT is valid after FSMC_CLK is high | 2 | | |

Figure 4-19 Synchronous bus multiplexing PSRAM write waveform

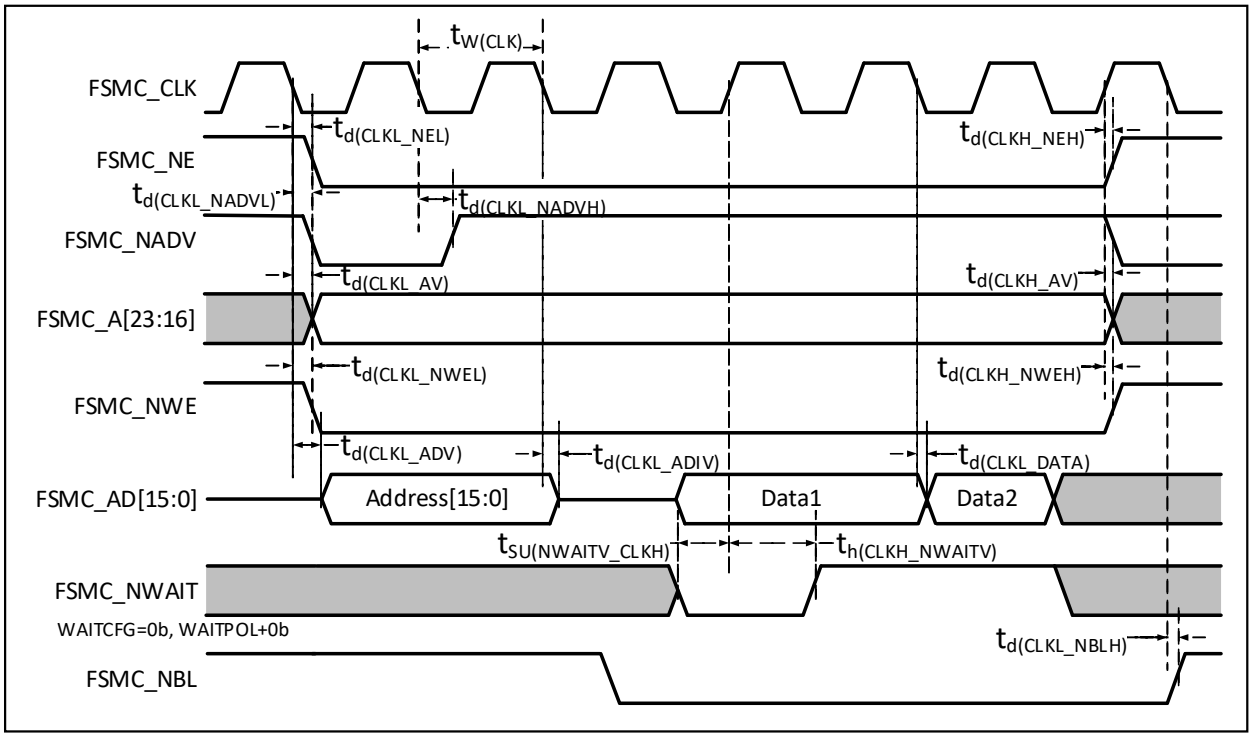



Table 4-34 Synchronous bus multiplexing PSRAM write timing

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(CLK)}$ | FSMC_CLK period | $2t_{HCLK}$ | | ns |
| $t_{d(CLKL\_NEL)}$ | FSMC_CLK as low as FSMC_NE | 0 | 5 | |
| $t_{d(CLKH\_NEH)}$ | FSMC_CLK is as high as FSMC_NE | $0.5t_{HCLK}$ | $0.5t_{HCLK}$ | |
| $t_{d(CLKL\_NADVL)}$ | FSMC_CLK as low as FSMC_NADV as low | 0 | 5 | |
| $t_{d(CLKL\_NADVH)}$ | FSMC_CLK as low as FSMC_NADV as high | 0 | 5 | |
| $t_{d(CLKL\_AV)}$ | FSMC_CLK is as low as FSMC_Ax valid (x = 16…23) | 0 | 5 | |
| $t_{d(CLKH\_AIV)}$ | FSMC_CLK as high as FSMC_Ax is invalid (x = 16…23) | 0 | 5 | |
| $t_{d(CLKL\_NWEL)}$ | FSMC_CLK as low as FSMC_NWE | 0 | | |
| $t_{d(CLKH\_NWEH)}$ | FSMC_CLK is as high as FSMC_NWE | 0 | | |
| $t_{d(CLKL\_ADV)}$ | FSMC_CLK as low as FSMC_AD[15:0] is valid | 0 | 5 | |
| $t_{d(CLKL\_ADIV)}$ | FSMC_CLK as low as FSMC_AD[15:0] is invalid | 0 | 5 | |
| $t_{d(CLKL\_DATA)}$ | FSMC_AD[15:0] is valid after FSMC_CLK is low | 2 | | |
| $t_{SU(NWAITV\_CLKH)}$ | FSMC_NWAIT is valid before FSMC_CLK is high | 6 | | |
| $t_{h(CLKH\_NWAITV)}$ | FSMC_NWAIT is valid after FSMC_CLK is high | 2 | | |
| $t_{d(CLKL\_NBLH)}$ | FSMC_CLK low to FSMC_NBL high | 2 | | |

NAND controller waveform and timing

Test conditions: NAND operation area, 16-bit data width is selected, ECC calculation circuit is enabled, 512-byte page size, other timing configurations are setting registers FSMC_PCR2=0x0002005E, FSMC_PMEM2=0x01020301, FSMC_PATT2=0x01020301.

Figure 4-20 NAND controller read operation waveform

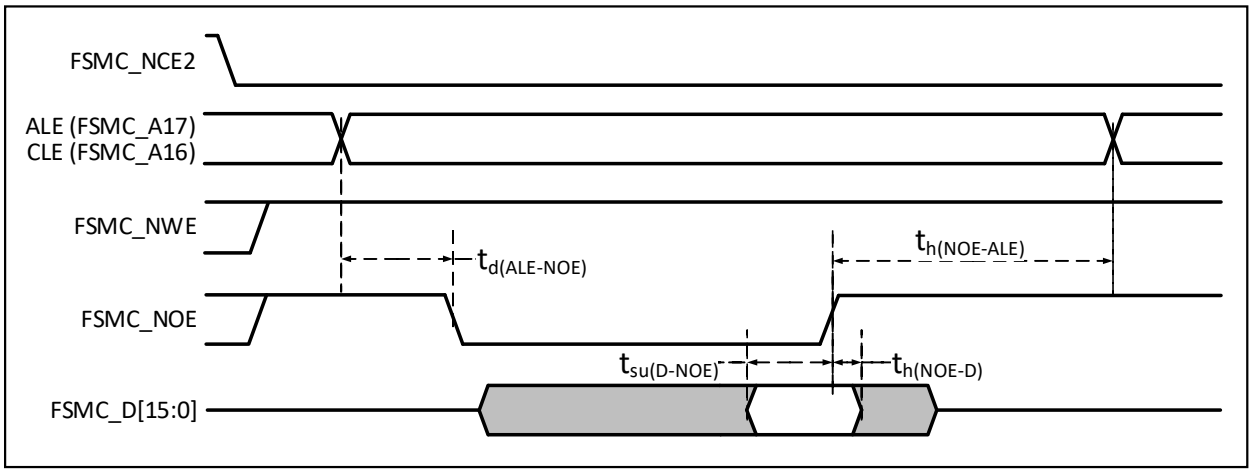



Figure 4-21 NAND controller write operation waveform

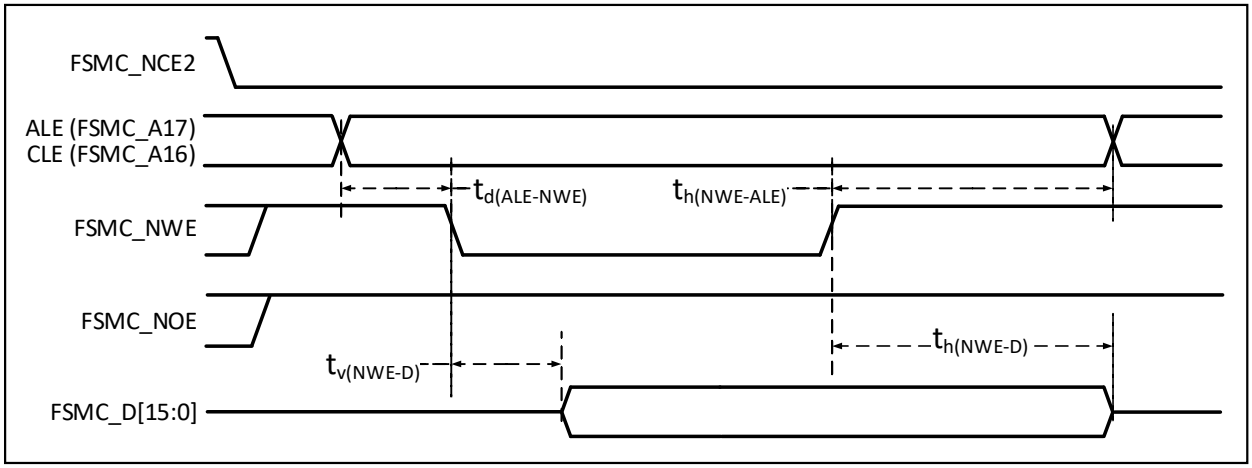



Figure 4-22 Read operation waveform of NAND controller in general storage space

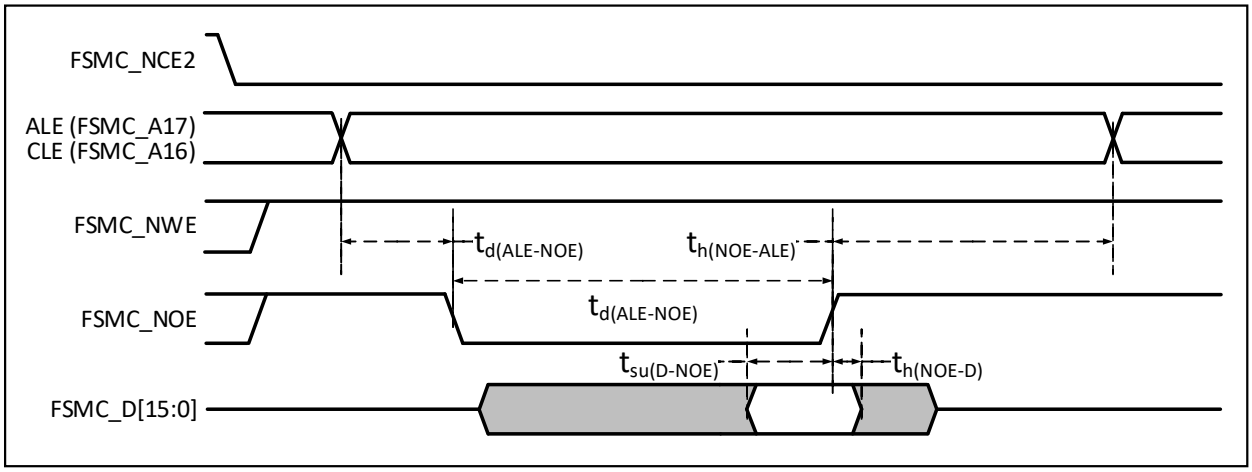


Figure 4-23 Write operation waveform of NAND controller in general storage space

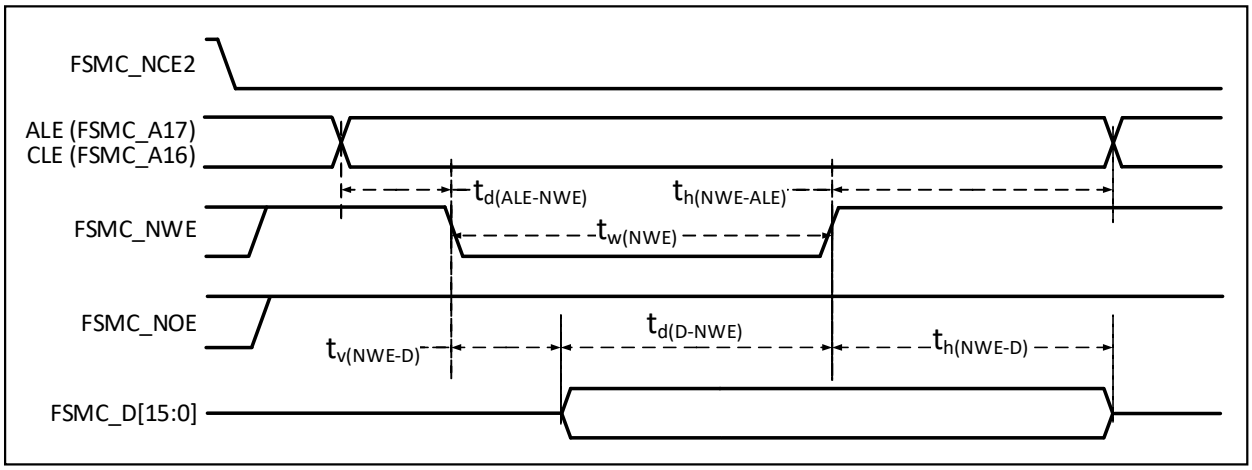



Table 4-35 Timing characteristics of NAND Flash read and write cycles

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{d(D-NWE)}$ | Before FSMC_NWE high to FSMC_D[15:0] data is valid | $4t_{HCLK}$ | | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $4t_{HCLK}$ | | |
| $t_{su(D-NOE)}$ | Before FSMC_NOE is high until FSMC_D[15:0] data is valid | 20 | | |
| $t_{h(NOE-D)}$ | After FSMC_NOE is high, the data is valid until FSMC_D[15:0] | 15 | | |
| $t_{w(NWE)}$ | FSMC_NWE low time | $4t_{HCLK}$ | | |
| $t_{v(NWE-D)}$ | FSMC_NWE as low as FSMC_D[15:0] data is valid | 0 | | |
| $t_{h(NWE-D)}$ | FSMC_NWE is as high as FSMC_D[15:0] The data is invalid | $2t_{HCLK}$ | | |
| $t_{d(ALE-NWE)}$ | Before FSMC_NWE is low until FSMC_ALE is valid | $2t_{HCLK}$ | | |
| $t_{h(NWE-ALE)}$ | FSMC_NWE as high as FSMC_ALE is invalid | $2t_{HCLK}$ | | |
| $t_{d(ALE-NOE)}$ | Before FSMC_NOE is low until FSMC_ALE is valid | $2t_{HCLK}$ | | |
| $t_{h(NOE-ALE)}$ | FSMC_NOE as high as FSMC_ALE is invalid | $4t_{HCLK}$ | | |

### 4.3.19 DVP Interface characteristics

Figure 4-24 DVP timing waveform

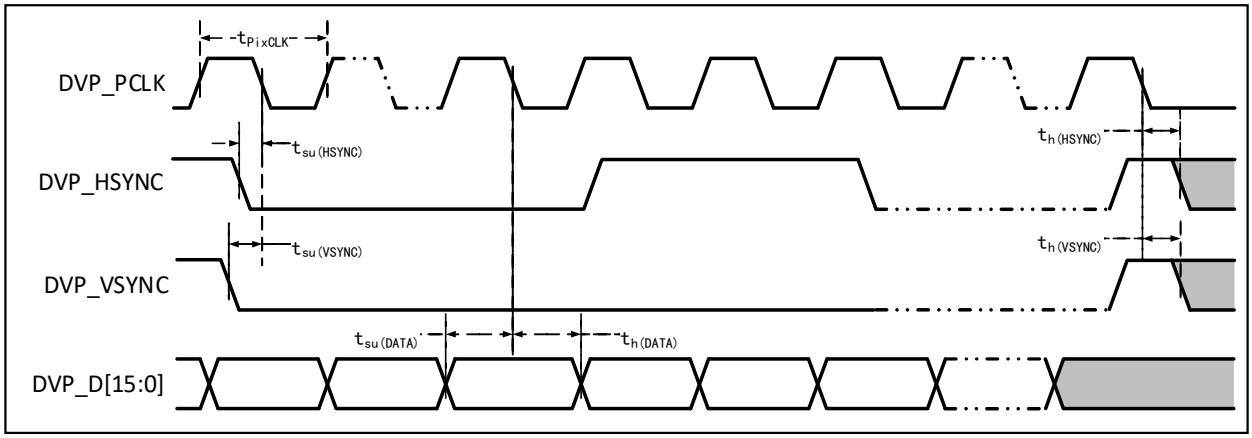



Table 4-36 DVP interface characteristics

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| $f_{PixCLK}/t_{PixCLK}$ | Pixel clock input frequency | | 144 | MHz |
| $DuCy_{(PixCLK)}$ | Pixel clock duty cycle | 15 | | % |
| $t_{su(DATA)}$ | Data establishment time | 2 | | ns |
| $t_{h(DATA)}$ | Data retention time | 1 | | |
| $t_{su(HSYNC)}/t_{su(VSYNC)}$ | HSYNC/VSYNC signal input setup time | 2 | | |
| $t_{h(HSYNC)}/t_{h(VSYNC)}$ | HSYNC/VSYNC signal input hold time | 1 | | |

### 4.3.20 Gigabit Ethernet interface features

Figure 4-25 ETH-SMI timing waveform

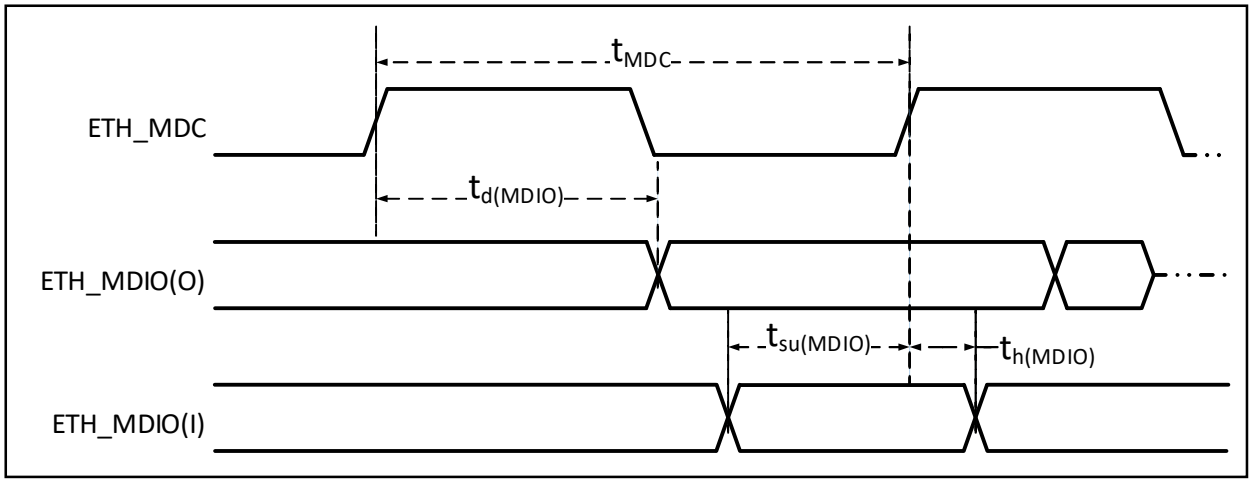



Table 4-37 SMI signal characteristics of Ethernet MAC

| Symbol | Parameter | Min | Max | Unit | Symbol |
|---|---|---|---|---|---|
| $f_{MDC}/t_{MDC}$ | MDC clock frequency | | | 12 | MHz |
| $t_{d(MDIO)}$ | MDIO write data valid time | 0 | | 300 | ns |
| $t_{su(MDIO)}$ | Read data establishment time | 10 | | | |
| $t_{h(MDIO)}$ | Read data retention time | 10 | | | |

Figure 4-26 ETH-RMII signal timing waveform

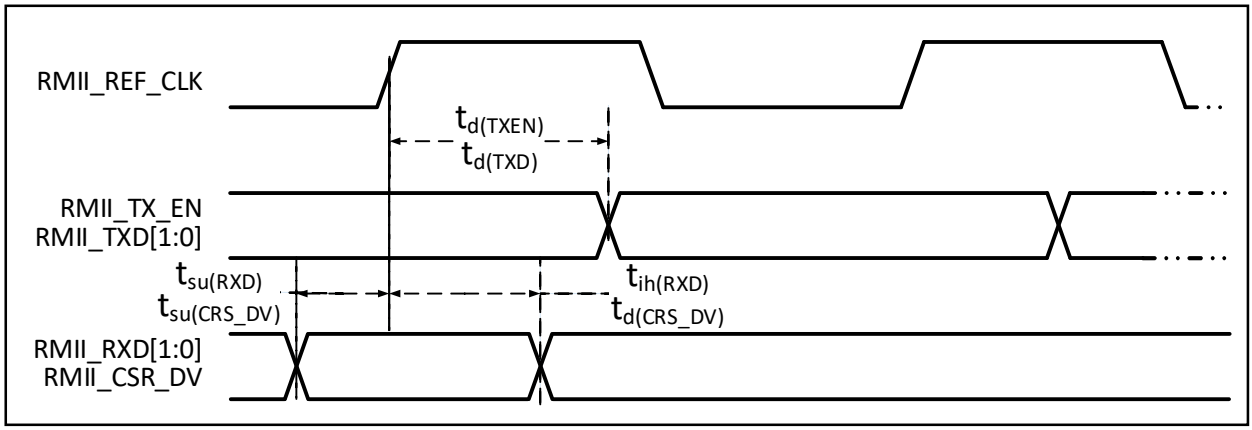



Table 4-38 RMII signal characteristics of Ethernet MAC

| Symbol | Parameter | Min | Max | Unit | Symbol |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Setup time of received data | 4 | | | ns |
| $t_{ih(RXD)}$ | Hold time of received data | 2 | | | |
| $t_{su(CRS\_DV)}$ | Carrier detect signal establishment time | 4 | | | |
| $t_{ih(CRS\_DV)}$ | Carrier detect signal hold time | 2 | | | |
| $t_{d(TXEN)}$ | Transmission enable effective delay time | 11 | 13 | 16 | |
| $t_{d(TXD)}$ | Data transmission effective delay time | 11 | 13 | 16 | |

Figure 4-27 ETH-MII signal timing waveform

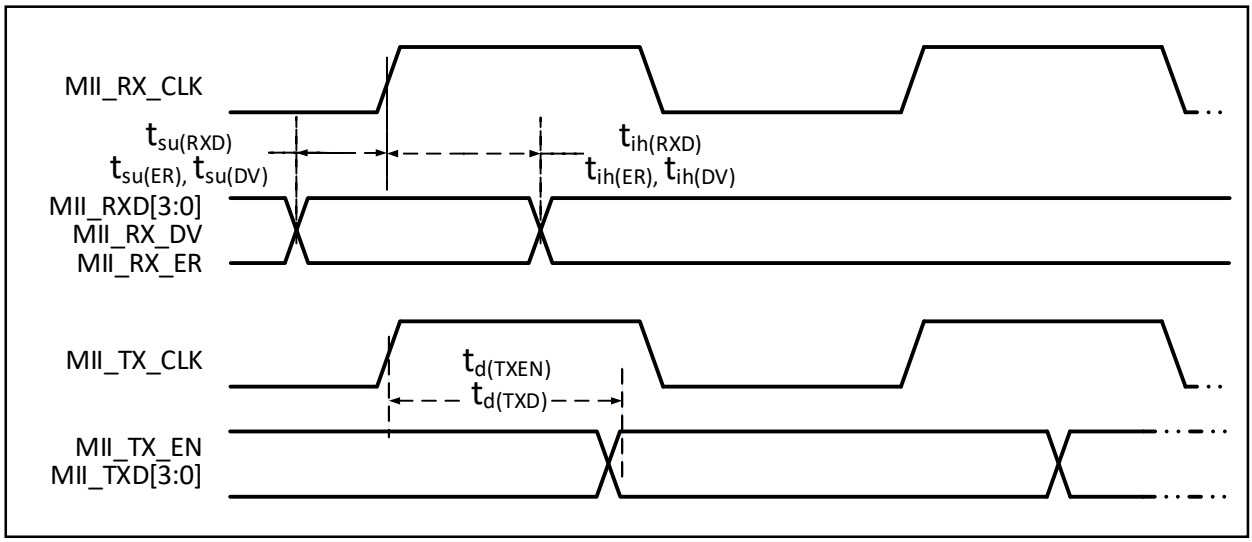



Table 4-39 MII signal characteristics of Ethernet MAC

| Symbol | Parameter | Min | Max | Unit | Symbol |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Setup time of received data | 10 | | | ns |
| $t_{ih(RXD)}$ | Hold time of received data | 10 | | | |
| $t_{su(DV)}$ | Data valid signal establishment time | 10 | | | |
| $t_{ih(DV)}$ | Data valid signal hold time | 10 | | | |
| $t_{su(ER)}$ | Error signal establishment time | 10 | | | |
| $t_{ih(ER)}$ | Error signal hold time | 10 | | | |
| $t_{d(TXEN)}$ | Transmission enable effective delay time | 11 | 13 | 16 | |
| $t_{d(TXD)}$ | Data transmission effective delay time | 11 | 13 | 16 | |

Figure 4-28 ETH-RGMII signal timing waveform

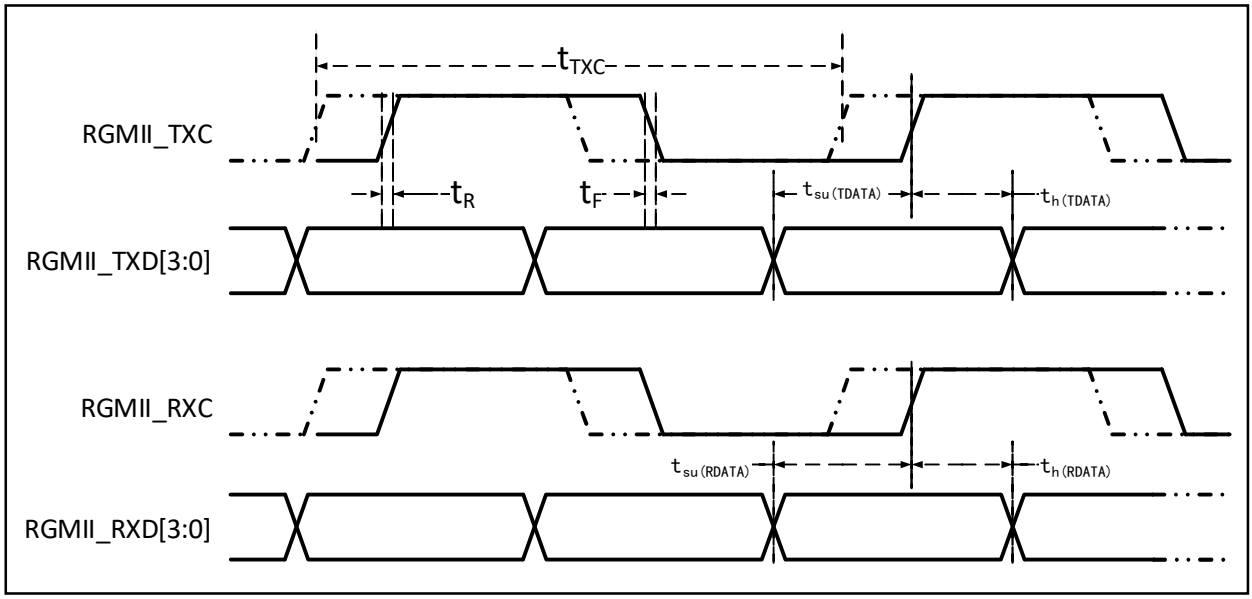



Table 4-40 RGMII signal characteristics of Ethernet MAC

| Symbol | Parameter and description | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|
| $f_{TXC}/t_{TXC}$ | TXC/RXC clock frequency | 7.2 | 8 | 8.8 | ns |
| $t_R$ | TXC/RXC rise time | | | 2.0 | |
| $t_F$ | TXC/RXC fall time | | | 2.0 | |
| $t_{su(TDATA)}$ | Time to send data establishment | 1.2 | 2.0 | | |
| $t_{h(TDATA)}$ | Send data hold time | 1.2 | 2.0 | | |
| $t_{su(RDATA)}$ | Input data creation time | 1.2 | 2.0 | | |
| $t_{h(RDATA)}$ | Input data retention time | 1.2 | 2.0 | | |

### 4.3.21 12- bit ADC characteristics

Table 4-41 ADC characteristics

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 2.4 | | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 2.4 | | $V_{DDA}$ | V |
| $I_{VREF}$ | | | | 160 | 220 | uA |
| $I_{DDA}$ | | | | 480 | 530 | uA |
| $f_{ADC}$ | ADC clock frequency | | | | 14 | MHz |
| $f_S$ | Sampling rate | | 0.05 | | 1 | MHz |
| $f_{TRIG}$ | External trigger frequency | $f_{ADC}$ = 14MHz | | | 875 | KHz |
| | | | | | 16 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | | 0 | | $V_{REF+}$ | V |
| $R_{AIN}$ | External input impedance | | | | 50 | KΩ |
| $R_{ADC}$ | Sampling switch resistance | | | 0.6 | 1 | KΩ |
| $C_{ADC}$ | Internal sample and hold | | | 8 | | pF |

| | | | | | | |
|---|---|---|---|---|---|---|
| | capacitor | | | | | |
| $t_{CAL}$ | Calibration time | $f_{ADC}$ = 14MHz | | | 0.143 | us |
| | | | | | | $1/f_{ADC}$ |
| $t_{Iat}$ | Injection trigger conversion delay | $f_{ADC}$ = 14MHz | | | | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_{Iatr}$ | Conventional trigger conversion delay | $f_{ADC}$ = 14MHz | | | 0.143 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_s$ | Sampling time | $f_{ADC}$ = 14MHz | 0.107 | | 17.1 | us |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-on time | | | | 1 | us |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 14MHz | 1 | | 18 | us |
| | | | 14 | | 252 | $1/f_{ADC}$ |

Formula: Maximum $R_{AIN}$

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-42 Maximum RAIN when fADC = 14MHz

| $T_S$ (cycle) | $t_S$ (us) | Max $R_{AIN}$(KΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | Invalid |
| 239.5 | 17.1 | Invalid |

Table 4-43 ADC error

| Symbol | Parameter | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| EO | Offset error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 3.3V | | ±2 | | LSB |
| ED | Differential nonlinearity error | | | ±0.5 | ±3 | |
| EL | Integral nonlinearity error | | | ±1 | ±4 | |

$C_p$ represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger $C_p$ value will reduce the conversion accuracy, the solution is to reduce the $f_{ADC}$ value.

Figure 4-29 ADC typical connection diagram

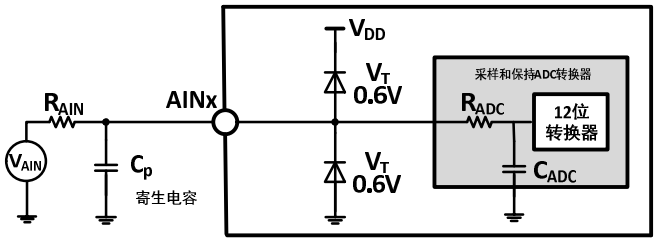
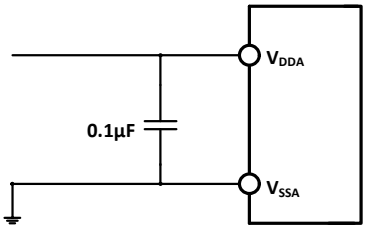



Figure 4-30 Analog power supply and decoupling circuit reference




### 4.3.22 Temperature sensor characteristics

Table 4-44 Temperature sensor characteristics

| Symbol | Parameters | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| Avg_Slope | Average slope | | | 4.3 | | mV/℃ |
| $V_{25}$ | Voltage at 25℃ | | 1.34 | 1.43 | 1.52 | V |
| $T_{S\_temp}$ | When reading temperature, ADC sampling time | $f_{ADC}$ = 14MHz | | | 17.1 | us |

### 4.3.23 DAC characteristics

Table 4-45 DAC characteristics

| Symbol | Parameters | Condition | Min | Typical value | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 2.4 | 3.3 | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | $V_{REF+}$ must be lower than $V_{DDA}$ | 2.4 | 3.3 | 3.6 | V |
| $R_L$ | Load resistance when the buffer is open | | 5 | | | kΩ |
| $C_L$ | Load capacitance when the buffer is turned on | | | | 50 | pF |
| $V_{OUT\_MIN}$ | When the buffer is turned on, the 12-bit DAC converts | | 3 | | | mV |
| $V_{OUT\_MAX}$ | | | | | $V_{REF+}$-0.01 | V |
| $V_{OUT\_MIN}$ | 12-bit DAC conversion when the buffer is off | | | 0 | | mV |
| $V_{OUT\_MAX}$ | | | | | $V_{REF+}$-0.02 | V |
| $I_{VREF+}$ | No load | | | 60 | | uA |
| | No load, when $V_{REF+}$=3.6V, the input value is 0xF1C | | | 202 | | |
| $I_{DDA}$ | No load, input value 0x800 | | | 211 | | uA |
| | No load, when $V_{REF+}$=3.6V, the input value is 0xF1C | | | 193 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| DNL | Differential nonlinearity error | | | ±1 | | LSB |
| INL | ntegral nonlinearity error | | | ±4 | | LSB |
| Offset | Offset error (the difference between the value measured at code 0x800 and the ideal value $V_{REF+}$/2 deviation) | | | ±8 | | mV |
| | | $V_{REF+}$=3.6V | | ±10 | | LSB |
| Gain error | | DAC is configured as 12 bits | | ±0.1 | | % |
| Amplifier gain | Amplifier gain in open loop | 5kΩ load (max) | 80 | 85 | | dB |
| $t_{SETTLING}$ | The gain setting time of the amplifier in open loop (full range: 10-bit input code changes from minimum to maximum, DAC_OUT reaches ±1 LSB of its final value) | $C_{LOAD}$≤50pF<br>$R_{LOAD}$≥5kΩ | | | | us |
| 更新速率 | When the input code has a small change (from the value i to i+1LSB), the maximum frequency of the correct DAC_OUT is obtained | $C_{LOAD}$≤50pF<br>$R_{LOAD}$≥5kΩ | | | | MS/s |
| $t_{WAKEUP}$ | Time to wake up from off state(PDV18 changes from 1 to 0) | $C_{LOAD}$≤50pF，$R_{LOAD}$≥5kΩ, the input code is between the minimum and maximum possible values | | | | us |
| PSRR+ | Power supply rejection ratio (relative to VDDA) (static DC measurement) | No $R_{LOAD}$, $C_{LOAD}$≤50pF | | -100 | -75 | dB |

# Chapter 5 Package and Ordering Information

## Chip package

| Package | Body width | Pin pitch | | Package description | Order model |
|---|---|---|---|---|---|
| LQFP48 | 7*7mm | 0.5mm | 19.7mil | LQFP48（7*7）patch | CH32V203C6T6 |
| LQFP32 | 7*7mm | 0.5mm | 19.7mil | LQFP48（7*7）patch | CH32V203K8T6 |
| LQFP48 | 7*7mm | 0.5mm | 19.7mil | LQFP48（7*7）patch | CH32V203C8T6 |
| QFN48X7 | 7*7mm | 0.5mm | 19.7mil | Square without lead 48-pin | CH32V203C8U6 |
| LQFP48 | 7*7mm | 0.5mm | 19.7mil | LQFP48（7*7）patch | CH32V303CBT6 |
| LQFP64M | 10*10mm | 0.5mm | 19.7mil | LQFP64M（10*10）patch | CH32V303RBT6 |
| LQFP64M | 10*10mm | 0.5mm | 19.7mil | LQFP64M（10*10）patch | CH32V303RCT6 |
| LQFP100 | 14*14mm | 0.5mm | 19.7mil | LQFP100（14*14）patch | CH32V303VCT6 |
| LQFP64M | 10*10mm | 0.5mm | 19.7mil | LQFP64M（10*10）patch | CH32V305RBT6 |
| LQFP64M | 10*10mm | 0.5mm | 19.7mil | LQFP64M（10*10）patch | CH32V307RCT6 |
| LQFP100 | 14*14mm | 0.5mm | 19.7mil | LQFP100（14*14）patch | CH32V307VCT6 |
| QFN48X5 | 5*5mm | 0.35mm | 13.8mil | Square without lead 48-pin | CH32V208CBU6 |
| LQFP64M | 10*10mm | 0.5mm | 19.7mil | LQFP64M（10*10）patch | CH32V208RBT6 |
| QFN68X8 | 8*8mm | 0.4mm | 15.75mil | Square without lead 68-pin | CH32V208WBU6 |

Note: The unit of dimensioning is mm (millimeters), the pin center spacing is always the nominal value, there is no error, and the other dimension error is not more than ±0.4mm or 15%.

Figure 5-1 QFN48X5 package

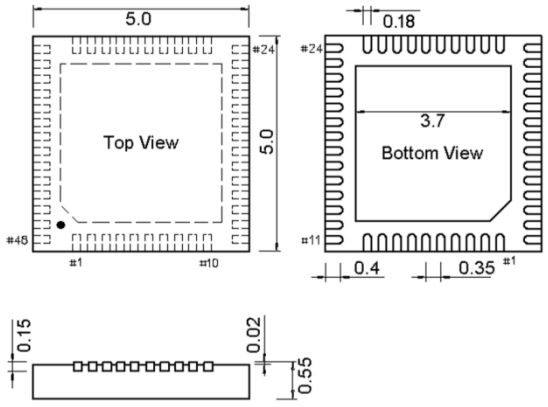


Figure 5-2 QFN48X7 package

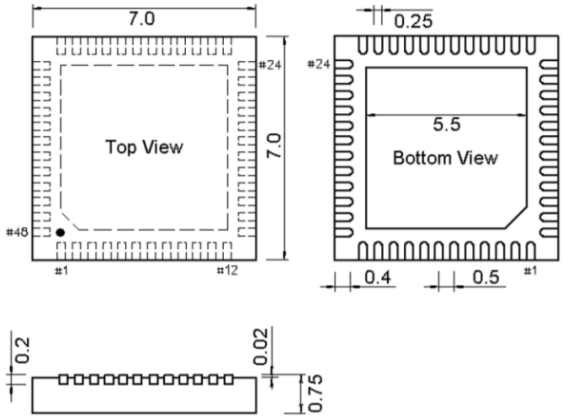



Figure 5-3 QFN68X8 package

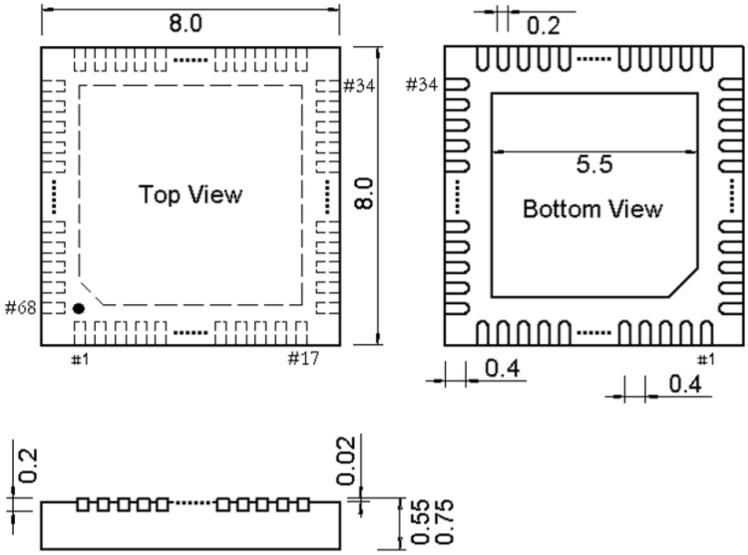



Figure 5-4 LQFP32 package

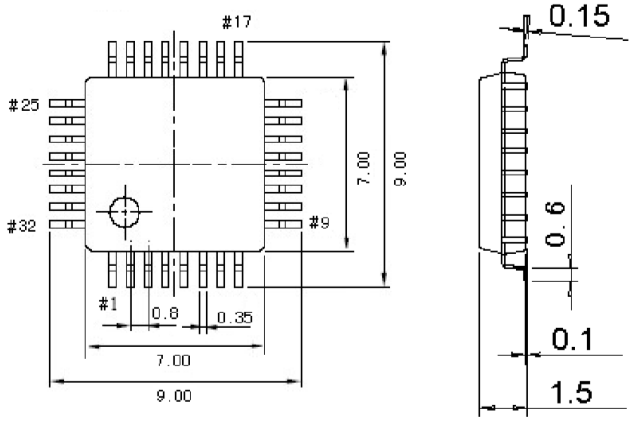


Figure 5-5 LQFP48 package

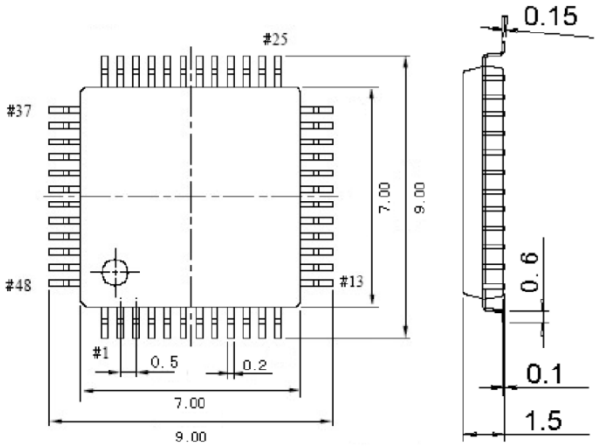



Figure 5-6 LQFP64M package

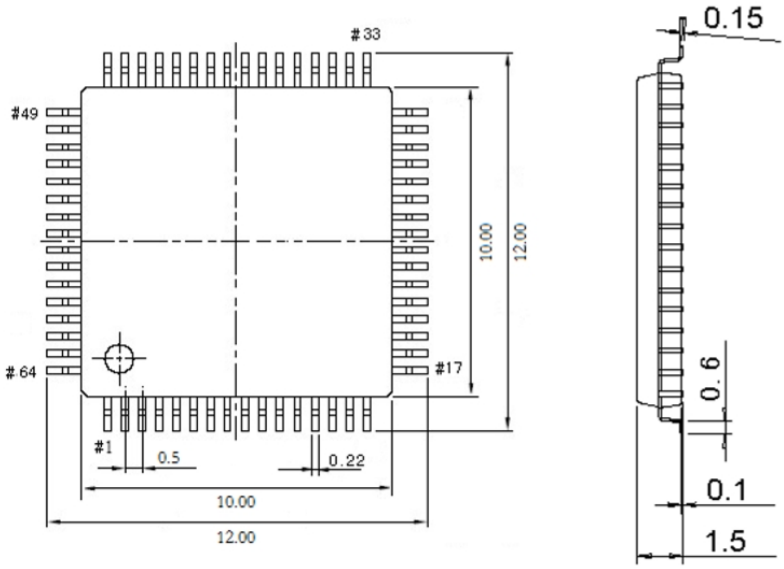
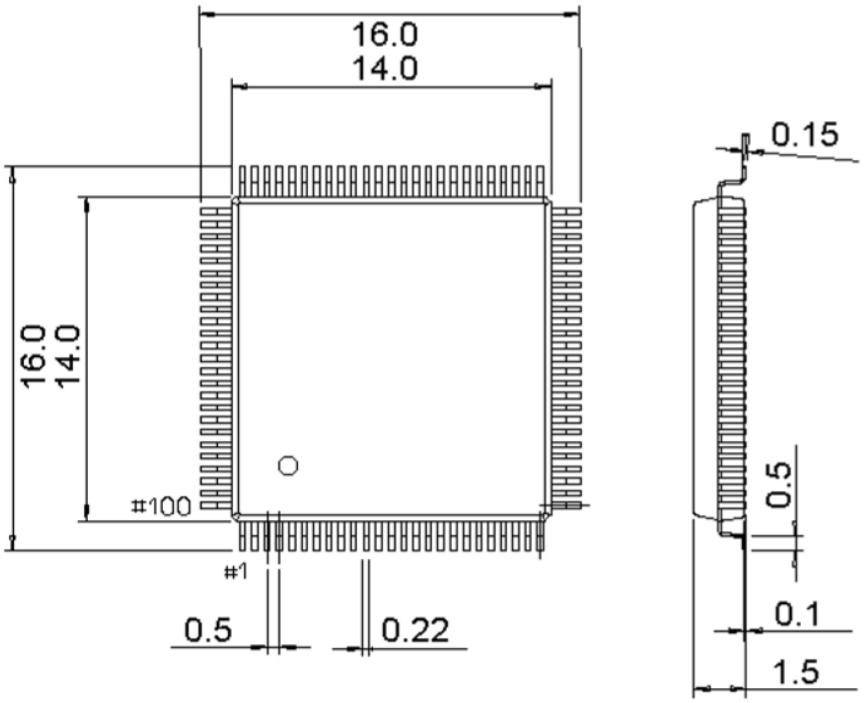


Figure 5-7 LQFP100 package



# Series Naming Rules

For example: CH32 F 1 03 R 8 T 6

Series

F = Based on ARM ISA

V = Based on RISC-V ISA

Type

0 = V2 core

1 = M3/V3A core, clock speed @72M

2 = M3/V4B core, clock speed @144M

3 = V4F floating-point core, clock speed @144M

Sub-series

30 = Cost-effective type

03 = General type

05 = Connection type (USB high speed, SDIO, dual CAN)

07 = Interconnection type (USB high speed, dual CAN, Ethernet, DVP, SDIO, FSMC)

08 = Wireless type (Bluetooth BLE5.1, CAN, USB, Ethernet)

Number of pins

G= 28 pins K = 32 pins

T = 36 pins C = 48 pins

R = 64 pins W = 68 pins

V = 100 pins Z = 144 pins

Flash capacity

6 = 32K flash

8 = 64K flash

B = 128K flash

C = 256K flash

Package

T = LQFP

U = QFN

Temperature range

5 = Commercial-grade, 0℃-70℃

6 = Industrial-grade, -40℃-85℃

3 = Automotive-grade, -40℃-125℃

0 = Wide-temperature-grade, -55℃-125℃