Adjusting Signal Timing (Part 1)

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ABSTRACT

It is becoming a routine requirement for PCB designers to tune traces on boards. Such tuning can be relative (i.e. traces are equal length) or absolute (i.e. traces must be a proscribed length.) This article, Part 1 of a two-part series, addresses why traces need to be tuned at all, how to determine signal propagation speeds and times so that proper trace length can be determined, and how sensitive propagation time (and therefore tuning) is to factors such as $\mathcal{E}_r$, trace length, trace pattern, etc. The special case of differential traces is mentioned, and some examples of tuning on a high-speed computer motherboard are illustrated.

It is a fairly routine requirement, now, for PCB designers to need to adjust trace lengths in order to meet a signal timing objective. We call that "tuning." Part 1 will explore several aspects of this requirement:

- Why do we need to tune traces at all?
- How do we tune traces?
- How much trace length do we need to add?
- How closely can we tune them (that is, what are the error sources and the sensitivities to those sources)?
- Is there any sensitivity to the trace patterns used?
- How do we handle vias?

In Part 2 of this series I will look specifically at the issue of crosstalk when traces are "tromboned" in order to add length.

WHY DO WE NEED TO TUNE TRACES?

In digital circuits, everything happens in discrete increments of time. These increments are typically controlled by the digital clock. Every time the clock "ticks," instructions are executed and the results of these instructions then wait for the next clock "tick." The clock ticks must be spaced far enough in time for each execution to be completed, and the results of each instruction must be ready and "waiting" for the next instruction to begin. If the clock ticks too fast, or if the results of a prior instruction don't arrive at the next point of the circuit in time, digital signal errors will occur.

When referring to **Figure 1**, think of Driver A as being a clock driver. It is sending its signal to devices B1 and B2. If the clock signal arrives too early, processing errors may occur. In this illustration, the distance between A and B2 is acceptable, but B1 is too close (**Figure 1(a)**). In order to keep things in synch, we add length to the trace between A and B1 (**Figure 1(b)**) so that the clock signal takes longer to reach B1. In **Figure 1(b)** the clock signal arrives at B1 and B2 at the same time.

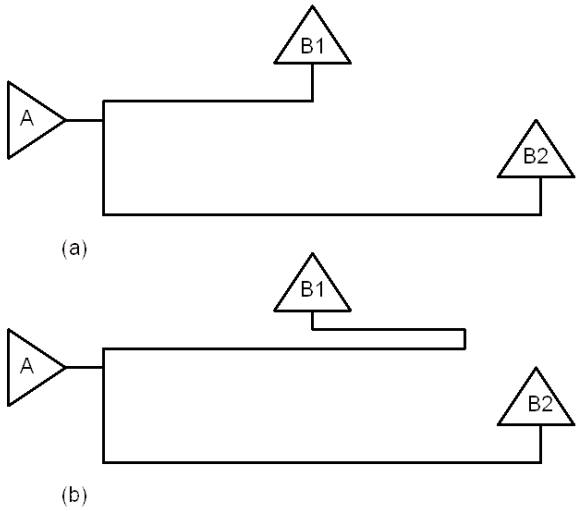


Figure 1: If the signal from driver A is to arrive at B1 and B2 at the same time, additional length must be added between A and B1.

This is simply one of many examples of where traces need to be adjusted to match trace lengths. An excellent second example is the case of "probe cards" (see **Figure 2**). Probe cards are typically used to test individual circuits, often at the semiconductor wafer level. It would not be unusual for there to be over 100 individual probes on the probe card.

One of the important things to be measured on the chip under test might be whether all the signals are propagating though the chip at the correct speed, and therefore showing up at the probe points at the correct point in time. The probe card is connected to a piece of test equipment. If the propagation time across the probe card is different for different signals, how does the test equipment know if the signal timing differences are caused by the chip under test or by the probe card itself? It is, of course, possible to calibrate the probe card, but it is often preferable to make all the traces on the probe card exactly the same length (so that the propagation time for each trace is exactly the same) so that no calibration is necessary.

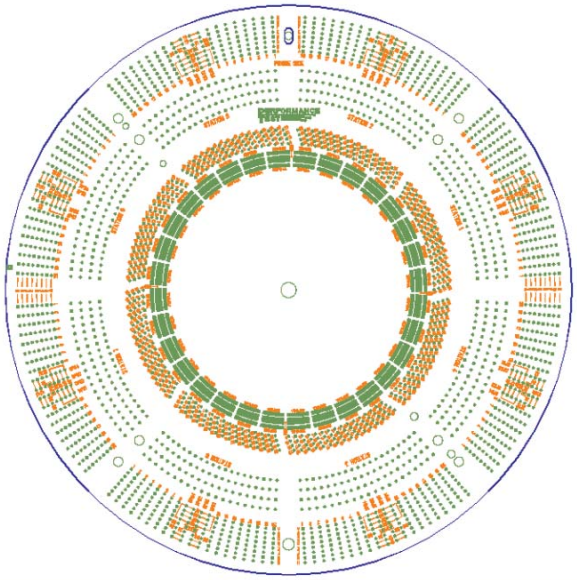


Figure 2: Typical probe card

There are numerous other examples where the tuning of signal or clock traces might be required. We might have a number of traces (a signal bus) containing related signals through a circuit. These signals must all "line up" at the end at exactly the same time. We at UltraCAD once had a board where 16 different signal buses, each with 16 individual traces, traveled approximately 14 inches across a board. The signals on all 256 traces had to arrive at the output of the board at exactly the same time. In other cases there may be some uncertainty regarding when a signal will arrive at a device, or how long it might take the signal to "settle down" so that its level (a digital "one" or "zero") may be read correctly. The clock signal may have to be delayed in order to provide the necessary cushion for this to happen.

HOW ARE TRACES TUNED?

It is not often we have the luxury to shorten traces. Usually we have routed our traces about as short as practical. Therefore, the tuning mechanism that is usually available to us is to selectively lengthen traces. **Appendix 1** includes views of a computer motherboard where the tuning of single ended and differential pairs is evident.

HOW MUCH LENGTH DO WE ADD?

Tuning requirements are usually either relative or absolute. By relative, I mean we may have a requirement that "all traces must be the same length." This is a relatively[1] easy requirement to accomplish. We determine the minimum length required for the "worst case" trace (the one where the minimum trace length will be the longest) and then add length to all the other traces so that they come up to the same length. The only calculation required is the length of the trace itself.

But often the requirement is an absolute one. The circuit design engineer may have stated something like "There must be 865 ps delay between these two devices on this trace." Determining this requirement is not the responsibility of the board designer; it is the responsibility of the circuit design engineer. But it is the board designer's responsibility to implement this requirement. Implementing this requirement not only requires using the correct trace length, it also requires (first) knowing how fast the signal will propagate along the trace in the first place. The correct trace length cannot be determined until we know how far a signal can travel (along a trace) in 865 ps.

The fundamental starting point for this type of calculation is the speed of light, 186,280 miles per second. This is the speed of light in the air[2], and therefore the speed of an electronic signal along a wire in the air. In terms more meaningful to us as board designers, this is:

$$Speed = \frac{186,280\ miles}{Sec} * \frac{5,280\ feet}{mile} * \frac{12\ inch}{foot} * \frac{1000\ mils}{inch} * \frac{10^{-12}\ \text{sec}}{ps} = 11.8\ mils/ps \quad \text{Eq. 1}$$

or:

$$\text{Propagation time} = 1/\text{speed} = .0847\ ps/mil \quad [\text{Eq. 2}]$$

So, the requirement for an 865 ps delay in the air would mean a wire slightly longer than ten inches (10.2 in would be closer).

But this calculation yields the speed (or the propagation time) for a signal in the air. Signals slow down when they travel in any other environment.[3] If the environment is homogeneous (the same everywhere around the wire or trace), then the speed and propagation times are given by this relationship:

$$Speed = \frac{11.8}{\sqrt{\varepsilon_r}} mils / ps \qquad [Eq\ 3]$$

and:

$$Propagation time = .0847 * \sqrt{\varepsilon_r}\ ps / mil \qquad [Eq\ 4]$$

where $\mathcal{E}_r$ is the relative dielectric coefficient of the material surrounding the wire or trace. The minimum value for the relative dielectric coefficient is 1.0 (the value for air). It is larger than 1.0 for every other material. In particular, the relative dielectric coefficient for FR4, the material commonly used for circuit board is approximately 4.0. The square root of 4 is 2, so the speed of a signal on our boards is approximately half that of a signal in the air.

To relate this to the example above, if we want our trace to be 865 ps long in FR4 with an $\mathcal{E}_r$ of 4.0, then the propagation time would be:

$$Propagation time = .0847 * \sqrt{4} = .0847 * 2 = .1694\ ps / mils \qquad [Eq\ 5]$$

Our trace, then, would have to be 865/.1694 = 5106 mils long (5.1 inches).

These calculations work very well when the trace is in a homogeneous environment. And that is usually the case when we are dealing with traces in a stripline environment. Microstrip traces, however, are not in a homogeneous environment. Microstrip traces have one material underneath the trace (between the trace and the underlying plane), and another environment (typically air) above the trace. But they may also have conformal coating and solder mask (and maybe other materials) near or over the trace, with uncontrolled thicknesses. So the effective $\mathcal{E}_r$ for microstrip traces can be very difficult to determine.

In addition, even if the materials are known, it has been shown that the propagation time along a microstrip trace is also dependent on the width of the trace and the distance between the trace and the plane. A good estimate for the propagation time of a microstrip trace is to take the propagation time for the same trace in a stripline environment (surrounded by the dielectric) and multiply it by a factor: [4]

$$Propagation time (microstrip) = factor * .0847 * \sqrt{\varepsilon_r}\ ps / mils \qquad [Eq\ 6]$$

where:

Factor = 0.8566 + 0.0294*Ln(W) - 0.00239*H - 0.0101* $\mathcal{E}_r$

and where:

W = Trace Width (mils)

H = Trace Height above the reference plane (mils)

Ln = natural logarithm

Consequently, if we must tune traces with precision, this can be difficult to accomplish in microstrip environments. There are simply too many variables that are difficult to control. So, if traces must be tuned to precision, a good rule is to keep those traces in a stripline environment where the environment can be controlled more tightly.

SOURCES OF ERRORS

It is one thing to calculate the propagation time for traces on our boards and to know how much trace length to add. It is another thing to know how sensitive our calculations are to various possible sources of error. People tend to be concerned with seven possible sources of error:

1. Sensitivity to length
2. Sensitivity to line width
3. Sensitivity to $\mathcal{E}_r$
4. Via lengths

And when traces loop back closely to themselves (an effect we call "tromboning"):

5. Sensitivity to signal path within the trace
6. Impact of differential impedance
7. Impact of crosstalk

Length: We have shown (Equation 5) that the propagation time (in stripline with FR4 where $\mathcal{E}_r$ = 4) is .1694 ps/mil. That means, if we wish to control the time to within 1.0 ps, we need to control the trace length to within about 6 mils. Alternatively, a one mil change in trace length leads to a .169 ps change in propagation time.

Width: In a stripline environment, propagation time is not a function of trace width. Therefore, there is no sensitivity at all to any tolerance on width.

In a microstrip environment, a changing width can

change the factor in **Equation 6**. For reasonable numbers on a normal board, the factor may change by maybe .5 % for a 15% change in line width, resulting in a .5% change in propagation time (about .008 ps/mil). This would be approximately 8 ps in a one inch length of trace. This is probably insignificant in most cases, but if it is a concern, then route critical traces in a stripline environment.

Sensitivity to $\mathcal{E}_r$: As we can see from **Equation 6**, propagation time is a function of the square root of the relative dielectric coefficient. A little math shows that (at least in the range of FR4) a .1 unit change in $\mathcal{E}_r$ leads to about a .002 ps/mil change in propagation time. This would lead to about 2 ps per inch, again probably not very significant.

Vias: The use of vias introduces at least two considerations into the tuning equation. The first has to do with the length of the via itself. It would seem evident that the length of the via should be included in the overall length of the trace. For example, if a trace travels on one layer for 750 mils, passes through a 62 mil via to another layer, then travels for another 250 mils to a via that goes back to a device pad on the first layer, the total path length is 1124 mils. Care must be taken here. We know of some design tools that measure trace length quite accurately, yet ignore any via lengths that might be in the path!

A second consideration is that vias add a small amount of capacitance to the trace at that point. That additional capacitance can attenuate some of the highest-order harmonics in the waveform. This has the apparent effect of slowing down the rise time, and therefore making the trace look slightly longer than it really is.[5] Although real, this effect is so small it can usually be ignored in all but the most extreme cases. But for these reasons, some engineers will not allow traces with very critical timing requirements to change layers on a board.

There are a variety of ways we can add length to our traces. One common way is to let the trace loop back upon itself. Loopbacks are seen in **Figure 1** and in the Appendix. We sometimes refer to these loops as "trombones" and the practice of using such loopbacks as "tromboning." A potential concern of tromboning is that there may be coupling between the adjacent traces. This coupling may impact propagation time by altering the path through the trace, by creating differential impedance issues that then change timing, and by creating crosstalk issues between the two sections of the trace.

Path: **Figure 3** illustrates a trace that loops back on itself. Three possible current paths are shown through the trace. We normally assume the current flows down the centerline of the trace (black line, (a)), at least the maximum current density flows there. But if there is an identical current flowing in the opposite direction in the adjacent trace (which there is almost by definition), then there is mutual inductance between the two trace segments. The impact of this is that the lowest impedance path for the current is where the two currents are closest together (green (b) or red (c) traces). This is exactly the same effect as why a high-speed return current for a signal wants to travel on the plane directly under the signal trace.

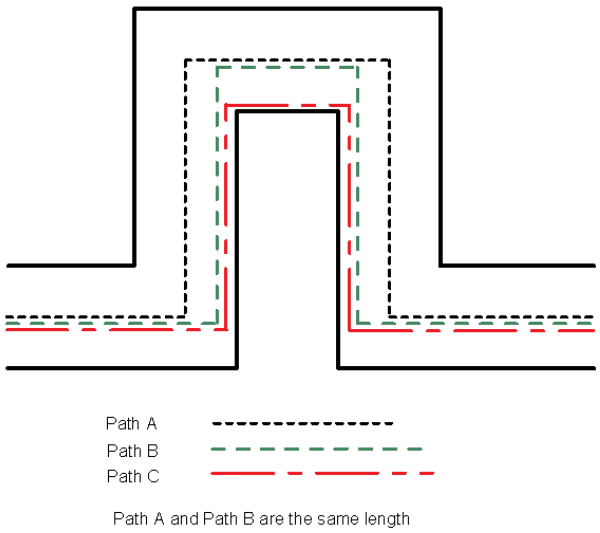


Figure 3: Alternative paths the current may take as a trace loops back on itself.

Upon inspection, it is apparent that the green path (b) is exactly the same length path as the black path (a). If this is the current path, there is no change in length. But if the red line (c) represents the path, then this path length is shorter by one trace width for each turn. For a 6 mil trace, this is about 1 ps per turn. A tuned trace may have many (10 or 20) such turns, resulting in as much as a 10 or 20 ps error in propagation time (the trace would appear faster by that much.)

I know of no studies that would confirm or reject the theory that the red path is in fact the correct path in such a situation.

Differential impedance: The signal in the adjacent part of the loop is, by definition, equal and opposite to the

signal in the first part of the loop. This is the definition of a differential pair. When there is differential coupling between two traces, their impedance reduces as a function of that coupling.[6]

Since it is known that the impedance of a transmission line is:

$$Z = \sqrt{\frac{L}{C}}$$

And also that the velocity of propagation is:

$$V_p = \sqrt{L * C}$$

Therefore, it follows that:

$$V_p = Z * C$$

Therefore, does it follow that the velocity of propagation changes when the impedance reduces because of differential coupling?

The answer is "No." It turns out that (at least in stripline) both the L and the C change, and these changes exactly balance. So while the differential impedance does change, so does C, and the velocity of propagation does not.

Crosstalk: This is the one area where there can be a significant change in propagation time. When traces loop back on themselves, there is crosstalk between them. There is general agreement among experts that in the case of such trombone-like patterns the resulting delay time is shorter than the trace length would predict. Howard Johnson states "Short, coupled switchbacks produce smaller delays than the total trace length would indicate. Long, coupled switchbacks distort the signals."[7]

Precisely how and why this happens, and the effect of this, will be covered in Part 2 of this article series.

PATTERN SENSITIVITY

There are a variety of ways trace lengths can be added. The Mentor Graphics Expedition design tool offers the designer several choices and several design rule options in its Editor Control Menu (see **Figure 4**).

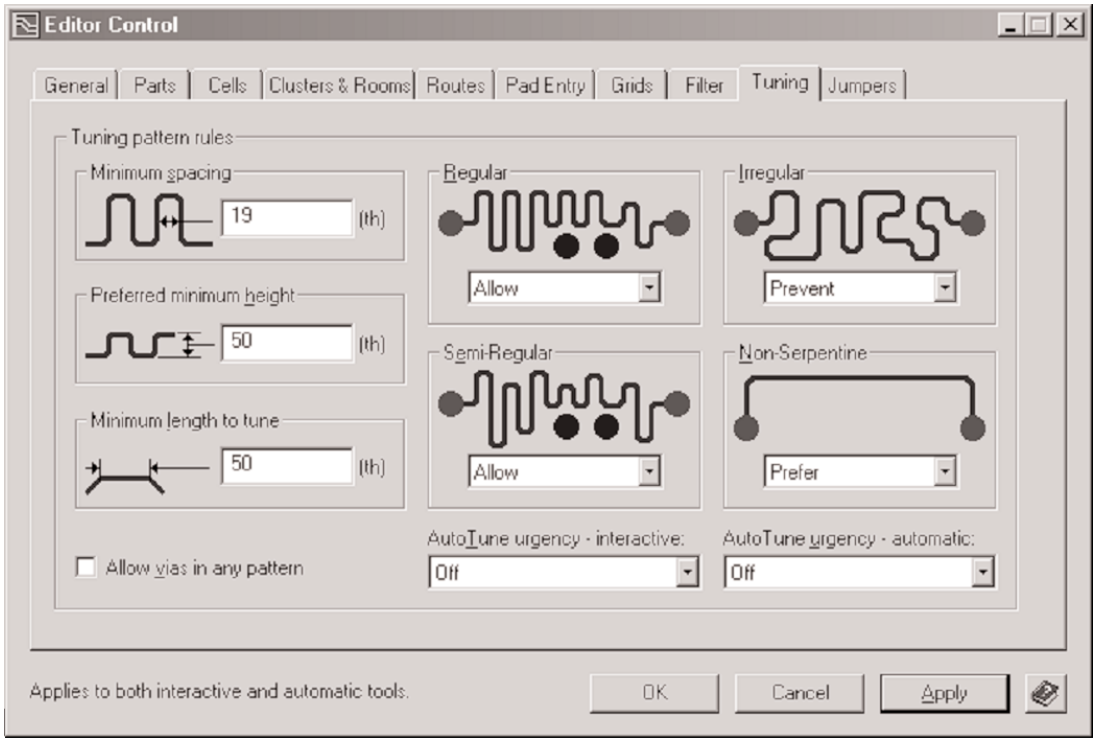


Figure 4: Expedition design rules editor..

Assuming other high-speed design rules related to impedance control and EMI are satisfied, I know of no reason to prefer any one of these rules over any other, except for the crosstalk issues I will cover in Part 2 of this series.

There are some people who may argue that a closely spaced pattern, like the one shown in **Figure 5**, might look like a dish antenna and cause EMI issues,[8] we don't believe such is the case, particularly if loop areas are otherwise small and if the traces are in stripline environments.

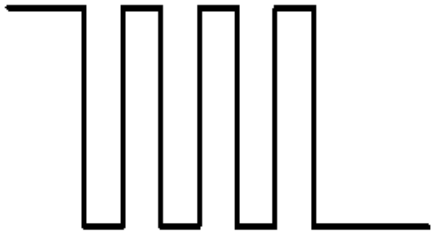


Figure 5: Some people think this trace configuration resembles a "dish" antenna.

THE SPECIAL CASE OF DIFFERENTIAL PAIRS:

I pointed out in another article[9] that if signal integrity is an issue then differential trace pairs must be equal length and also equally spaced. The equal length requirement is to prevent "mode shift," or common mode (and therefore EMI) problems. The equal spacing requirement is to maintain constant differential impedance. If you have a requirement as is illustrated in **Figure 6**, you can't meet both of these requirements at the same time! There is not industry wide agreement on what to do in such a situation, but my view is this: The mode shift requirement is more important than the constant impedance requirement. So trace length should be added to the inner trace to match the trace lengths. Further, I believe it is desirable to add that additional trace length as close as practical to the point where the trace lengths began to differ, as shown in the figure. This minimizes the length over which the mode shift might occur.

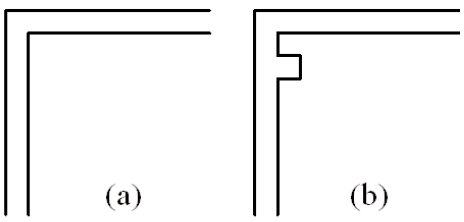


Figure 6: The differential pair in (a) cannot meet the requirements of equal length and equal spacing at the same time. It is preferable to add length to the inner trace, as suggested in (b), in order to match trace lengths.

SUMMARY

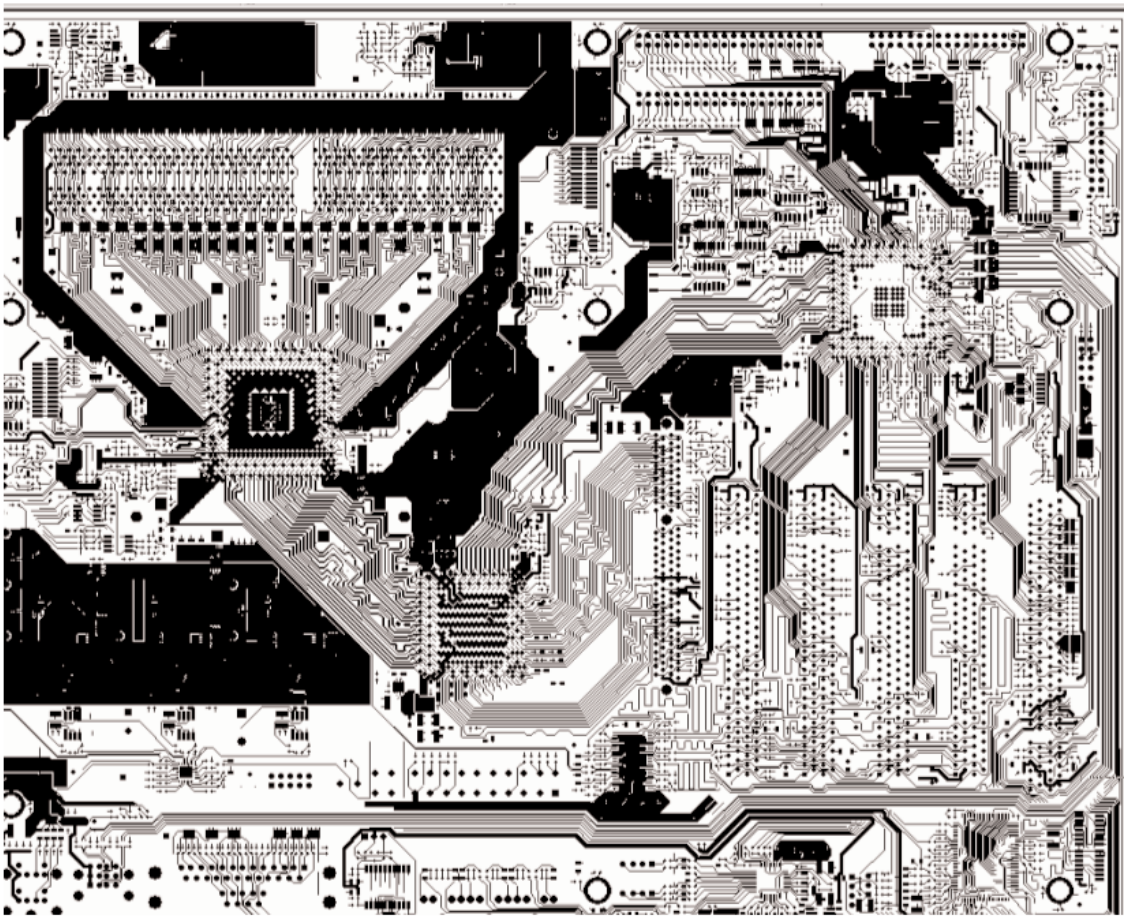
It is common for PCB traces to require tuning to meet various timing objectives. We tune traces by adding length to them. If the requirements are relative, i.e. traces must simply be the same length, tuning is not too difficult. But if there are absolute timing requirements that must be met, then the designer also needs to know the propagation speed of the signal in the trace environment. In stripline environments, the propagation speed is solely determined by the relative dielectric coefficient of the material, but in microstrip environments the calculations are much more complicated and can also depend on trace parameters (width and distance from the plane.) The trace pattern used is generally not too important except for crosstalk issues when the traces segments closely "trombone" to each other.

FOOTNOTES

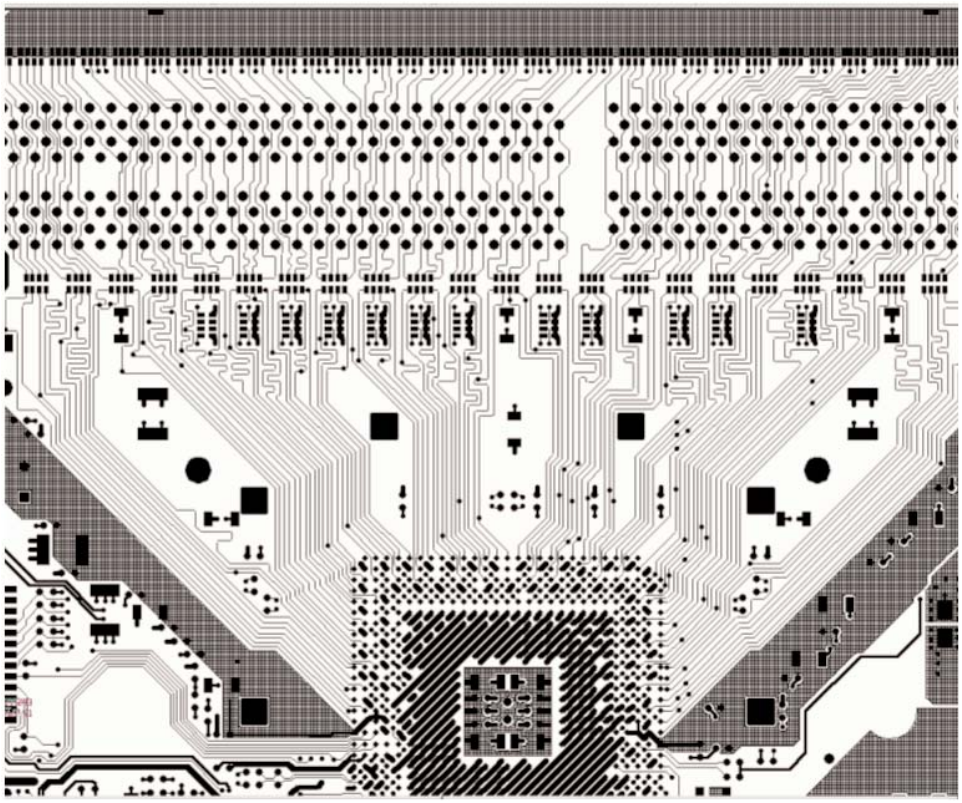
1. No pun intended!
2. This is actually the speed of light in a vacuum. But the speed of light in the air is so close to this that the difference is meaningful only to an astronomer!
3. See "Propagation Times and Critical Length: How They Interrelate," available at *www.mentor.com/pcb/tech_papers.cfm*.
4. The common "adjustment" for the effective $\mathcal{E}_r$ of microstrip traces, $\mathcal{E}'_r = .475\mathcal{E}_r + .67$, has been shown to be inaccurate. See "Microstrip Propagation Times: Slower Than We Think," avalable at *www.mentor.com/pcb/tech_papers.cfm.*
5. See "The Effects Of Vias on PCB Traces, Printed Circuit Design, August, 1996, available at *www.ultracad.com*.
6. See "Differential Impedance: What's the Difference?", Printed Circuit Design, August, 1998, available at *www.ultracad.com*.
7. Howard Johnson, "Serpentine Delays", EDN Magazine, February 2001
8. Unfortunately, UltraCAD argued this many years ago, a position it has since retracted!
9 See "Differential Design Rules: Truth vs Fiction", available at *www.mentor.com/pcb/tech_papers.cfm*

APPENDIX 1

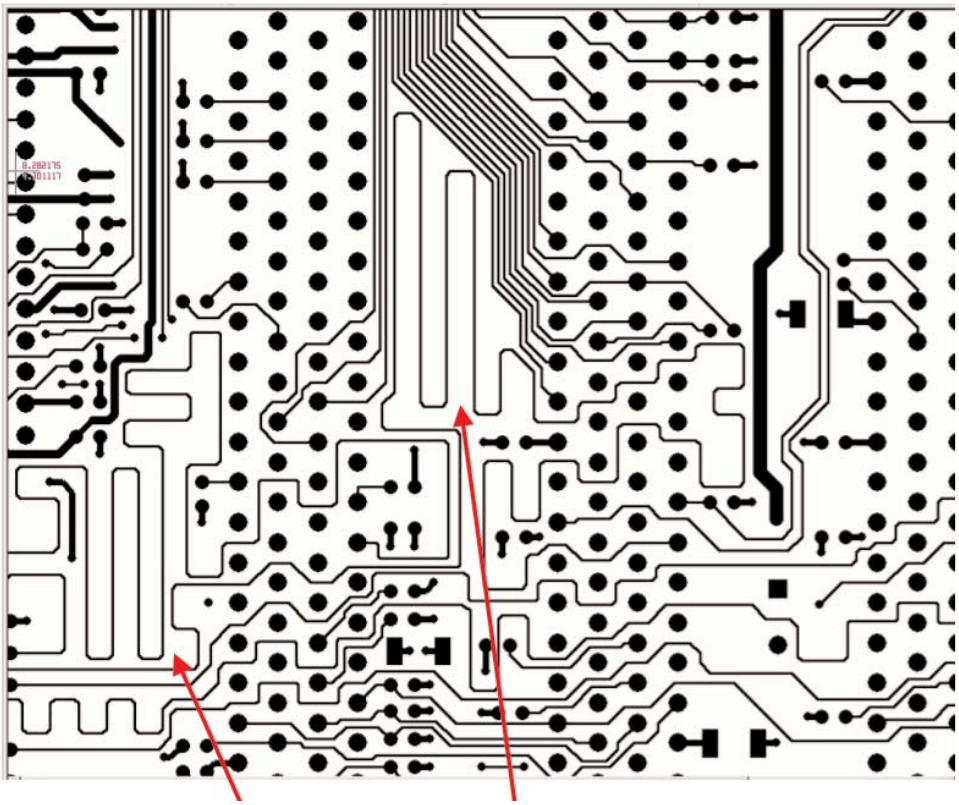
Here are several illustrations of trace routing and tuning on a computer motherboard, courtesy of Wayne Pulliam and Advanced Micro Devices (AMD).



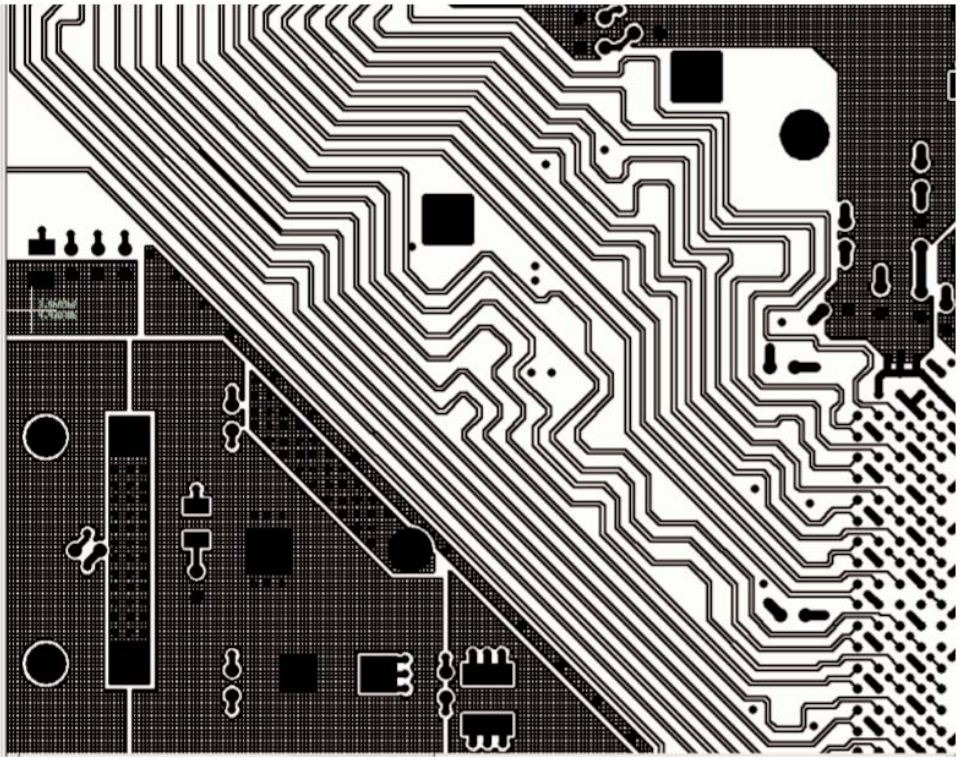
This motherboard is routed on two trace layers. Here is one of those layers.



Here is a closer view (above) of the upper left corner of the previous picture. The amount of trace tuning is apparent.



There are numerous tuned traces on this portion of the board. Note in particular the areas of "tromboning" (arrows) where the segments are separated to prevent crosstalk between them.



In this area of the board differential trace pairs are tuned between the two parts of the circuit.

ABOUT THE AUTHOR

Douglas Brooks has a BS and an MS in Electrical Engineering from Stanford University and a PhD from the University of Washington. During his career has held positions in engineering, marketing, and general management with such companies as Hughes Aircraft, Texas Instruments and ELDEC.

Brooks has owned his own manufacturing company and he formed UltraCAD Design Inc. in 1992. UltraCAD is a service bureau in Bellevue, WA, that specializes in large, complex, high density, high speed designs, primarily in the video and data processing industries. Brooks has written numerous articles through the years, including articles and a column for Printed Circuit Design magazine, and has been a frequent seminar leader at PCB Design Conferences. His primary objective in his speaking and writing has been to make complex issues easily understandable to those without a technical background. You can visit his web page at http://www.ultracad.com and e-mail him at doug@eskimo.com.