5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Name	Description	Remark
1	VCC_IN	Power Supply (3.3V)	
2	VCC_IN	Power Supply (3.3 V)	
3	GND	Ground	
4	GND	Ground	
5	RX0-	Differential Data Input, CH0 (Negative)	R0 ~ R5, G0
6	RX0+	Differential Data Input, CH0 (Positive)	
7	GND	Ground	
8	RX1-	Differential Data Input, CH1 (Negative)	G1 ~ G5, B0, B1
9	RX1+	Differential Data Input , CH1 (Positive)	
10	GND	Ground	
11	RX2-	Differential Data Input , CH2 (Negative)	B2 ~ B5, DE, Hsync, Vsync
12	RX2+	Differential Data Input , CH2 (Positive)	
13	GND	Ground	
14	CLK-	Differential Clock Input (Negative)	LVDS Level Clock
15	CLK+	Differential Clock Input (Positive)	
16	GND	Ground	
17	NA	Non-connection	
18	NA	Non-connection	
19	GND	Ground	
20	GND	Ground	

Note (1) Connector Part No.: STARCONN 076B20-0048RA-G4 or JAE FI-SEB20P-HFE or equivalent.

Note (2) Mating Connector Part No.: JAE-FI-SE20M, FI-S20S or equivalent.

Note (3) The first pixel is odd.

Note (4) Input signal of even and odd clock should be the same timing.