XC9536 In-System Programmable CPLD

DS064 (v6.2) April 15, 2005

Product Specification

Features

- 5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 100 MHz
- 36 macrocells with 800 usable gates
- Up to 34 user I/O pins
- 5V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3V or 5V I/O capability
- Advanced CMOS 5V Fast FLASH™ technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 44-pin PLCC, 44-pin VQFP, 48-pin CSP packages

Description

The XC9536 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9536 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) = MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC9536 device.

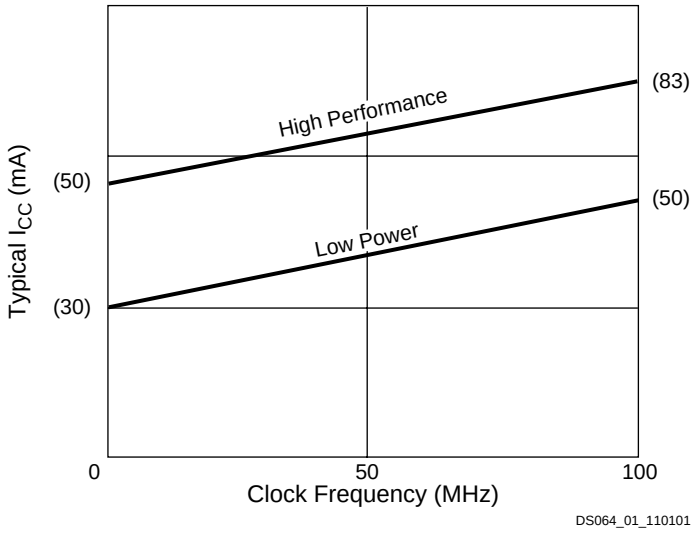


Figure 1: **Typical I_{CC} vs. Frequency for XC9536**

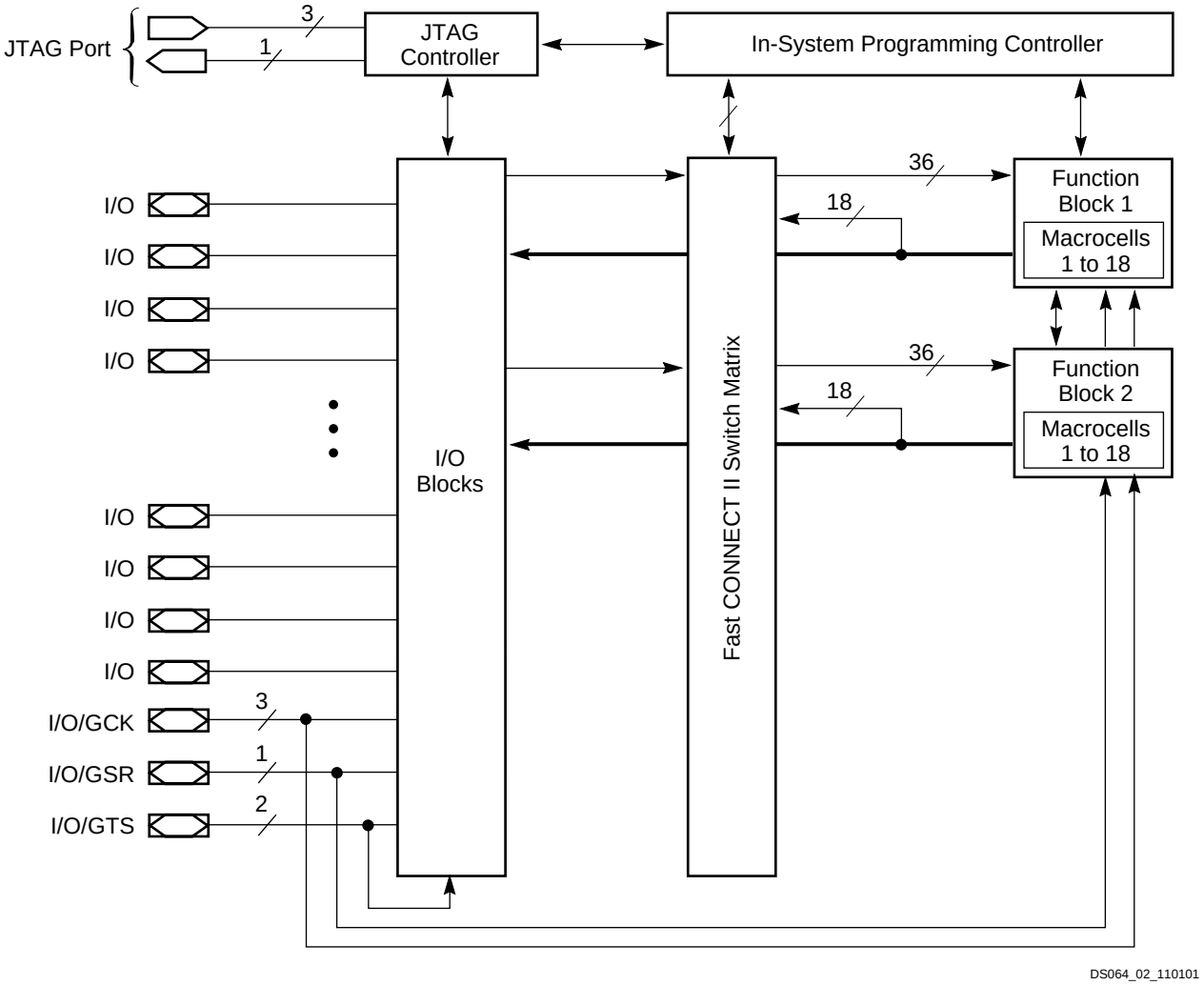


Figure 2: **XC9536 Architecture**
Function block outputs (indicated by the bold line) drive the I/O blocks directly.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	4.75	5.25	V
		Industrial T_A = –40°C to +85°C	4.5	5.5	
V_{CCIO}	Supply voltage for output drivers for 5V operation	Commercial T_A = 0°C to 70°C	4.75	5.25	V
		Industrial T_A = –40°C to +85°C	4.5	5.5	
	Supply voltage for output drivers for 3.3V operation		3.0	3.6	
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles

DC Characteristic Over Recommended Operating Conditions

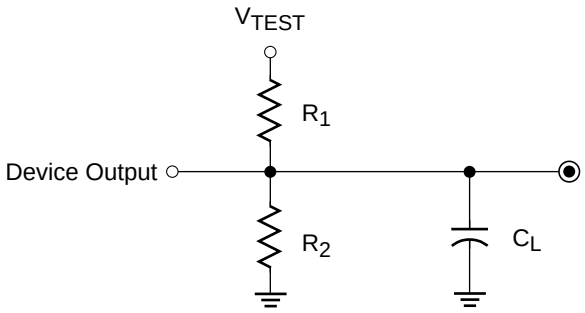
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5V outputs	I_{OH} = –4.0 mA, V_{CC} = Min	2.4	-	V
	Output high voltage for 3.3V outputs	I_{OH} = –3.2 mA, V_{CC} = Min	2.4	-	V
V_{OL}	Output low voltage for 5V outputs	I_{OL} = 24 mA, V_{CC} = Min	-	0.5	V
	Output low voltage for 3.3V outputs	I_{OL} = 10 mA, V_{CC} = Min	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	-	±10	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	30 (Typical)		mA

AC Characteristics

Symbol	Parameter	XC9536-5		XC9536-6		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	5.0	-	6.0	-	7.5	-	10.0	-	15.0	ns
T_{SU}	I/O setup time before GCK	3.5	-	3.5	-	4.5	-	6.0	-	8.0	-	ns
T_{H}	I/O hold time after GCK	0	-	0	-	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	4.0	-	4.0	-	4.5	-	6.0	-	8.0	ns
f_{CNT}(1)	16-bit counter frequency	100.0	-	100.0	-	125.0	-	111.1	-	95.2	-	MHz
f_{SYSTEM}(2)	Multiple FB internal operating frequency	100.0	-	100.0	-	83.3	-	66.7	-	55.6	-	MHz
T_{PSU}	I/O setup time before p-term clock input	0.5	-	0.5	-	0.5	-	2.0	-	4.0	-	ns
T_{PH}	I/O hold time after p-term clock input	3.0	-	3.0	-	4.0	-	4.0	-	4.0	-	ns
T_{PCO}	P-term clock output valid	-	7.0	-	7.0	-	8.5	-	10.0	-	12.0	ns
T_{OE}	GTS to output valid	-	5.0	-	5.0	-	5.5	-	6.0	-	11.0	ns
T_{OD}	GTS to output disable	-	5.0	-	5.0	-	5.5	-	6.0	-	11.0	ns
T_{POE}	Product term OE to output enabled	-	9.0	-	9.0	-	9.5	-	10.0	-	14.0	ns
T_{POD}	Product term OE to output disabled	-	9.0	-	9.0	-	9.5	-	10.0	-	14.0	ns
T_{WLH}	GCK pulse width (High or Low)	4.0	-	4.0	-	4.0	-	4.5	-	5.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	7.0	-	7.0	-	7.0	-	7.5	-	8.0	-	ns

Notes:

1. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable. f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0V	5.0V	160Ω	120Ω	35 pF
	3.3V	3.3V	260Ω	360Ω	35 pF

DS067_03_110101

Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC9536-5		XC9536-6		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Buffer Delays												
T_{IN}	Input buffer delay	-	1.5	-	1.5	-	2.5	-	3.5	-	4.5	ns
T_{GCK}	GCK buffer delay	-	1.5	-	1.5	-	1.5	-	2.5	-	3.0	ns
T_{GSR}	GSR buffer delay	-	4.0	-	4.0	-	4.5	-	6.0	-	7.5	ns
T_{GTS}	GTS buffer delay	-	5.0	-	5.0	-	5.5	-	6.0	-	11.0	ns
T_{OUT}	Output buffer delay	-	2.0	-	2.0	-	2.5	-	3.0	-	4.5	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	-	0	-	0	ns
Product Term Control Delays												
T_{PTCK}	Product term clock delay	-	3.0	-	3.0	-	3.0	-	3.0	-	2.5	ns
T_{PTSR}	Product term set/reset delay	-	1.0	-	1.0	-	2.0	-	2.5	-	3.0	ns
T_{PTTS}	Product term 3-state delay	-	5.5	-	5.5	-	4.5	-	3.5	-	5.0	ns
Internal Register and Combinatorial Delays												
T_{PDI}	Combinatorial logic propagation delay	-	0.5	-	0.5	-	0.5	-	1.0	-	3.0	ns
T_{SUI}	Register setup time	2.5	-	2.5	-	1.5	-	2.5	-	3.5	-	ns
T_{HI}	Register hold time	1.0	-	1.0	-	3.0	-	3.5	-	4.5	-	ns
T_{COI}	Register clock to output valid time	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns
T_{AOI}	Register async. S/R to output delay	-	6.0	-	6.0	-	6.5	-	7.0	-	8.0	ns
T_{RAI}	Register async. S/R recover before clock	5.0	-	5.0	-	7.5	-	10.0	-	10.0	-	ns
T_{LOGI}	Internal logic delay	-	1.0	-	1.0	-	2.0	-	2.5	-	3.0	ns
T_{LOGILP}	Internal low power logic delay	-	9.0	-	9.0	-	10.0	-	11.0	-	11.5	ns
Feedback Delays												
T_F	Fast CONNECT II feedback delay	-	6.0	-	6.0	-	8.0	-	9.5	-	11.0	ns
Time Adders												
T_{PTA}(1)	Incremental product term allocator delay	-	0.8	-	0.8	-	1.0	-	1.0	-	1.0	ns
T_{SLEW}	Slew-rate limited delay	-	3.5	-	3.5	-	4.0	-	4.5	-	5.0	ns

Notes:
1. T_{PTA} is multiplied by the span of the function as defined in the XC9500 family data sheet.

XC9536 I/O Pins

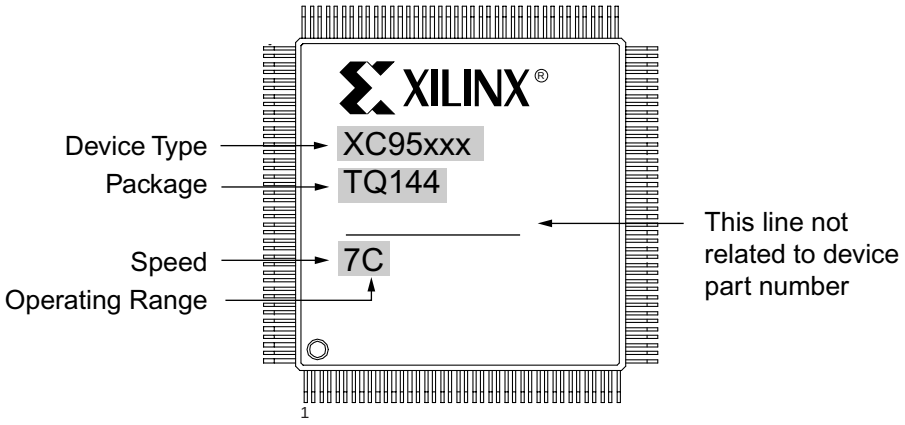
Function Block	Macrocell	PC44	VQ44	CS48	BScan Order
1	1	2	40	D6	105
1	2	3	41	C7	102
1	3	5[1]	43[1]	B7[1]	99
1	4	4	42	C6	96
1	5	6[1]	44[1]	B6[1]	93
1	6	8	2	A6	90
1	7	7[1]	1[1]	A7[1]	87
1	8	9	3	C5	84
1	9	11	5	B5	81
1	10	12	6	A4	78
1	11	13	7	B4	75
1	12	14	8	A3	72
1	13	18	12	B2	69
1	14	19	13	B1	66
1	15	20	14	C2	63
1	16	22	16	C3	60
1	17	24	18	D2	57
1	18	–	–	-	54
2	1	1	39	D7	51
2	2	44	38	E5	48
2	3	42[1]	36[1]	E6[1]	45
2	4	43	37	E7	42
2	5	40[1]	34[1]	F6[1]	39
2	6	39[1]	33[1]	G7[1]	36
2	7	38	32	G6	33
2	8	37	31	F5	30
2	9	36	30	G5	27
2	10	35	29	F4	24
2	11	34	28	G4	21
2	12	33	27	E3	18
2	13	29	23	F2	15
2	14	28	22	G1	12
2	15	27	21	F1	9
2	16	26	20	E2	6
2	17	25	19	E1	3
2	18	-	-	-	0

Notes: :
1. Global control pin.

XC9536 Global, JTAG and Power Pins

Pin Type	PC44	VQ44	CS48
I/O/GCK1	5	43	B7
I/O/GCK2	6	44	B6
I/O/GCK3	7	1	A7
I/O/GTS1	42	36	E6
I/O/GTS2	40	34	F6
I/O/GSR	39	33	G7
TCK	17	11	A1
TDI	15	9	B3
TDO	30	24	G2
TMS	16	10	A2
V_{CCINT} 5V	21, 41	15, 35	C1,F7
V_{CCIO} 3.3V/5V	32	26	G3
GND	23, 10, 31	17, 4, 25	A5, D1, F3
No Connects	—	—	C4, D3, D4, E4

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Notes:

1. Due to the small size of chip scale packages, part marking on these packages does not follow the above sample and the complete part number cannot be included in the marking. Part marking on chip scale packages by line:
   - Line 1 = X (Xilinx logo), then truncated part number (no XC), i.e., 95xxx.
   - Line 2 = Not related to device part number.
   - Line 3 = Not related to device part number.
   - Line 4 = Package code, speed, operating temperature, three digits not related to device part number. Package code: C1 = CS48.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9536-5PC44C	5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536-5VQ44C	5 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	C
XC9536-5CS48C	5 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9536-6PC44C	6 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536-6VQ44C	6 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	C
XC9536-7PC44C	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536-7VQ44C	7.5 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	C
XC9536-7CS48C	7.5 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9536-7PC44I	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9536-7VQ44I	7.5 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	I
XC9536-10PC44C	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536-10VQ44C	10 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	C
XC9536-10CS48C	10 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9536-10PC44I	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9536-10VQ44I	10 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	I
XC9536-10CS48I	10 ns	CS48	48-ball	Chip Scale Package (CSP)	I
XC9536-15PC44C	15 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536-15VQ44C	15 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	C
XC9536-15PC44I	15 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9536-15VQ44I	15 ns	VQ44	44-pin	Very Thin Quad Flat Pack (VQFP)	I

Notes:

1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/04/98	5.0	Revised datga sheet to remove PCI compliancy statement and remove T_{LP}.
06/18/03	6.0	Updated format.
08/21/03	6.1	Updated Package Device Marking Pin 1 orientation.
04/15/05	6.2	Added Asynchronous Preset Reset Pulse Width Specification (T_{APRPW})