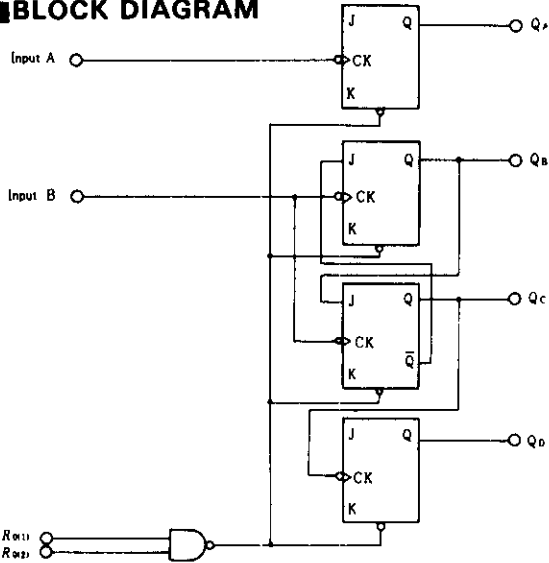


HD74LS92 • Divide-by-Twelve Counters

The HD74LS92 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-stage binary counter for divide-by-six. To use this maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Reset/Count Function Table

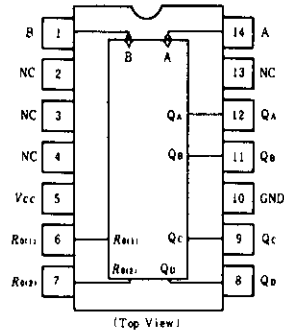
Reset Inputs		Outputs			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

BCD Count Sequence (Notes 1)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Notes) 1. Output Q_A is connected to input B for BCD count.
3. H; high level, L; low level, X; irrelevant

■ PIN ARRANGEMENT



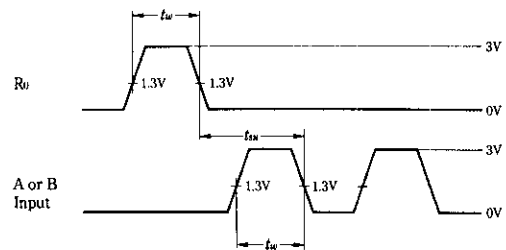
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	R Input	7.0	V
	A, B Input	5.5	V
Operating temperature range	T_{opr}	-20 ~ +75	°C
Storage temperature range	T_{stg}	-65 ~ +150	°C

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Count frequency	A input	0	—	32	MHz
	B input	0	—	16	
Pulse width	A input	15	—	—	ns
	B input	30	—	—	
	Reset inputs	15	—	—	
Setup time	t_{su}	25	—	—	ns

■ TIMING DEFINITION



HD74LS92

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	—		V
		V_{IL}			—	—	0.8	V
Output voltage		V_{OH}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -400\mu\text{A}$		2.7	—		V
		V_{OL}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, I_{OL} = 4\text{mA}^{**}$		—	—	0.4	V
		V_{OL}	$V_{IL} = 0.8\text{V}, I_{OL} = 8\text{mA}^{**}$		—	—	0.5	V
Input current	Any Reset	I_{IL}	$V_{CC} = 5.25\text{V}, V_I = 0.4\text{V}$		—	—	0.4	mA
	A input				—	—	2.4	
	B input				—	—	3.2	
	Any Reset	I_{IH}	$V_{CC} = 5.25\text{V}, V_I = 2.7\text{V}$		—	—	20	μA
	A input				—	—	40	
	B input				—	—	80	
	Any Reset	I_I	$V_{CC} = 5.25\text{V}$	$V_I = 7\text{V}$	—	—	0.1	mA
	A input			$V_I = 5.5\text{V}$	—	—	0.2	
	B input				—	—	0.4	
Short circuit output current		I_{OS}	$V_{CC} = 5.25\text{V}$		-20	—	100	mA
Supply current ***		I_{CC}	$V_{CC} = 5.25\text{V}$		—	9	15	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75\text{V}, I_{IK} = -18\text{mA}$		—	—	-1.5	V

* $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

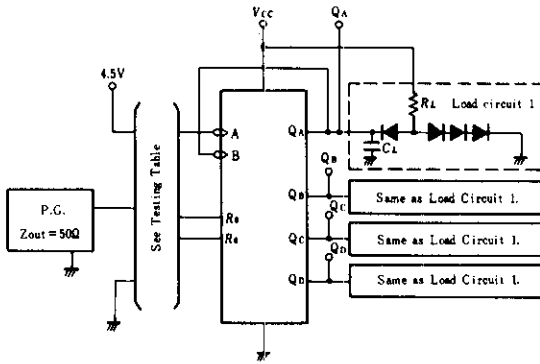
*** I_{CC} is measured with all outputs open both R_o inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

■ SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$)

Item	Symbol	Input	Outputs	Test Conditions	min	typ	max	Unit	
Maximum count frequency	f_{max}	A	Q_A	$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$	32	42	—	MHz	
		B	Q_B		16	—	—	MHz	
Propagation delay time	t_{PLH}	A	Q_A		—	10	16	ns	
			Q_B		—	12	18	ns	
	t_{PLH}	A	Q_D		—	32	48	ns	
			Q_C		—	34	50	ns	
	t_{PHL}	B	Q_B		—	10	16	ns	
			Q_C		—	14	21	ns	
	t_{PLH}	B	Q_C		—	10	16	ns	
			Q_D		—	14	21	ns	
	t_{PLH}	B	Q_D		—	—	21	32	ns
			Q_A		—	—	23	35	ns
	t_{PHL}	Set to 0	$Q_A - Q_D$	—	—	26	40	ns	

TESTING METHOD

1) Test Circuit



- Notes) 1. Input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR=1\text{MHz}$, duty cycle=50%
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074 $\text{\textcircled{P}}$.

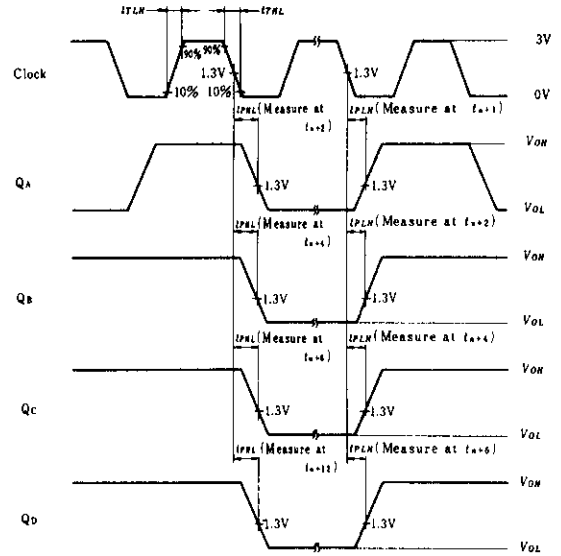
2) Testing Table

Item	From input to output	Inputs			Outputs			
		A	B	R_0	Q_A	Q_B	Q_C	Q_D
f_{max}	A \rightarrow Q	IN	to Q_A	GND	Out	Out	Out	Out
	B \rightarrow Q	4.5V	IN	GND	-	Out	Out	Out
t_{PLH}	A \rightarrow Q_A	IN	to Q_A	GND	Out	-	-	-
	A \rightarrow Q_D	IN	to Q_A	GND	-	-	-	Out
t_{PHL}	B \rightarrow Q_B	4.5V	IN	GND	-	Out	-	-
	B \rightarrow Q_D	4.5V	IN	GND	-	-	Out	-
	$R_0 \rightarrow$ Q	IN*	to Q_A	IN	Out	Out	Out	Out

*; For initialized.

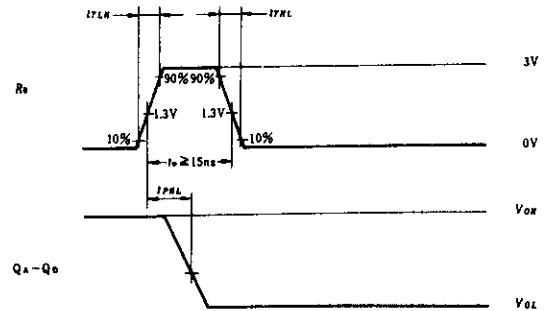
**; Measured with each input and unused inputs at 4.5V.

Waveform-1 f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q)

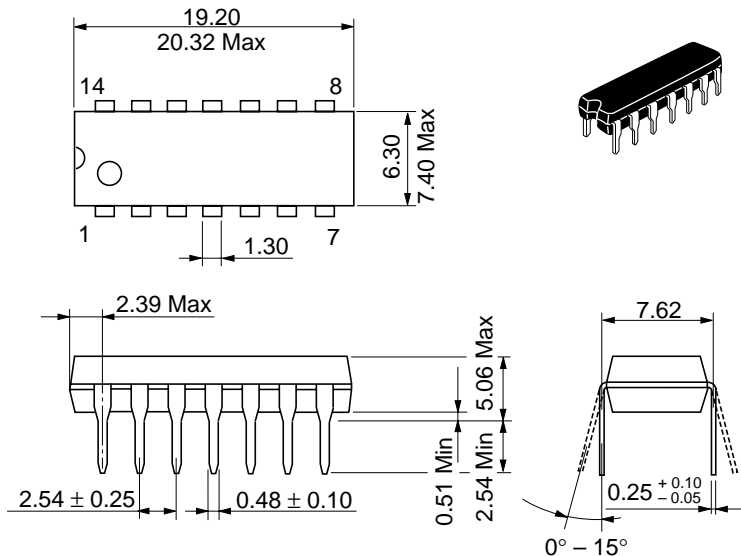


- Notes) 1. Input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR=1\text{MHz}$, duty cycle=50% and; for f_{max} , $t_{TLH}=t_{THL} \leq 2.5\text{ns}$.
 2. t_n is reference bit time when all outputs are low.

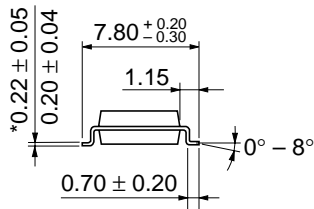
Waveform-2 t_{PHL} ($R_0 \rightarrow$ Q)



- Notes) 1. $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$.

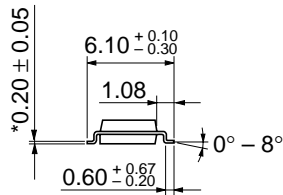
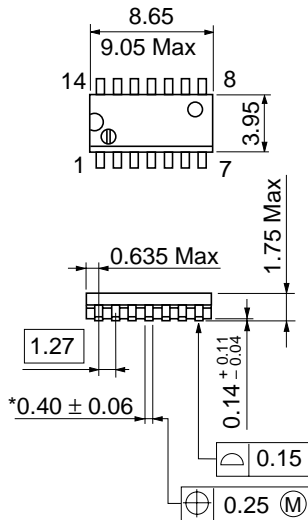


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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