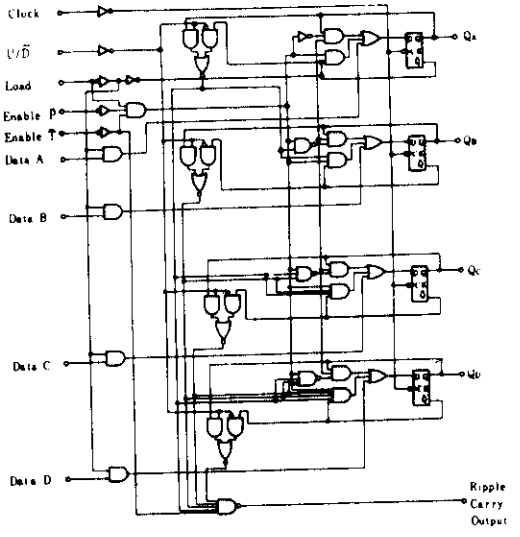
HD74LS669 ●Synchronous Up/Down 4-bit Binary Counters

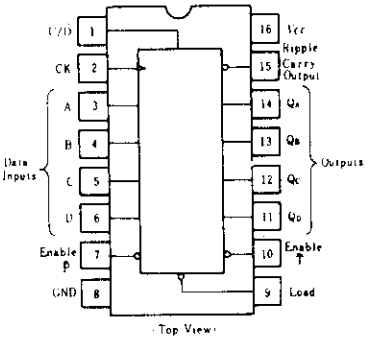
This synchronous presettable 4-bit binary counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages.

Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Output current		I_{OH}	—	—	−400	μA
Output current		I_{OL}	—	—	8	mA
Clock frequency		f_{clock}	0	—	25	MHz
Clock pulse width		$t_{w(CK)}$	25	—	—	ns
Setup time	Input Data A, B, C, D	t_{su}	25	—	—	ns
	Enable $\overline{P}$, $\overline{T}$		35	—	—	
	Load		30	—	—	
	Up/Down		35	—	—	
Hold time		t_h	0	—	—	ns

■ELECTRICAL CHARACTERISTICS (Ta=−20～+75°C)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2	—	—	V
		V_{IL}			—	—	0.8	V
Output voltage		V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−400μA		2.7	—	—	V
		V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=4mA	—	—	0.4	V
				I_{OL}=8mA	—	—	0.5	V
Input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	I_{IH}	V_{CC}=5.25V, V_I=2.7V		—	—	20	μA
	Clock, $\overline{T}$				—	—	20	
	Load				—	—	40	
	A, B, C, D, $\overline{P}$, U/$\overline{D}$	I_{IL}	V_{CC}=5.25V, V_I=0.4V		—	—	−0.4	mA
	Clock, $\overline{T}$				—	—	−0.4	
	Load				—	—	−0.8	
	A, B, C, D, $\overline{P}$, U/$\overline{D}$	I_I	V_{CC}=5.25V, V_I=7V		—	—	0.1	mA
	Clock, $\overline{T}$				—	—	0.1	
	Load				—	—	0.2	
Short-circuit output current		I_{OS}	V_{CC}=5.25V		−20	—	−100	mA
Supply current **		I_{CC}	V_{CC}=5.25V		—	20	34	mA
Input clamp voltage		V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

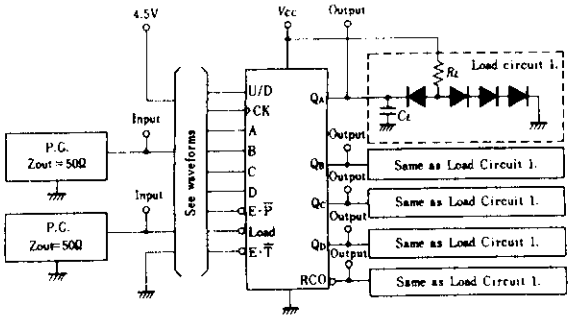
** I_{CC} is measured after applying a momentary 4.5V, then ground, to clock input with all other inputs grounded the outputs open.

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	f_{max}			C_L=15pF, R_L=2kΩ	25	32	—	MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry		—	26	40	ns
	t_{PHL}				—	40	60	
	t_{PLH}	Clock	Q_A～Q_D		—	18	27	ns
	t_{PHL}				—	18	27	
	t_{PLH}	Enable $\overline{T}$	Ripple Carry		—	11	17	ns
	t_{PHL}				—	29	45	
	t_{PLH}	Up/Down	Ripple Carry		—	22	35	ns
	t_{PHL}				—	26	40	

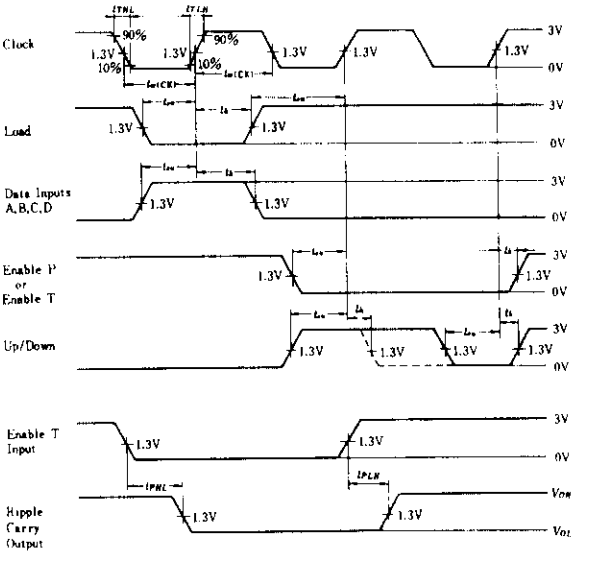
■TESTING METHOD

1) Test Circuit



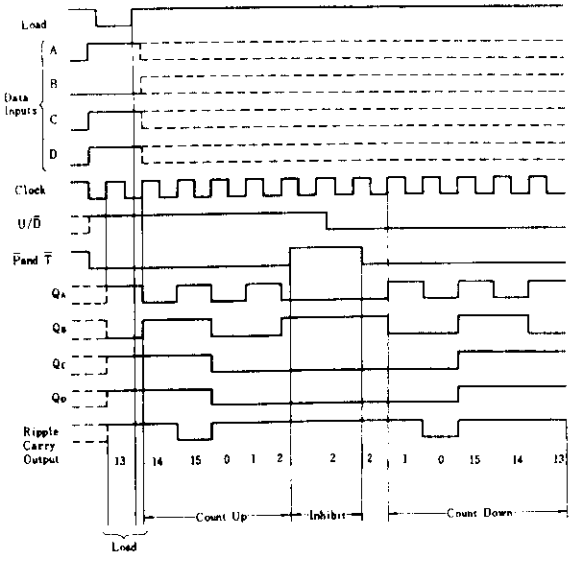
Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

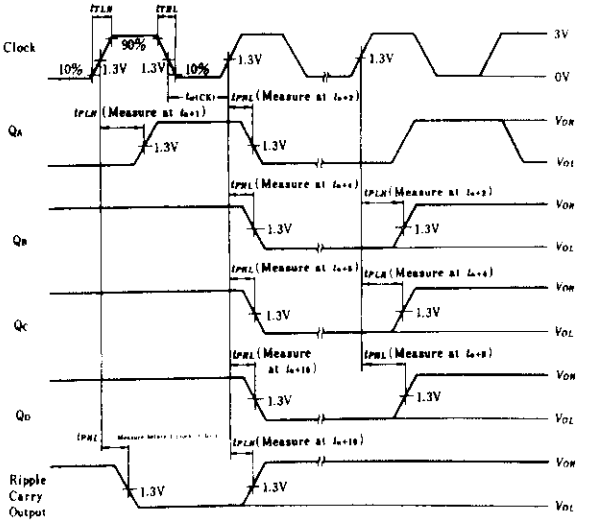
Waveform



Notes) 1. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A through Q_D high).
2. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) are ripple carry output transition will be in phase. If the count is maximum (15) the ripple carry output will be out of phase.
3. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz

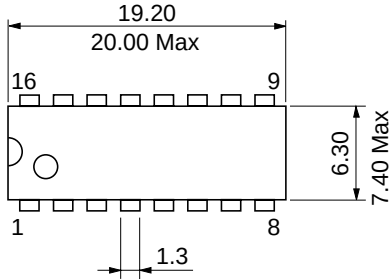
■COUNT SEQUENCE

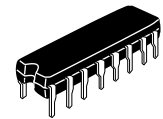


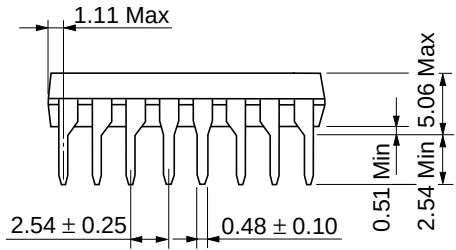


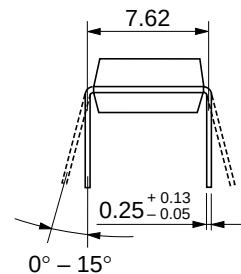
Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, $PRR = 1$MHz, duty cycle 50%.
2. For f_{max}, $t_{TLH} = t_{THL} \leqq 2.5$ns.
3. t_n is the bit-time when all outputs are low.

Unit: mm



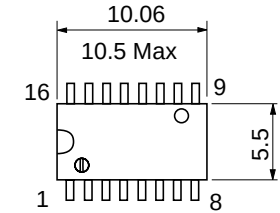


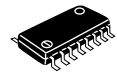


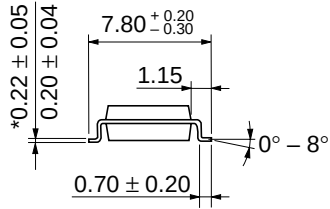


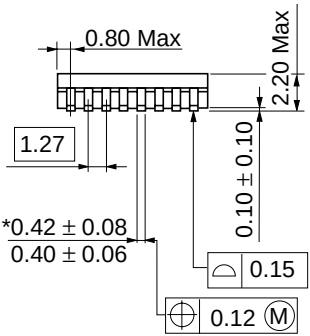
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm









*Dimension including the plating thickness
Base material dimension

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JEDEC	—
EIAJ	Conforms
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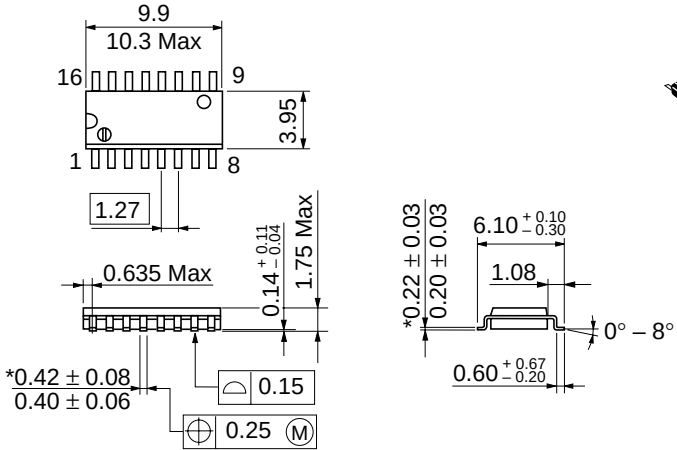
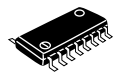
Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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