

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT597

**8-bit shift register with input
flip-flops**

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit shift register with input flip-flops

74HC/HCT597

FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay SH _{CP} to Q | C _L = 15 pF; V _{CC} = 5 V | 17 | 20 | ns |
| | ST _{CP} to Q | | 25 | 29 | ns |
| | $\overline{\text{PL}}$ to Q | | 21 | 26 | ns |
| f _{max} | maximum clock frequency SH _{CP} | | 96 | 83 | MHz |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per package | notes 1 and 2 | 29 | 32 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

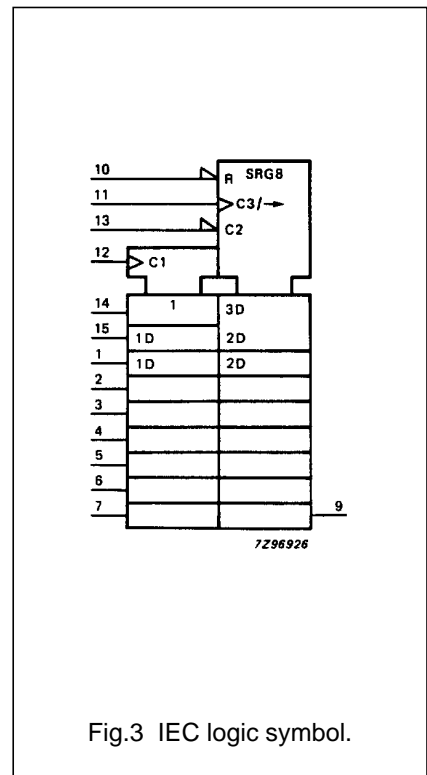
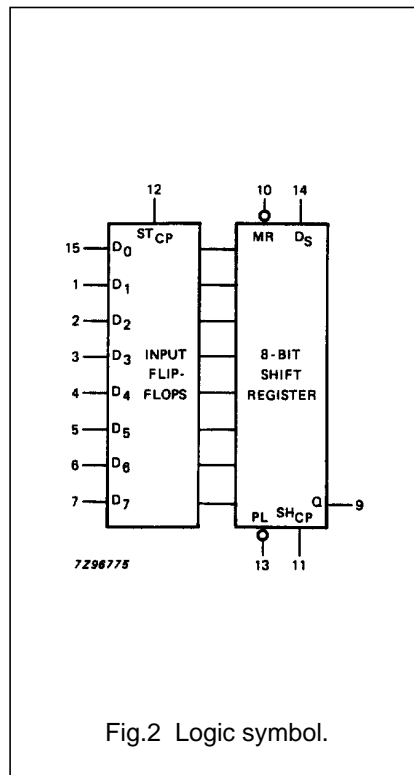
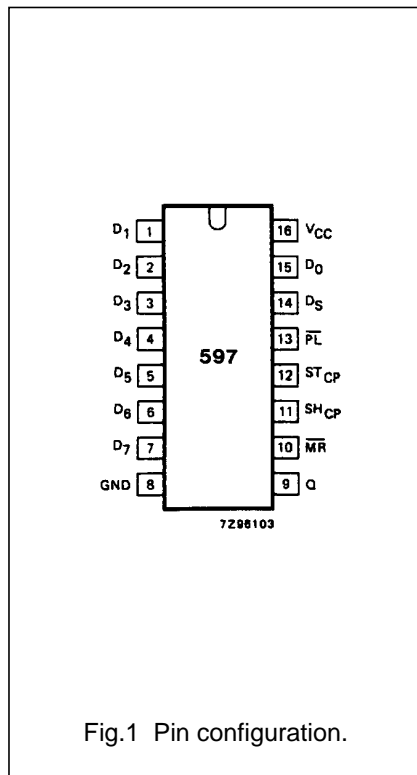
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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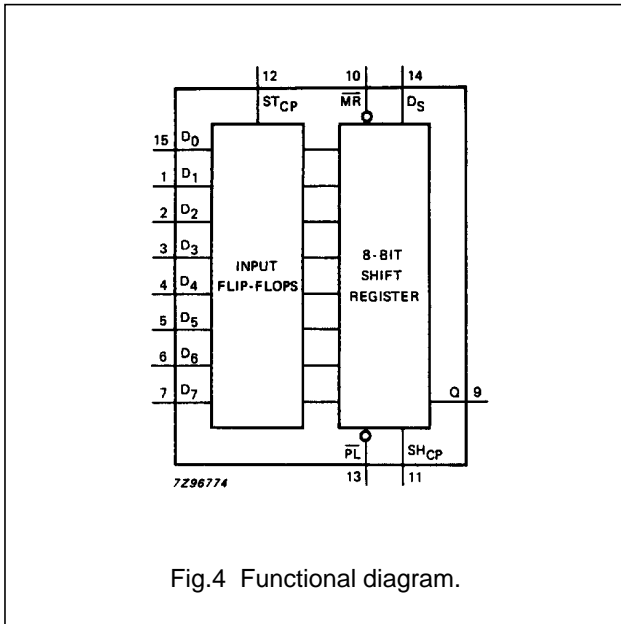
PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|-------------------------|----------------------------------|---|
| 8 | GND | ground (0 V) |
| 9 | Q | serial data output |
| 10 | \overline{MR} | asynchronous reset input (active LOW) |
| 11 | SH _{CP} | shift clock input (LOW-to-HIGH, edge-triggered) |
| 12 | ST _{CP} | storage clock input (LOW-to-HIGH, edge-triggered) |
| 13 | \overline{PL} | parallel load input (active LOW) |
| 14 | D _S | serial data input |
| 15, 1, 2, 3, 4, 5, 6, 7 | D ₀ to D ₇ | parallel data inputs |
| 16 | V _{CC} | positive supply voltage |



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FUNCTION TABLE

| ST _{CP} | SH _{CP} | \overline{PL} | \overline{MR} | FUNCTION |
|------------------|------------------|-----------------|-----------------|---|
| ↑ | X | X | X | data loaded to input latches |
| ↑ | X | L | H | data loaded from inputs to shift register |
| no clock edge | X | L | H | data transferred from input flip-flops to shift register |
| X | X | L | L | invalid logic, state of shift register indeterminate when signals removed |
| X | X | H | L | shift register cleared |
| X | ↑ | H | H | shift register clocked $Q_n = Q_{n-1}$, $Q_0 = D_S$ |

Notes

- H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↑ = LOW-to-HIGH CP transition

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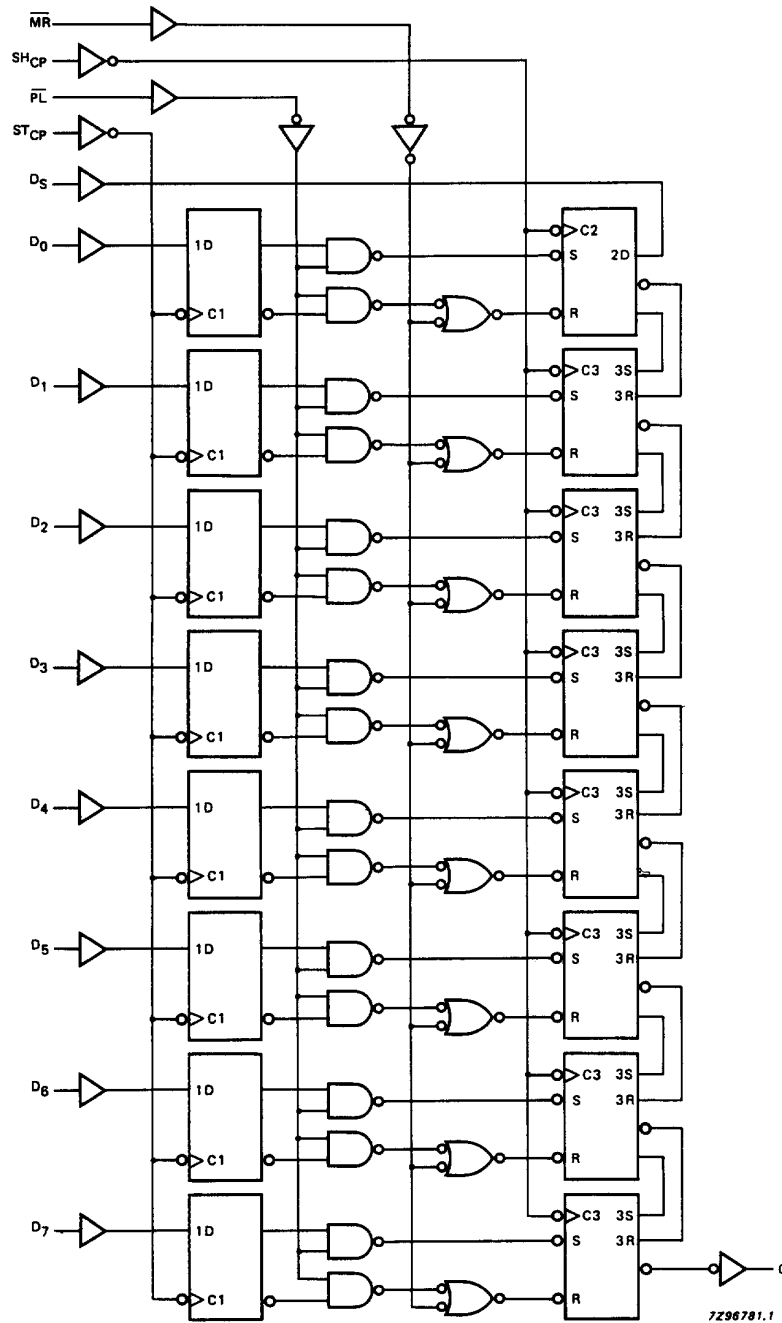


Fig.5 Logic diagram.

8-bit shift register with input flip-flops

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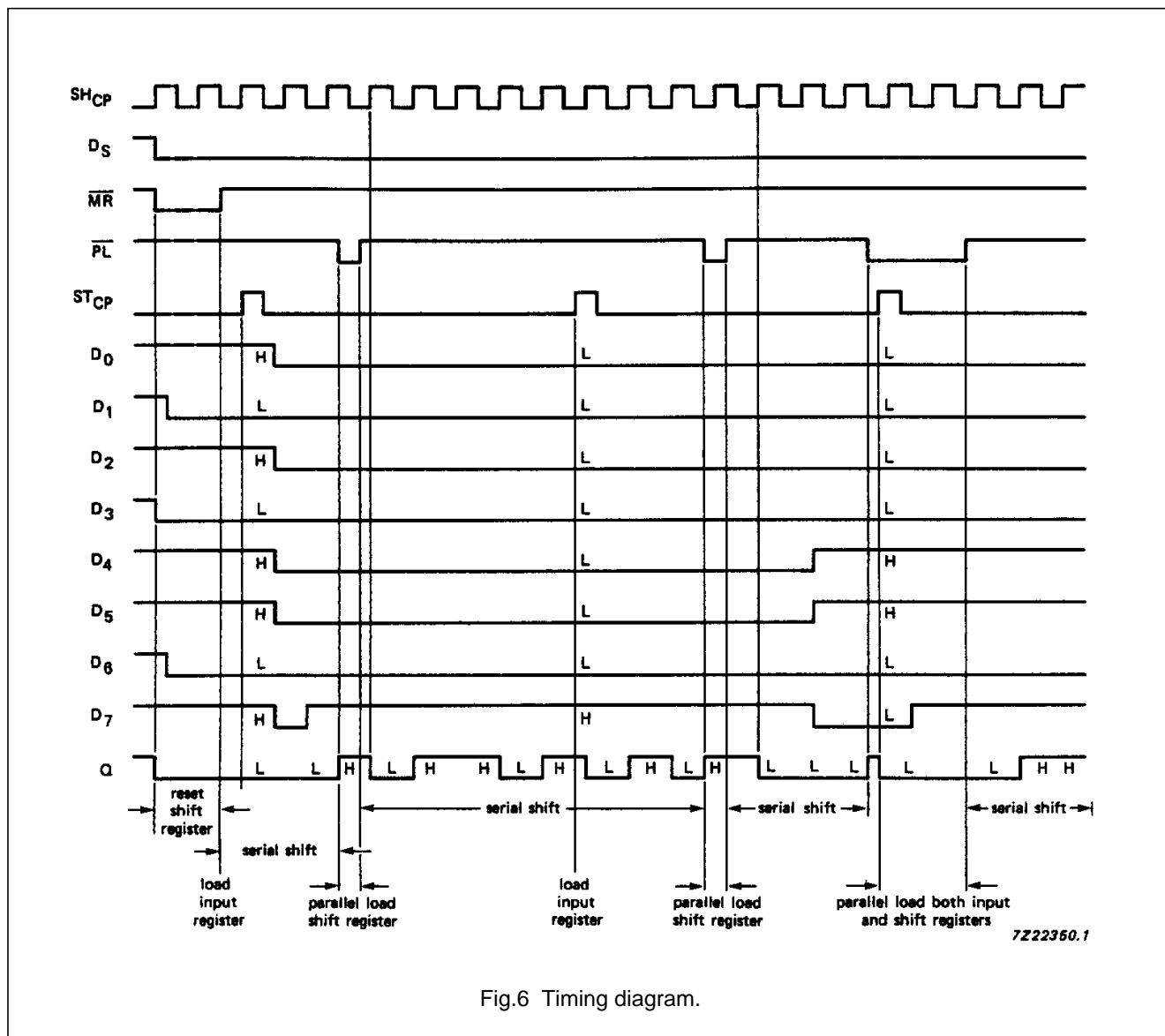


Fig.6 Timing diagram.

8-bit shift register with input flip-flops

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|--------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay SH _{CP} to Q | | 55 20 16 | 175 35 30 | | 220 44 37 | | 265 53 45 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} | propagation delay MR to Q | | 58 21 17 | 175 35 30 | | 220 44 37 | | 265 53 45 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHL} / t _{PLH} | propagation delay ST _{CP} to Q | | 80 29 23 | 250 50 43 | | 315 63 54 | | 375 75 64 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay PL to Q | | 69 25 20 | 215 43 37 | | 270 54 46 | | 325 65 55 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _w | ST _{CP} pulse width HIGH or LOW | 80 16 14 | 11 4 3 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _w | SH _{CP} pulse width HIGH or LOW | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _w | MR pulse width LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| t _w | PL pulse width LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{rem} | removal time MR to SH _{CP} | 60 12 10 | -3 -1 -1 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.10 |
| t _{su} | set-up time D _n to ST _{CP} | 60 12 10 | 8 3 2 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.11 |

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| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|------------------|---|-----------------------|-----------------|------|-----------------|------|-----------------|------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{su} | set-up time D _S to SH _{CP} | 60 12 10 | 11 4 3 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.11 |
| t _{su} | set-up time \overline{PL} to SH _{CP} | 60 12 10 | 11 4 3 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.12 |
| t _h | hold time D _n to ST _{CP} | 5 5 5 | -3 -1 -1 | | 5 5 5 | | 5 5 5 | | ns | 2.0 4.5 6.0 | Fig.11 |
| t _h | hold time \overline{PL} , D _S to SH _{CP} | 5 5 5 | -6 -2 -2 | | 5 5 5 | | 5 5 5 | | ns | 2.0 4.5 6.0 | Fig.11 |
| f _{max} | maximum pulse frequency SH _{CP} | 6.0 30 35 | 29 87 104 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig.7 |

8-bit shift register with input flip-flops**74HC/HCT597**

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-------------------------------------|-----------------------|
| D _S | 0.25 |
| D _n | 0.30 |
| \overline{PL} , \overline{MR} | 1.50 |
| ST _{CP} , SH _{CP} | 1.50 |

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AC WAVEFORMS FOR 74HCT

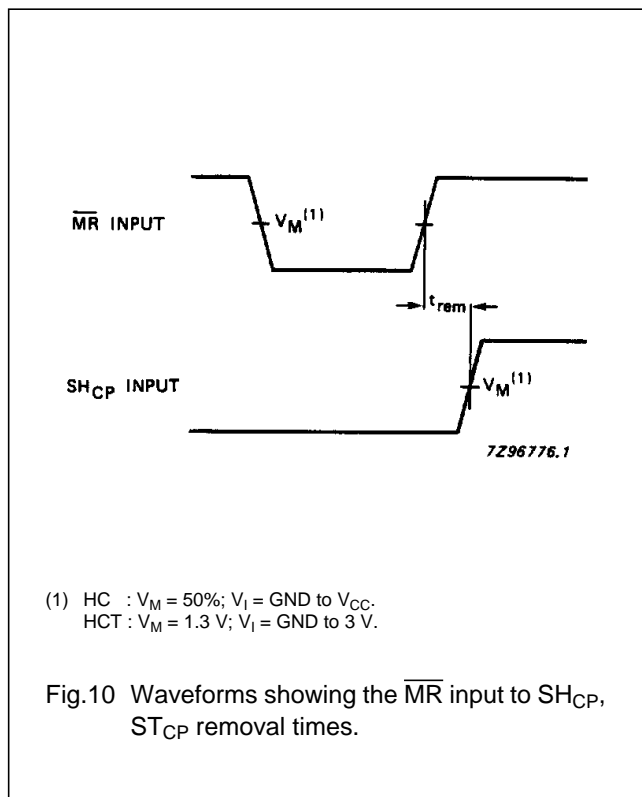
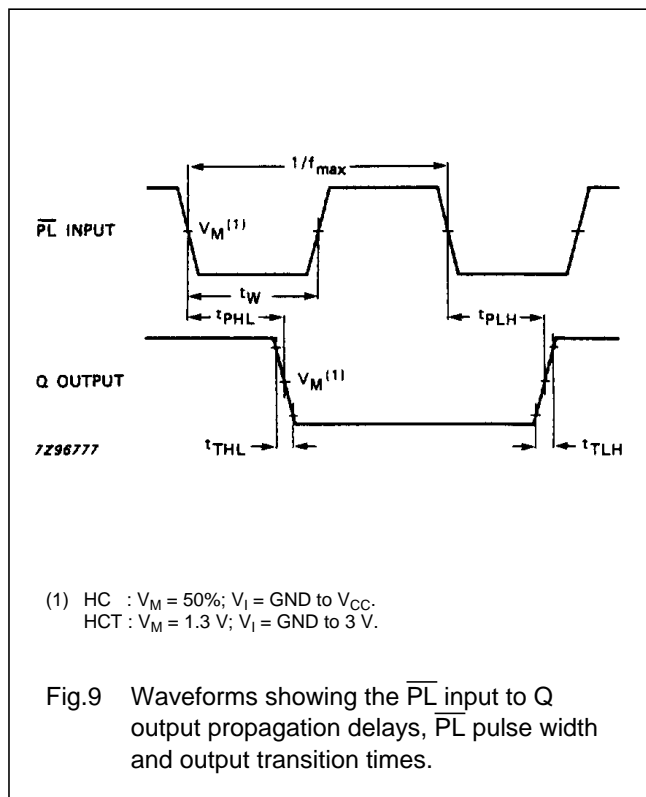
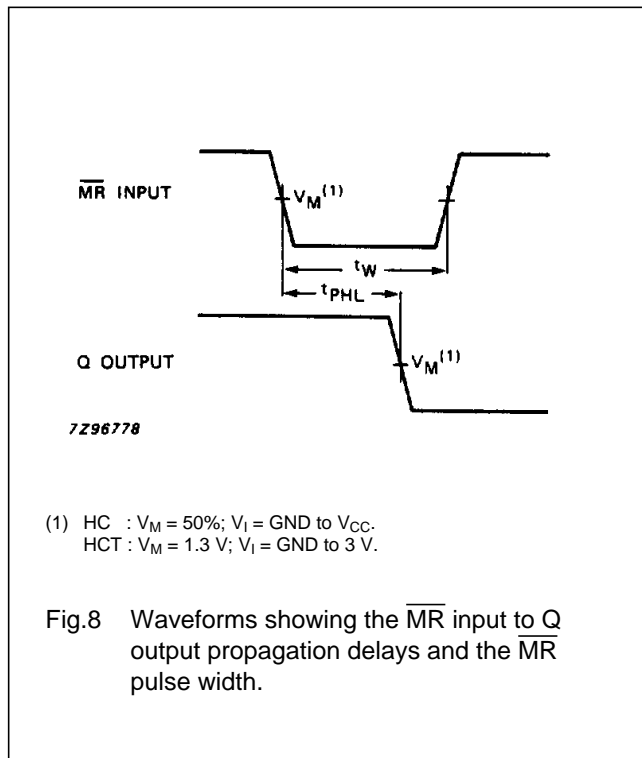
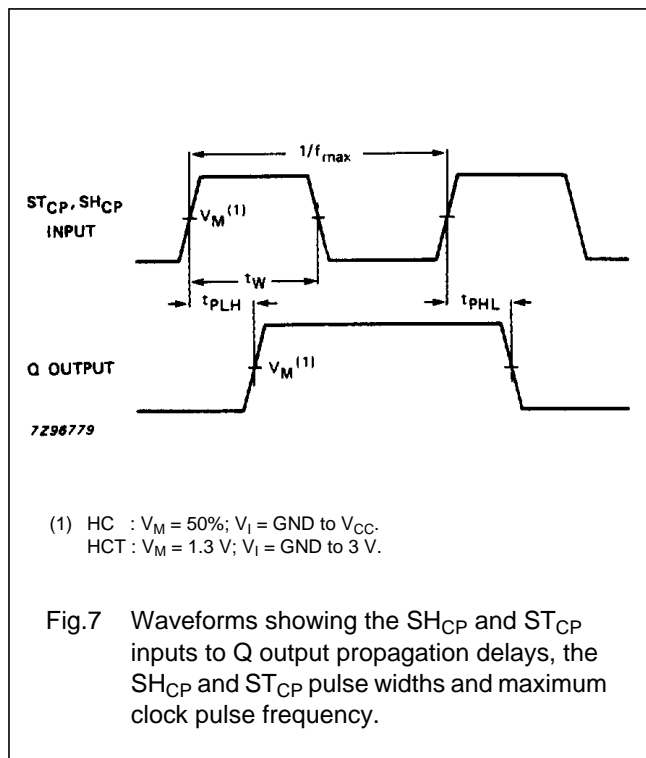
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|-----|------|------------------------|-----------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay SH _{CP} to Q | | 23 | 40 | | 50 | | 60 | ns | 4.5 | Fig.7 | |
| t _{PHL} | propagation delay MR to Q | | 28 | 49 | | 61 | | 74 | ns | 4.5 | Fig.8 | |
| t _{PHL} / t _{PLH} | propagation delay ST _{CP} to Q | | 33 | 57 | | 71 | | 86 | ns | 4.5 | Fig.7 | |
| t _{PHL} / t _{PLH} | propagation delay PL to Q | | 30 | 52 | | 65 | | 78 | ns | 4.5 | Fig.9 | |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.9 | |
| t _w | SH _{CP} pulse width HIGH or LOW | 16 | 7 | | 20 | | 24 | | ns | 4.5 | Fig.7 | |
| t _w | ST _{CP} pulse width HIGH or LOW | 16 | 6 | | 20 | | 24 | | ns | 4.5 | Fig.7 | |
| t _w | $\overline{\text{MR}}$ pulse width LOW | 25 | 14 | | 31 | | 38 | | ns | 4.5 | Fig.8 | |
| t _w | $\overline{\text{PL}}$ pulse width LOW | 20 | 10 | | 25 | | 30 | | ns | 4.5 | Fig.9 | |
| t _{rem} | removal time $\overline{\text{MR}}$ to SH _{CP} | 12 | -2 | | 15 | | 18 | | ns | 4.5 | Fig.10 | |
| t _{su} | set-up time D _n to ST _{CP} | 12 | 5 | | 15 | | 18 | | ns | 4.5 | Fig.11 | |
| t _{su} | set-up time D _S to SH _{CP} | 12 | 2 | | 15 | | 18 | | ns | 4.5 | Fig.11 | |
| t _{su} | set-up time $\overline{\text{PL}}$ to SH _{CP} | 12 | 4 | | 15 | | 18 | | ns | 4.5 | Fig.12 | |
| t _h | hold time D _n to ST _{CP} | 5 | -1 | | 5 | | 5 | | ns | 4.5 | Fig.11 | |
| t _h | hold time $\overline{\text{PL}}$, D _S to SH _{CP} | 5 | -2 | | 5 | | 5 | | ns | 4.5 | Fig.11 | |
| f _{max} | maximum pulse frequency SH _{CP} | 30 | 75 | | 24 | | 20 | | MHz | 4.5 | Fig.7 | |

8-bit shift register with input flip-flops

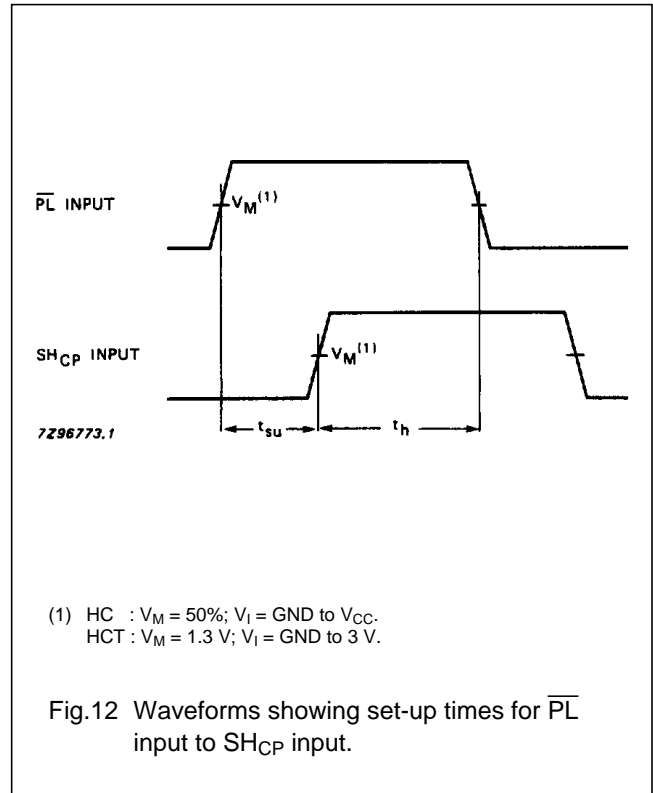
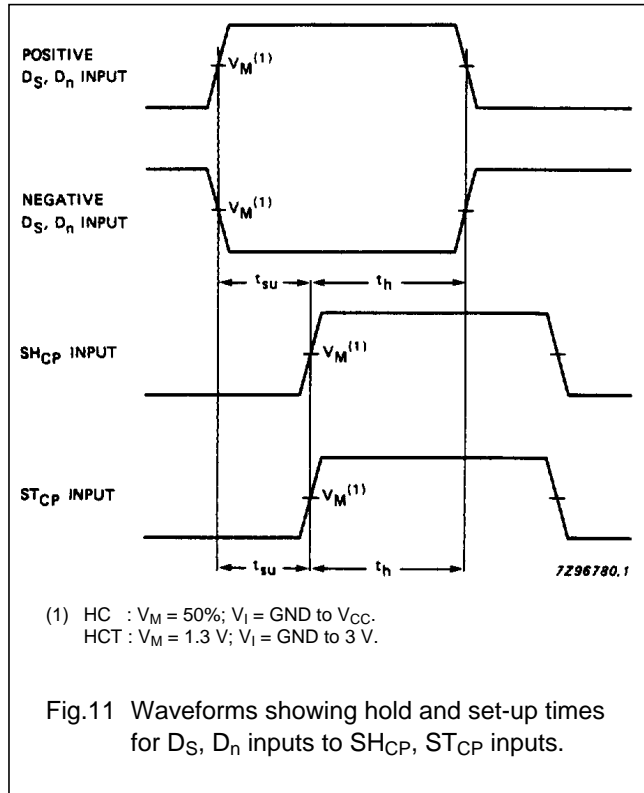
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AC WAVEFORMS



8-bit shift register with input flip-flops

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PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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