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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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8-bit Serial or Parallel-input/Serial-output Shift Register (with 3-state outputs)

RENESAS

ADE-205-511 (Z) 1st. Edition Sep. 2000

Description

The HD74HC589 is similar in function to the HD74HC597, which is not a 3-state device.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output, O_H , is a three-state output, allowing this device to be used in bus-oriented systems.

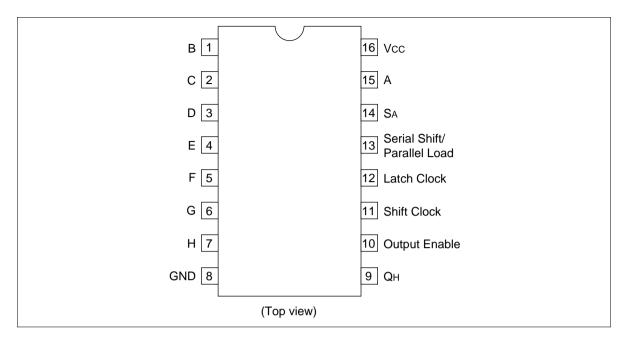
Features

- High Speed Operation: t_{pd} (Shift Clock to Q_H) = 15 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)

Function Table

Latch Clock LCK	Shift Clock SCK	Serial Shift/ Parallel Load	Output Enable	Function
	Х	Х	Х	Data are loaded into input latches
	Х	L	L	Data are loaded from input into shift registers
X	Х	L	L	Data are transfered from input latches to shift registers
L, H, 🔨	L, H, 🔨	Х	Н	Outputs are disabled
Х		Н	L	Serial shift $Q_n = Q_{n-1}, Q_0 = SER$

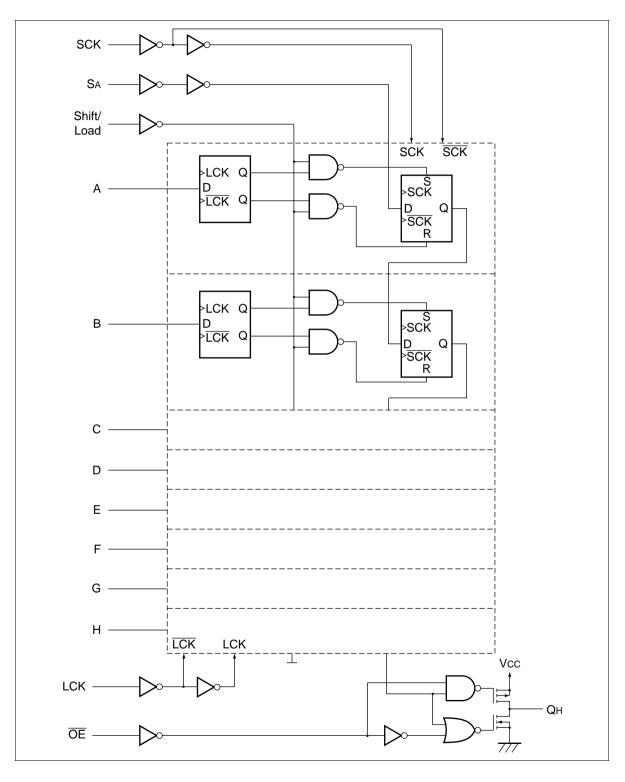
Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V _{cc}	-0.5 to +7.0	V
Input voltage	V _{IN}	–0.5 to V _{cc} + 0.5	V
Output voltage	V _{OUT}	–0.5 to V _{cc} + 0.5	V
Output current	I _{OUT}	±35	mA
DC current drain per V_{cc} , GND	I _{cc} , I _{gnd}	±75	mA
DC input diode current	I _{IK}	±20	mA
DC output diode current	І _{ок}	±20	mA
Power Dissipation per package	P _T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Logic Diagram



RENESAS

DC Characteristics

			Ta =	: 25°C	;	Ta = - +85°C	–40 to C			
ltem	Symbol	V_{cc} (V)	Min	Тур	Мах	Min	Max	Unit	Test Condition	าร
Input voltage	V _{IH}	2.0	1.5	—	_	1.5		V		
		4.5	3.15		—	3.15		_		
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5		0.5	V		
		4.5		_	1.35		1.35	_		
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9		V	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \ \mu A$
		4.5	4.4	4.5	—	4.4		_		
		6.0	5.9	6.0	—	5.9	—	_		
		4.5	4.18		—	4.13		_		I _{OH} = -6 mA
		6.0	5.68	_	—	5.63	—			I _{OH} = -7.8 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \ \mu A$
		4.5	—	0.0	0.1	_	0.1	_		
		6.0		0.0	0.1	_	0.1	_		
		4.5	—	—	0.26	—	0.33			I _{oL} = 6 mA
		6.0	—	—	0.26		0.33			I _{oL} = 7.8 mA
Off-state output current	I _{oz}	6.0	—	—	±0.5	—	±5.0	μA	$Vin = V_{IH} \text{ or } V_{IL},$ Vout = V _{CC} or C	
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V _{cc} or GN	ND
Quiescent supply current	I _{cc}	6.0		_	4.0		40	μA	Vin = V _{cc} or GN	ND, Iout = 0 μ A

			Ta =	: 25°C)	Ta = ∙ +85°0	–40 to C		
ltem	Symbol	V _{cc} (V)	Min	Тур	Мах	Min	Max	Unit	Test Conditions
Maximum clock	f_{max}	2.0	—	—	5		4	MHz	
frequency		4.5	—	—	27	—	21	_	
		6.0	—	—	32	—	25		
Propagation delay	t _{PLH}	2.0	—	—	200	—	250	ns	Latch clock to Q_{\scriptscriptstyleH}
time	t _{PHL}	4.5		20	40		50		
		6.0	—	—	34		43		
	t _{PLH}	2.0		—	175		220	ns	Shift clock to Q_H
	t _{PHL}	4.5	—	15	35	—	44	_	
		6.0	—	—	30	—	37		
	t _{PLH}	2.0	_	_	175		220	ns	Serial shift/prallel load to Q_{H}
	t _{PHL}	4.5	_	16	35		44		
		6.0	_	_	30	_	37	_	
Output enable	t _{zL}	2.0	_	_	150		190	ns	
time	t _{zH}	4.5	_	9	30		38		
		6.0	_	_	26	_	33	_	
Output disable	t_{LZ}	2.0	_	_	150		190	ns	
time	t _{HZ}	4.5	_	14	30		38		
		6.0	—	—	26	—	33		
Pulse width	t _w	2.0	80	_	_	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	_	17	—	_	
Setup time	t _{su}	2.0	100			125		ns	Data to latch clock
		4.5	20	1	_	25	—	_	
		6.0	17	_		21	_		
	t _{su}	2.0	100	_	_	125	—	ns	S _A to shift clock
		4.5	20			25	—	_	
		6.0	17			21	_	_	
	t _{su}	2.0	100	—	—	125	—	ns	Serial shift/parallel load to
		4.5	20			25		_	shift clock
		6.0	17	_	_	21	_		

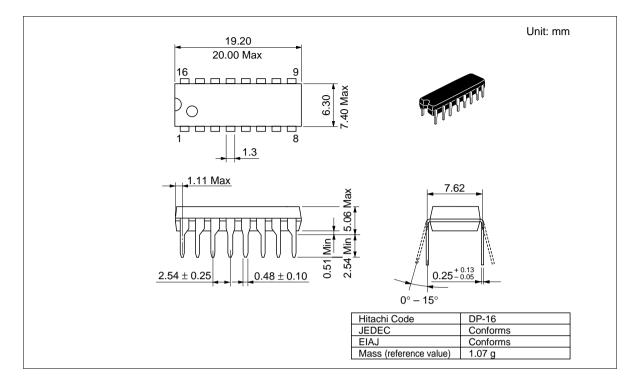
AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

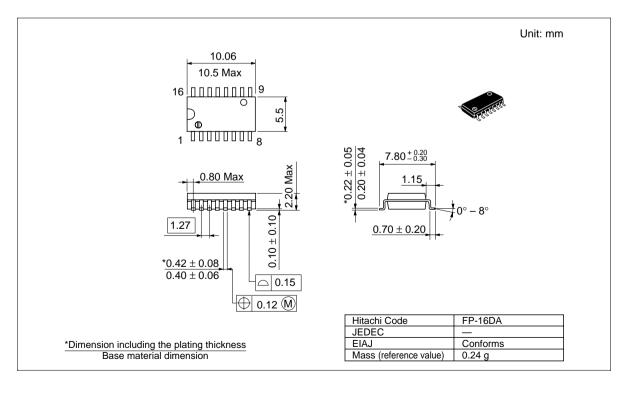


AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$) (cont)

			Та	= 25°C			–40 to		
ltem	Symbol	V _{cc} (V)			, Max	+85°C Min		Unit	Test Conditions
Hold time	t _h	2.0	5		_	5	_	ns	Latch clock to data
		4.5	5	0	—	5	_	-	
		6.0	5	_	_	5	_	-	
	t _h	2.0	5		_	5	_	ns	Shift clock to S _A
		4.5	5		_	5	_	-	
		6.0	5	_	_	5	_	-	
	t _h	2.0	5	_	_	5	_	ns	Shift clock to serial shift/
		4.5	5		_	5	_	_	parallel load
		6.0	5	_	_	5	_	-	
Output rise/fall	t _{TLH}	2.0	_	_	75	—	95	ns	
time	t _{THL}	4.5		5	15	_	19	-	
		6.0	_	—	13	—	16	-	
Input capacitance	Cin	_		5	10	—	10	pF	

Package Dimensions







	Unit: mm
$\begin{array}{c} 9.9\\ 10.3 \text{ Max}\\ 16\\ 10.1 \text{ Max}\\ 16\\ 10.1 \text{ Max}\\ 9\\ 0.635 \text{ Max}\\ 1.27\\ 0.635 \text{ Max}\\ 1.27\\ 0.635 \text{ Max}\\ 1.27\\ 0.635 \text{ Max}\\ 0.15\\ 0.40 \pm 0.06\\ 0.25 \text{ W}\\ \end{array}$	$ \begin{array}{c} & & & \\ & &$
*Dimension including the plating thickness Base material dimension	Hitachi CodeFP-16DNJEDECConformsEIAJConformsMass (reference value)0.15 g

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