

## 74VHC574 • 74VHCT574 Octal D-Type Flip-Flop with TRI-STATE® Outputs

### General Description

The VHC574/VHCT574 is an advanced high speed CMOS octal flip-flop with TRI-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type flip-flop is controlled by a clock input (CP) and an output enable input ( $\overline{OE}$ ). When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V–7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

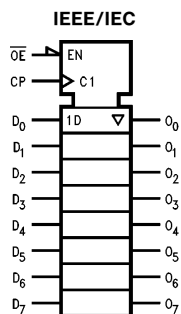
### Features

- High Noise Immunity:  
VHC:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min)  
VHCT:  $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$
  - Power Down Protection:  
VHC: Inputs Only  
VHCT: Inputs and Outputs
  - Low Noise:  
VHC:  $V_{OLP} = 0.6V$  (typ)  
VHCT:  $V_{OLP} = 0.8V$  (typ)
  - Low Power Dissipation:  
 $I_{CC} = 4 \mu A$  (Max) @  $T_A = 25^\circ C$
  - Balanced Propagation Delays:  $t_{PLH} \cong t_{PHL}$
  - Pin and Function Compatible with 74HC/HCT574
- Note:** VHCT specifications are Preliminary.

Commercial	Package Number	Package Description
74VHC574M	M20B	20-Lead Molded JEDEC SOIC
74VHCT574M	M20B	20-Lead Molded JEDEC SOIC
74VHC574SJ	M20D	20-Lead Molded EIAJ SOIC
74VHCT574SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC574MSC	MSC20	20-Lead Molded EIAJ Type 1 SSOP
74VHC574MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHCT574MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHC574N	N20A	20-Lead Molded DIP
74VHCT574N	N20A	20-Lead Molded DIP

**Note:** Surface mount packages are also available on Tape and Reel. EIAJ Type 1 SSOP available on Tape and Reel only, order MSCX. Specify by appending the suffix letter "X" to the ordering code.

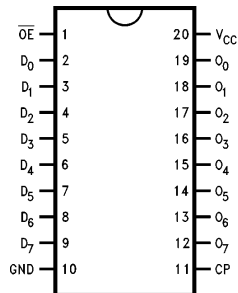
### Logic Symbol



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

### Connection Diagram

Pin Assignment for  
DIP, SSOP, TSSOP and SOIC






Pin Names	Description
$D_0$ – $D_7$	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$O_0$ – $O_7$	TRI-STATE Outputs

## Functional Description

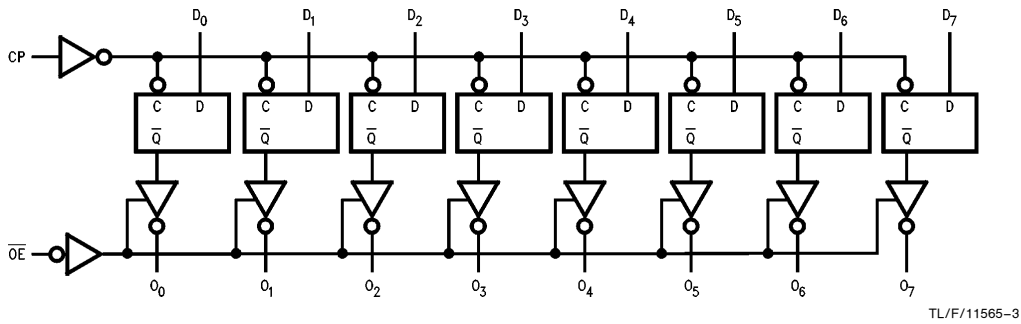
The VHC/VHCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Function Table

Inputs			Outputs
$D_n$	CP	$\overline{OE}$	$O_n$
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 = LOW-to-HIGH Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	
VHC	-0.5V to $V_{CC} + 0.5V$
VHCT*	-0.5V to +7.0V
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current	
(VHC)	$\pm 20$ mA
(VHCT)	-20 mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

\* $V_{OUT} > V_{CC}$  only if output is in H or Z state.

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
VHC	2.0V to +5.5V
VHCT	4.5V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	
VHC/VHCT	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 3.3V \pm 0.3V$ (VHC only)	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

## DC Characteristics for 'VHC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	74VHC				Units	Conditions	
			$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			
			Min	Typ	Max	Min			Max
$V_{IH}$	High Level Input Voltage	2.0 3.0-5.5	1.50 0.7 $V_{CC}$			1.50 0.7 $V_{CC}$	V		
$V_{IL}$	Low Level Input Voltage	2.0 3.0-5.5		0.50 0.3 $V_{CC}$		0.50 0.3 $V_{CC}$	V		
$V_{OH}$	High Level Output Voltage	2.0	1.9	2.0		1.9	V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50 \mu\text{A}$	
		3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4			
		3.0	2.58			2.48	V	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	
		4.5	3.94			3.80			
$V_{OL}$	Low Level Output Voltage	2.0		0.0	0.1		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50 \mu\text{A}$	
		3.0		0.0	0.1				
		4.5		0.0	0.1				
		3.0			0.36		V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	
		4.5			0.36				
$I_{OZ}$	TRI-STATE Output Off-State Current	5.5		$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	
$I_{IN}$	Input Leakage Current	0-5.5		$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5		4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	

## DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74VHC		Units	Conditions
			T <sub>A</sub> = 25°C			
			Typ	Limits		
**V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.0	1.2	V	C <sub>L</sub> = 50 pF
**V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.8	-1.0	V	C <sub>L</sub> = 50 pF
**V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C <sub>L</sub> = 50 pF
**V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C <sub>L</sub> = 50 pF

\*\*Parameter guaranteed by design.

## DC Characteristics for 'VHCT Family Devices (Preliminary)

Symbol	Parameter	V <sub>CC</sub> (V)	74VHCT				Units	Conditions	
			T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min			Max
V <sub>IH</sub>	High Level Input Voltage	4.5 5.5	2.0			2.0 20	V		
V <sub>IL</sub>	Low Level Input Voltage	4.5 5.5		0.8 0.8		0.8 0.8	V		
V <sub>OH</sub>	High Level Output Voltage	4.5	3.15	3.65		3.15	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	
			2.5			2.4	V	I <sub>OH</sub> = -8 μA	
V <sub>OL</sub>	Low Level Output Voltage	4.5	0.0	0.1		0.1	V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	
				0.36		0.44	V	I <sub>OL</sub> = 8 μA	
I <sub>OZ</sub>	TRI-STATE Output Off-State Current	5.5		±0.25		±2.5	μA	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	
I <sub>IN</sub>	Input Leakage Current	0-5.5		±0.1		±1.0	μA	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	5.5		4.0		40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
I <sub>CC(T)</sub>	Maximum I <sub>CC</sub> /Input	5.5		1.35		1.50	mA	V <sub>IN</sub> = 3.4V Other Input = V <sub>CC</sub> or GND	
I <sub>OPD</sub>	Output Leakage Current (Power Down State)	0.0		±0.5		+5.0	μA	V <sub>OUT</sub> = 5.5V	

## DC Characteristics for 'VHCT (Preliminary)

Symbol	Parameter	V <sub>CC</sub> (V)	74VHCT		Units	Conditions
			T <sub>A</sub> = 25°C			
			Typ	Limits		
**V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.2	1.5	V	C <sub>L</sub> = 50 pF
**V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.0	-1.3	V	C <sub>L</sub> = 50 pF
**V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0		2.0	V	C <sub>L</sub> = 50 pF
**V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0		0.8	V	C <sub>L</sub> = 50 pF

\*\*Parameter guaranteed by design.

## AC Electrical Characteristics for 'VHC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74VHC				Units	Conditions	
			T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min			Max
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CP to O <sub>n</sub> )	3.3 ± 0.3	8.5	13.2	1.0	15.5	ns	C <sub>L</sub> = 15 pF	
			11.0	16.7	1.0	19.0		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	5.6	8.6	1.0	10.0	ns	C <sub>L</sub> = 15 pF	
			7.1	10.6	1.0	12.0		C <sub>L</sub> = 50 pF	
t <sub>PZL</sub> t <sub>PZH</sub>	TRI-STATE Output Enable Time	3.3 ± 0.3	8.2	12.8	1.0	15.0	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF	
			10.7	16.3	1.0	18.5		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	5.9	9.0	1.0	10.5	ns	C <sub>L</sub> = 15 pF	
			7.4	11.0	1.0	12.5		C <sub>L</sub> = 50 pF	
t <sub>PLZ</sub> t <sub>PHZ</sub>	TRI-STATE Output Disable Time	3.3 ± 0.3	11.0	15.0	1.0	17.0	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	7.1	10.1	1.0	11.5		C <sub>L</sub> = 50 pF	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 1) C <sub>L</sub> = 50 pF	
		5.0 ± 0.5		1.0		1.0		C <sub>L</sub> = 50 pF	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3 ± 0.3	80	125	65		MHz	C <sub>L</sub> = 15 pF	
			50	75	45			C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	130	180	110			C <sub>L</sub> = 15 pF	
			85	115	75			C <sub>L</sub> = 50 pF	
C <sub>IN</sub>	Input Capacitance		4	10	10	pF	V <sub>CC</sub> = Open		
C <sub>OUT</sub>	Output Capacitance		6			pF	V <sub>CC</sub> = 5.0V		
C <sub>PD</sub>	Power Dissipation Capacitance		28			pF	(Note 2)		

**Note 1:** Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLH</sub> max - t<sub>PLH</sub> min|; t<sub>OSHL</sub> = |t<sub>PHL</sub> max - t<sub>PHL</sub> min|

**Note 2:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub> (opr.) = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/8 (per F/F). The total C<sub>PD</sub> when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C<sub>PD</sub> (total) = 20 + 8n.

## AC Operating Requirements for 'VHC

Symbol	Parameter	V <sub>CC</sub> (V)	74VHC				Units	Conditions	
			T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min			Max
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CP)	3.3 ± 0.3	5.0			5.0		ns	
		5.0 ± 0.5	5.0			5.0			
t <sub>S</sub>	Minimum Set-Up Time	3.3 ± 0.3	3.5			3.5		ns	
		5.0 ± 0.5	3.5			3.5			
t <sub>H</sub>	Minimum Hold Time	3.3 ± 0.3	1.5			1.5			
		5.0 ± 0.5	1.5			1.5			

## AC Electrical Characteristics for 'VHCT Devices (Preliminary)

Symbol	Parameter	V <sub>CC</sub> (V)	74VHCT				Units	Conditions		
			T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C				
			Min	Typ	Max	Min				Max
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time	5.0 ± 0.5	5.6	9.4	1.0	10.5	ns		C <sub>L</sub> = 15 pF	
			6.4	10.4	1.0	11.5			C <sub>L</sub> = 50 pF	
t <sub>PZL</sub> t <sub>PZH</sub>	TRI-STATE Output Enable Time	5.0 ± 0.5	6.5	10.2	1.0	11.5	ns	R <sub>L</sub> = 1 kΩ	C <sub>L</sub> = 15 pF	
			7.3	11.2	1.0	12.5			C <sub>L</sub> = 50 pF	
t <sub>PLZ</sub> t <sub>PHZ</sub>	TRI-STATE Output Disable Time	5.0 ± 0.5	7.0	11.2	1.0	12.0	ns	R <sub>L</sub> = 1 kΩ	C <sub>L</sub> = 50 pF	
t <sub>OSLH</sub> t <sub>OSSL</sub>	Output to Output Skew	5.0 ± 0.5	1.0		1.0		ns	(Note 1)		
f <sub>MAX</sub>	Maximum Clock Frequency	5.0 ± 0.5	90	140	80		MHz		C <sub>L</sub> = 15 pF	
			85	130	75				C <sub>L</sub> = 50 pF	
C <sub>IN</sub>	Input Capacitance		4	10	10		pF	V <sub>CC</sub> = Open		
C <sub>OUT</sub>	Output Capacitance		9				pF	V <sub>CC</sub> = 5.0V		
C <sub>PD</sub>	Power Dissipation Capacitance		27				pF	(Note 2)		

**Note 1:** Parameter guaranteed by design.  $t_{OSLH} = |t_{PLH \max} - t_{PLH \min}|$ ;  $t_{OSSL} = |t_{PHL \max} - t_{PHL \min}|$

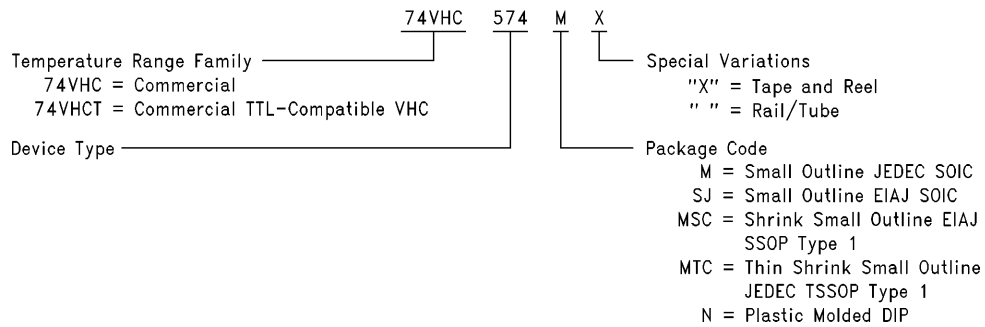
**Note 2:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC (opr.)</sub> = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC/B</sub> (per F/F). The total C<sub>PD</sub> when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C<sub>PD (total)</sub> = 20 + 12n.

## AC Operating Requirements for 'VHCT (Preliminary)

Symbol	Parameter	V <sub>CC</sub> (V)	74VHCT				Units	Conditions	
			T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C			
			Min	Typ	Max	Min			Max
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CP)	5.0 ± 0.5	6.5			6.5		ns	
t <sub>S</sub>	Minimum Set-Up Time	5.0 ± 0.5	2.5			2.5		ns	
t <sub>h</sub>	Minimum Hold Time	5.0 ± 0.5	2.5			2.5			

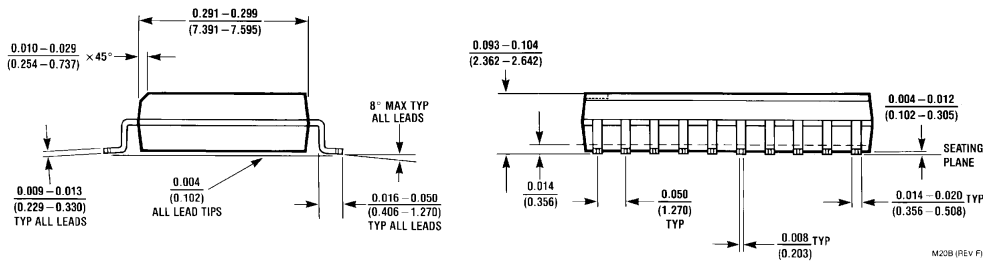
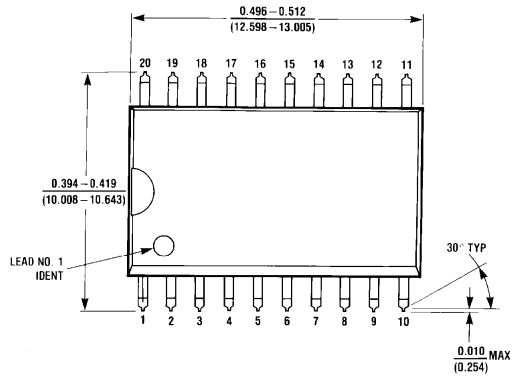
### Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:

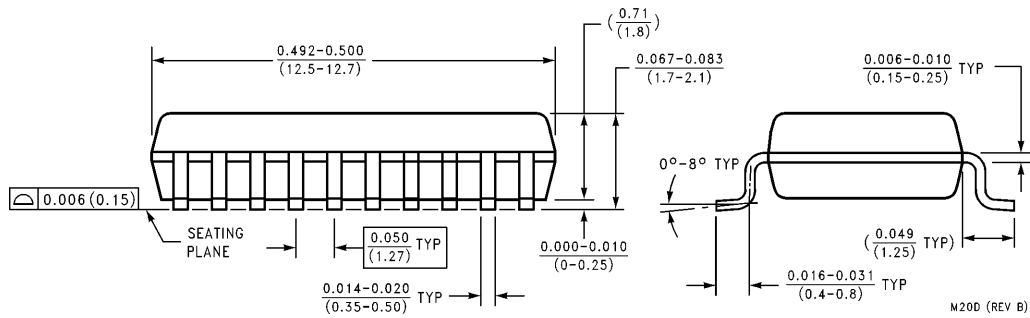
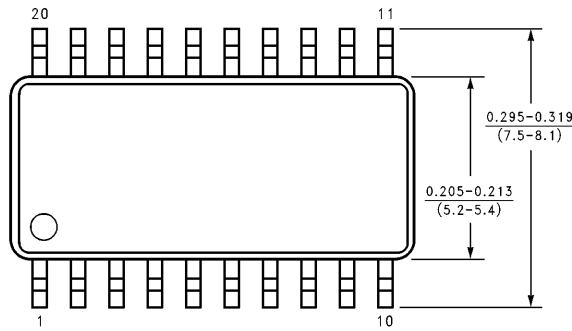


TL/F/11565-5

**Physical Dimensions** inches (millimeters) unless otherwise noted



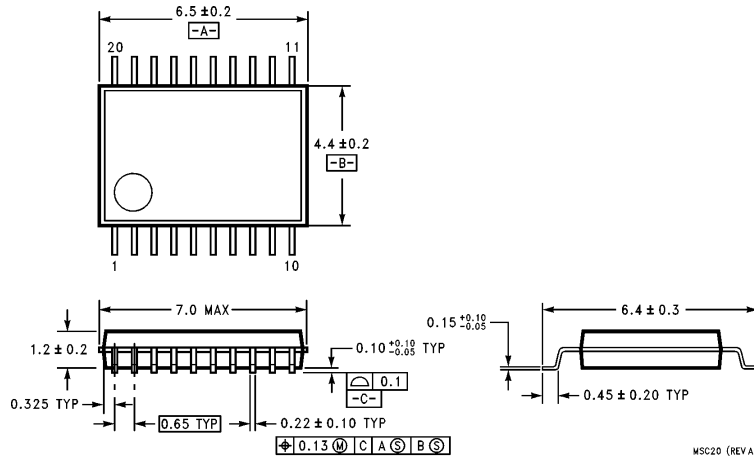
**20-Lead Small Outline Integrated Circuit JEDEC SOIC (M)**  
NS Package Number M20B



**20-Lead Plastic EIAJ SOIC (SJ)**  
NS Package Number M20D

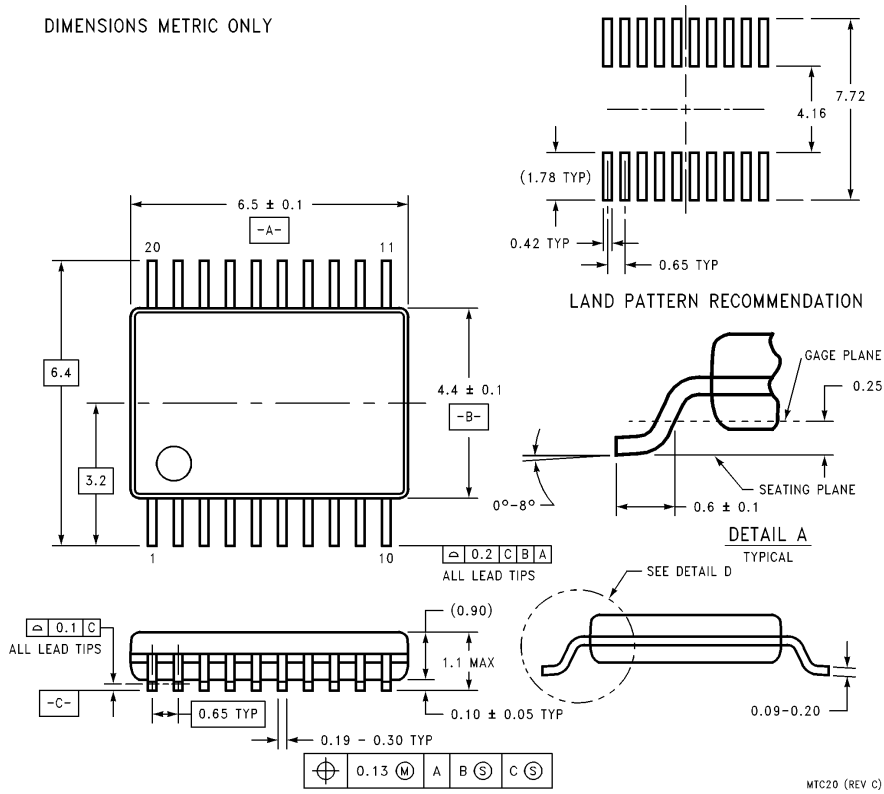


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



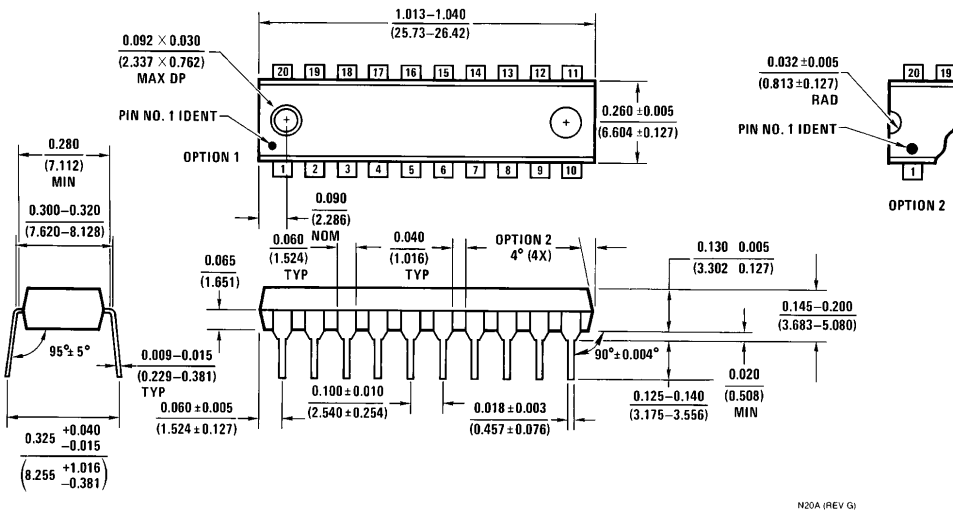
**20-Lead Shrink Small Outline EIAJ SSOP Type 1 (MSC)**  
NS Package Number MSC20

DIMENSIONS METRIC ONLY



**20-Lead Shrink Small Outline JEDEC TSSOP Type 1 (MTC)**  
NS Package Number MTC20

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Molded DIP (N)  
NS Package Number N20A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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