

# 4-Line To 10-Line Decoders (1-of-10)

LS42 LS43 LS44

## FEATURES

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
  - 4-Line to 16-Line Decoders
  - 3-Line to 8-Line Decoders

## DESCRIPTION

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The LS42 BCD-to-decimal decoders, the LS43 excess-3-to-decimal decoders, and the LS44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits.

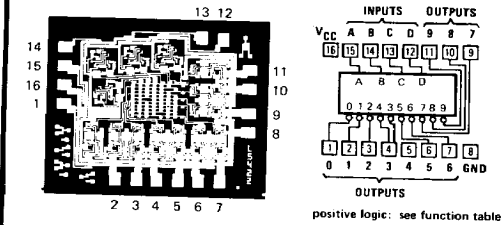
54LS circuits are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; 74LS circuits are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

NO.	LS42 BCD INPUT				LS43 EXCESS-3 INPUT				LS44 EXCESS 3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	L	L	L	H	L	L	L	H	L	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	L	H	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	L	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	L	L	H	L	L	L	H	H	L	H	H	H	H	H	H
5	L	H	L	H	L	L	L	L	L	H	L	L	L	H	H	H	L	H	H	H	H	H
6	L	H	H	L	L	L	L	L	L	H	L	L	L	H	H	H	L	H	H	H	H	H
7	L	H	L	L	L	H	L	H	L	H	L	L	L	H	H	H	L	H	H	H	L	H
8	H	L	L	L	L	H	L	H	L	H	L	L	L	H	H	H	L	H	H	H	H	L
9	H	L	L	H	L	H	L	L	L	H	L	L	L	H	H	H	L	H	H	H	H	L
INVALID	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H

H = high level, L = low level

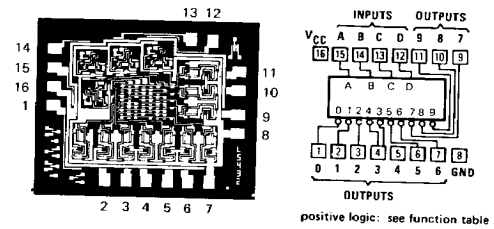
## PIN-OUT DIAGRAM

LS42  
BCD-TO-DECIMAL DECODER



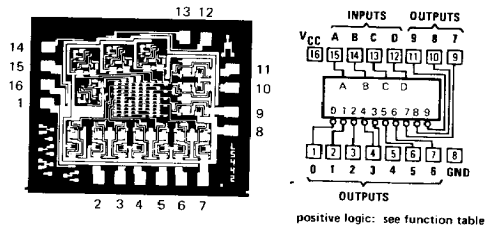
Die Size .077 x .065

LS43  
EXCESS-3-TO-DECIMAL DECODER



Die Size .077 x .065

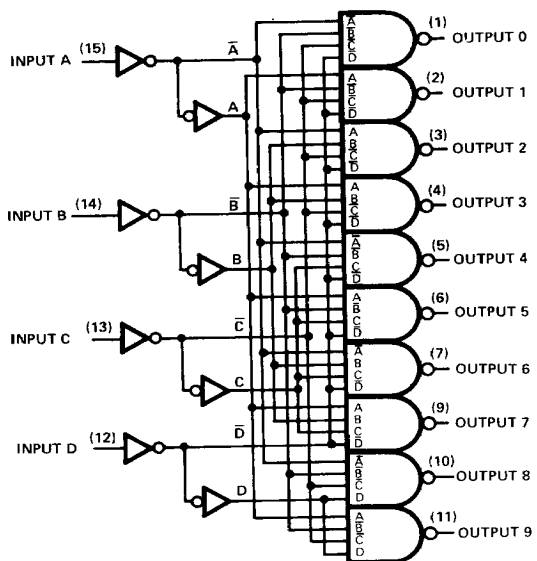
LS44  
EXCESS-3-GRAY-TO-DECIMAL DECODER



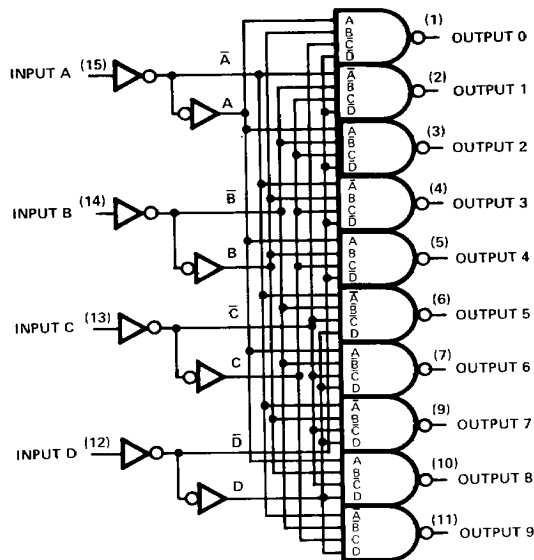
Die Size .077 x .065



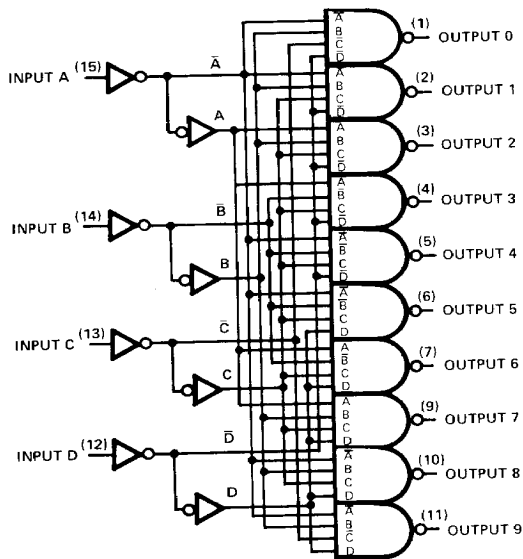
LOGIC DIAGRAMS



LS42  
BCD-TO-DECIMAL DECODERS



LS43  
EXCESS-3-TO-DECIMAL DECODERS



LS44  
EXCESS-3-GRAY-TO-DECIMAL-DECODERS

# 4-Line To 10-Line Decoders (1-of-10)

LS42 LS43 LS44

## Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*	9LS/54LS			9LS/74LS			Unit
		Min	Typ**	Max	Min	Typ**	Max	
$V_{IH}$		2			2			V
$V_{IL}$				0.7			0.8	V
$V_I$	$V_{CC}=\text{MIN}, I_I=-18\text{mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC}=\text{MIN}, V_{IH}=2\text{V}, V_{IL}=V_{IL\text{max}}, I_{OH}=-400\mu\text{A}$	2.5	3.5		2.7	3.5		V
$V_{OL}$	$V_{CC}=\text{MIN}, V_{IH}=2\text{V}, V_{IL}=V_{IL\text{max}}$		0.25	0.4		0.25	0.4	V
$I_I$	$V_{CC}=\text{MAX}, V_I=7\text{V}$			0.1		0.1		mA
$I_{IH}$	$V_{CC}=\text{MAX}, V_I=2.7\text{V}$			20		20		$\mu$ A
$I_{IL}$	$V_{CC}=\text{MAX}, V_I=0.4\text{V}$			-0.4		-0.4		mA
$I_{OS}^{\dagger}$	$V_{CC}=\text{MAX}$	-15		-100	-15		-100	mA
$I_{CC}^{\ddagger\dagger}$	$V_{CC}=\text{MAX}$		7	13		7	13	mA

\*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\*All typical values are at  $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$ .

$\dagger$ Not more than one output should be shorted at a time.

$\ddagger\dagger I_{CC}$  is measured with all outputs open and inputs grounded.

## Switching Characteristics, $V_{CC} = 5\text{V}$ Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	$-55^{\circ}\text{C}$			$+25^{\circ}\text{C}$			$+125^{\circ}\text{C}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>Test Conditions: <math>C_L = 15\text{pF}, R_L = 2\text{k}\Omega</math> (See Fig. A, page 2-174)</b>												
$t_{PHL}$	A,B,C or D	Any output 2 gate delay		15	26		14	25		15	26	ns
$t_{PHL}$	A,B,C or D	Any Output 3 gate delay		17	31		17	30		18	31	ns
$t_{PLH}$	A,B,C or D	Any output 2 gate delay		11	27		10	25		11	26	ns
$t_{PLH}$	A,B,C or D	Any output 3 gate delay		22	35		17	30		20	34	ns
<b>Test Conditions: <math>C_L = 50\text{pF}, R_L = 2\text{k}\Omega</math> (See Fig. A, page 2-174)</b>												
$t_{PHL}$	A,B,C or D	Any Output 2 gate delay		18	32		18	31		19	33	ns
$t_{PHL}$	A,B,C or D	Any Output 3 gate delay		21	35		22	35		23	36	ns
$t_{PHL}$	A,B,C or D	Any Output 2 gate delay		21	33		20	32		21	33	ns
$t_{PLH}$	A,B,C or D	Any Output 3 gate delay		29	36		25	38		28	40	ns

Note: AC specification shown under  $-55^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  are for 9LS devices only. All 50pF specifications are for 9LS only.

