

MC74AC4040

12-Stage Binary Ripple Counter

The MC74AC4040 consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4040 for some designs.

Features

- 140 MHz Typ. Clock
- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity
- Pb-Free Packages are Available

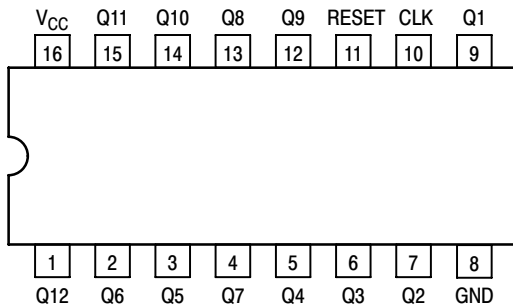


Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

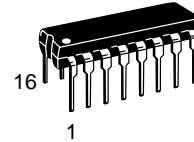
FUNCTION TABLE

| Clock | Reset | Output State |
|-------|-------|-----------------------|
| | L | No Change |
| | L | Advance to next state |
| X | H | All Outputs are low |

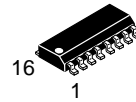


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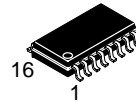
<http://onsemi.com>



PDIP-16
N SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



SOEIAJ-16
M SUFFIX
CASE 966

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-------------------|------------------|
| MC74AC4040N | PDIP-16 | 25 Units/Rail |
| MC74AC4040NG | PDIP-16 (Pb-Free) | 25 Units/Rail |
| MC74AC4040D | SOIC-16 | 48 Units/Rail |
| MC74AC4040DG | SOIC-16 (Pb-Free) | 48 Units/Rail |
| MC74AC4040DR2 | SOIC-16 | 2500 Tape & Reel |
| MC74AC4040DR2G | SOIC-16 (Pb-Free) | 2500 Tape & Reel |
| MC74AC4040M | SOEIAJ-16 | 50 Units/Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 4 of this data sheet.

MC74AC4040

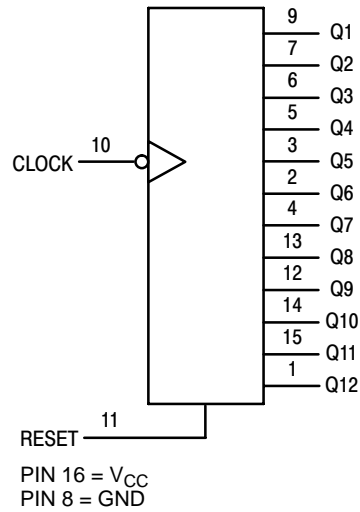


Figure 2. Logic Diagram

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Current, per Pin | ± 50 | mA |
| I_{CC} | DC V_{CC} or GND Current per Output Pin | ± 50 | mA |
| P_D | Power Dissipation in Still Air Plastic† SOIC Package† | 750 500 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 seconds (Plastic DIP or SOIC Package) | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating: Plastic DIP: - 10mW/°C from 65°C to 125°C SOIC Package: -7.0 mW/°C from 65°C to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------|---|-----|-----------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{IN}/V_{OUT} | Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | - |
| T_A | Operating Temperature, All Package Types | -40 | +85 | °C |
| t_r/t_f | Input Rise/Fall Time (Figure 1) $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 5.5\text{ V}$ | 0 | 150 40 25 | ns/V |

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DC CHARACTERISTICS (unless otherwise specified)

| Symbol | Parameter | Value | Unit | |
|----------|----------------------------------|-------|---------|---|
| I_{CC} | Maximum Quiescent Supply Voltage | 80 | μA | $V_{in} = V_{CC}$ or GND $V_{CC} = 5.5 V, T_A = \text{Worst Case}$ |
| I_{CC} | Maximum Quiescent Supply Current | 8.0 | μA | $V_{in} = V_{CC}$ or GND $V_{CC} = 5.5 V, T_A = 25^\circ C$ |

DC CHARACTERISTICS

| Symbol | Parameter | V_{CC} (V) | 74AC | | 74AC | | Unit | Conditions |
|-----------|-----------------------------------|-----------------|---------------------|-------------------|--------------------------------------|--|---------|--|
| | | | $T_A = +25^\circ C$ | | $T_A = -40^\circ C$ to $+85^\circ C$ | | | |
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum High Level Input Voltage | 3.0 | – | 2.1 | 2.1 | | V | $V_{OUT} = 0.1 V$ or $V_{CC} - 0.1 V$ |
| | | 4.5 | – | 3.15 | 3.15 | | | |
| | | 5.5 | – | 3.85 | 3.85 | | | |
| V_{IL} | Maximum Low Level Input Voltage | 3.0 | – | 0.9 | 0.9 | | V | $V_{OUT} = 0.1 V$ or $V_{CC} - 0.1 V$ |
| | | 4.5 | – | 1.35 | 1.35 | | | |
| | | 5.5 | – | 1.65 | 1.65 | | | |
| V_{OH} | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | | V | $I_{OUT} = -50 \mu A$ |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | – | 2.56 | 2.46 | | V | * $V_{IN} = V_{IL}$ or V_{IH} –12 mA I_{OH} –24 mA –24 mA |
| | | 4.5 | – | 3.86 | 3.76 | | | |
| | | 5.5 | – | 4.86 | 4.76 | | | |
| V_{OL} | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | | V | $I_{OUT} = 50 \mu A$ |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | – | 0.36 | 0.44 | | V | * $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA |
| | | 4.5 | – | 0.36 | 0.44 | | | |
| | | 5.5 | – | 0.36 | 0.44 | | | |
| I_{IN} | Maximum Input Leakage Current | 5.5 | – | ± 0.1 | ± 1.0 | | μA | $V_I = V_{CC}, GND$ |
| I_{OLD} | Minimum Dynamic Output Current† | 5.5 | – | – | 75 | | mA | $V_{OLD} = 1.65 V \text{ Max}$ |
| I_{OHD} | | 5.5 | – | – | –75 | | mA | $V_{OHD} = 3.85 V \text{ Min}$ |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

| Symbol | Parameter | V _{CC} * (V) | 74AC | | | 74AC | | Unit | Fig. No. |
|---|--|--------------------------|--|--------------|------------|---|------------|------|----------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | | |
| | | | Min | Typ | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 110 130 | 120 140 | – – | 100 120 | – – | MHz | – |
| t _{CP} to Q1 | Propagation Delay n _{CP} to Q1 | 3.3 5.0 | 2.0 2.0 | – – | 11 8.0 | 2.0 2.0 | 14 10 | ns | – |
| Q _n to Q _n +1 | Propagation Delay Q _n to Q _n +1 | 3.3 5.0 | 0 0 | – – | 5.5 3.5 | 0 0 | 6.5 4.5 | ns | – |
| MR to Q t _{HL} | Propagation Delay MR to Q | 3.3 5.0 | 3.0 3.0 | – – | 12 10 | 3.0 3.0 | 15 12 | ns | – |
| t _{rec} n _{CP} to MR | Recovery Time | 3.3 5.0 | 0 0 | -2.5 -1.5 | – – | 0 0 | – – | ns | – |
| t _w n _{CP} | Minimum Pulse Width Clock Pin | 3.3 5.0 | 4.0 3.0 | 3.5 2.5 | – – | 4.5 3.5 | – – | ns | – |
| t _w MR | Minimum Pulse Width Master Reset | 3.3 3.0 | 4.0 3.0 | 3.5 2.5 | – – | 4.5 3.5 | – – | ns | – |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

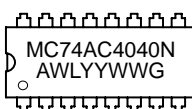
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|-----------------|-------------------------------|--------------|------|-------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0 V |
| C _{PD} | Power Dissipation Capacitance | 50 | pF | V _{CC} = 5.0 V |

MARKING DIAGRAMS

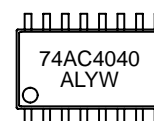
PDIP-16



SOIC-16



SOEIAJ-16

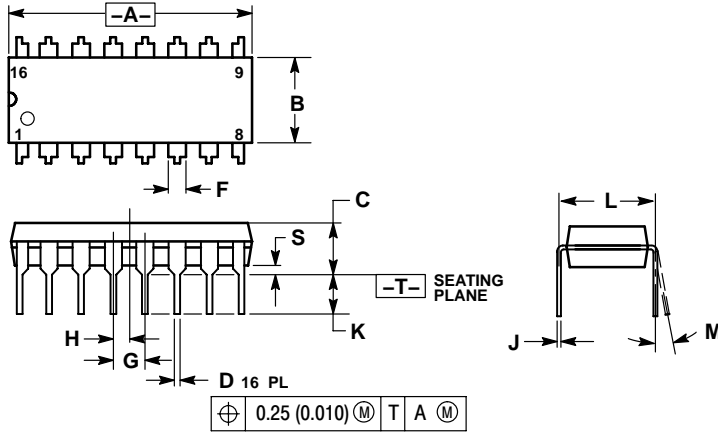


A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package

MC74AC4040

PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° 10° | | 0° 10° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

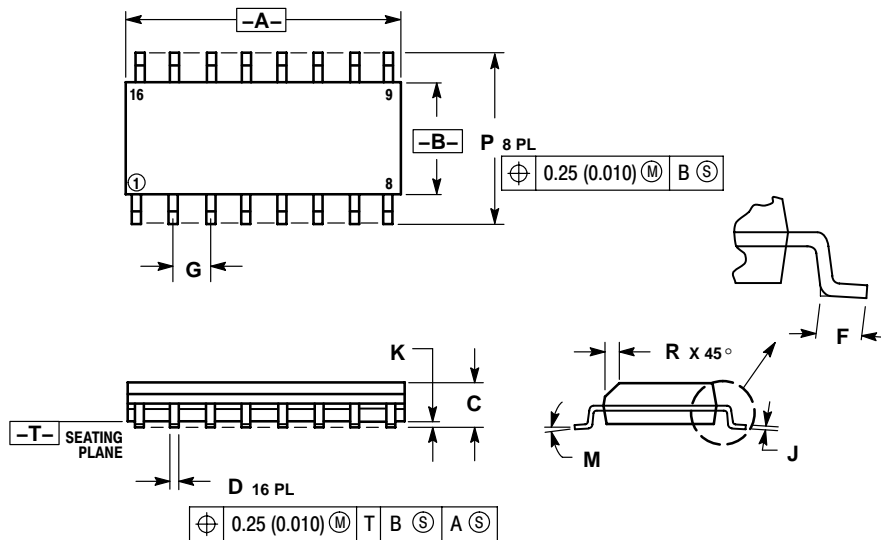
STYLE 1:

- PIN 1. CATHODE
- PIN 2. CATHODE
- PIN 3. CATHODE
- PIN 4. CATHODE
- PIN 5. CATHODE
- PIN 6. CATHODE
- PIN 7. CATHODE
- PIN 8. CATHODE
- PIN 9. ANODE
- PIN 10. ANODE
- PIN 11. ANODE
- PIN 12. ANODE
- PIN 13. ANODE
- PIN 14. ANODE
- PIN 15. ANODE
- PIN 16. ANODE

STYLE 2:

- PIN 1. COMMON DRAIN
- PIN 2. COMMON DRAIN
- PIN 3. COMMON DRAIN
- PIN 4. COMMON DRAIN
- PIN 5. COMMON DRAIN
- PIN 6. COMMON DRAIN
- PIN 7. COMMON DRAIN
- PIN 8. COMMON DRAIN
- PIN 9. GATE
- PIN 10. SOURCE
- PIN 11. GATE
- PIN 12. SOURCE
- PIN 13. GATE
- PIN 14. SOURCE
- PIN 15. GATE
- PIN 16. SOURCE

SOIC CASE 751B-05 ISSUE J



NOTES:

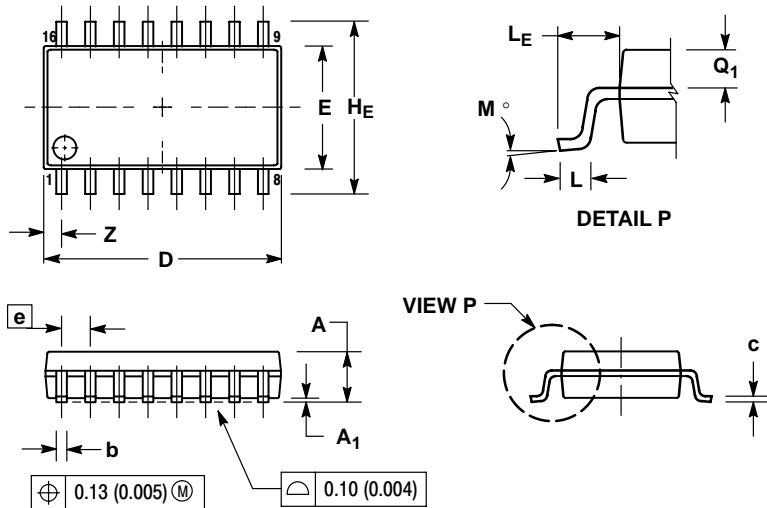
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° 7° | | 0° 7° | |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC74AC4040

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

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