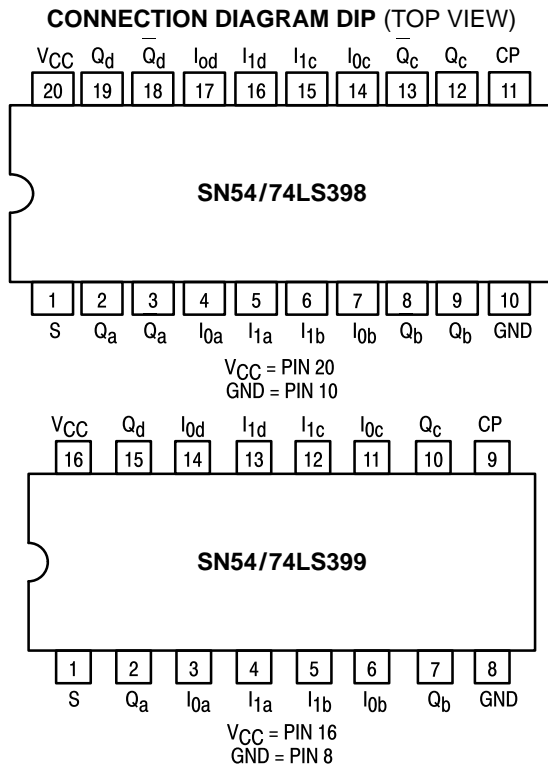




# QUAD 2-PORT REGISTER

The SN54/74LS398 and SN54/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The SN54/74LS398 features both Q and  $\bar{Q}$  inputs, while the SN54/74LS399 has only Q outputs.

- Select From Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complemented Outputs on SN54/74LS398
- Input Clamp Diodes Limit High-Speed Termination Effects



## PIN NAMES

S	Common Select Input
CP	Clock (Active HIGH Going Edge) Input
$I_{0a}-I_{0d}$	Data Inputs From Source 0
$I_{1a}-I_{1d}$	Data Inputs From Source 1
$Q_a-\bar{Q}_d$	Register True Outputs (Note b)
$Q_a-Q_d$	Register Complementary Outputs (Note b)

## LOADING (Note a)

	HIGH	LOW
S	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{0d}$	0.5 U.L.	0.25 U.L.
$I_{1a}-I_{1d}$	0.5 U.L.	0.25 U.L.
$Q_a-\bar{Q}_d$	10 U.L.	5 (2.5) U.L.
$Q_a-Q_d$	10 U.L.	5 (2.5) U.L.

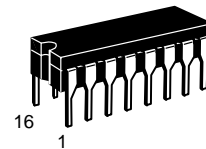
## NOTES:

- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

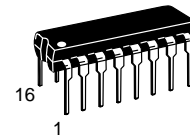
## SN54/74LS398 SN54/74LS399

### QUAD 2-PORT REGISTER

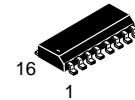
#### LOW POWER SCHOTTKY



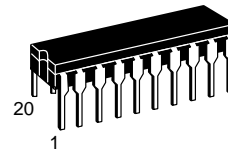
**J SUFFIX**  
CERAMIC  
CASE 620-09



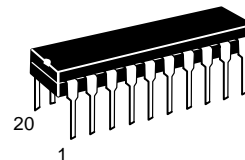
**N SUFFIX**  
PLASTIC  
CASE 648-08



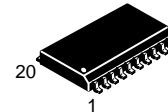
**D SUFFIX**  
SOIC  
CASE 751B-03



**J SUFFIX**  
CERAMIC  
CASE 732-03



**N SUFFIX**  
PLASTIC  
CASE 738-03



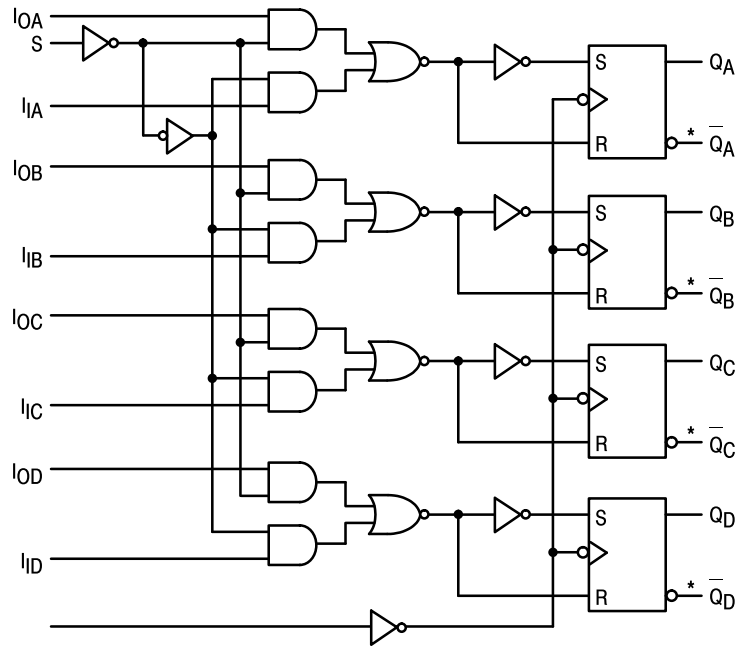
**DW SUFFIX**  
SOIC  
CASE 751D-03

## ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC
SN74LSXXXD	SOIC

# SN54/74LS398 • SN54/74LS399

## FUNCTIONAL BLOCK DIAGRAM



\* SN54/74LS398 only

## FUNCTIONAL DESCRIPTION

The SN54/74LS398 and SN54/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock in-

put (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The SN54/74LS398 has both Q and Q Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I <sub>0</sub>	I <sub>1</sub>	Q	Q*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

\*SN54/74LS398 only

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial

# SN54/74LS398 • SN54/74LS399

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			13	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output Q		18 21	27 32	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF

# SN54/74LS398 • SN54/74LS399

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock Pulse Width	20			ns	$V_{CC} = 5.0\text{ V}$
$t_S$	Data Setup Time	25			ns	
$t_S$	Select Setup Time	45			ns	
$t_H$	Hold Time, Any Input	0			ns	

## DEFINITIONS OF TERMS

SETUP TIME ( $t_S$ ) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME ( $t_H$ ) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

## AC WAVEFORMS

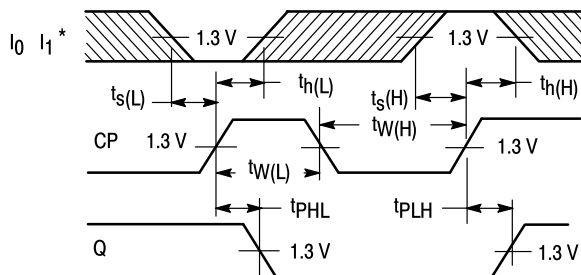


Figure 1

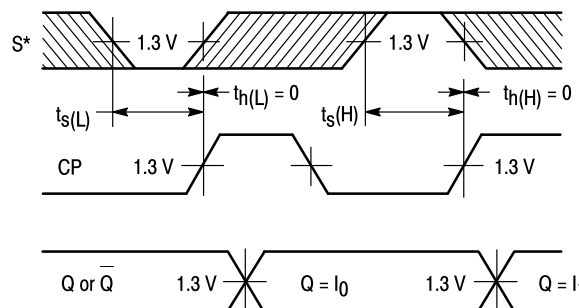


Figure 2

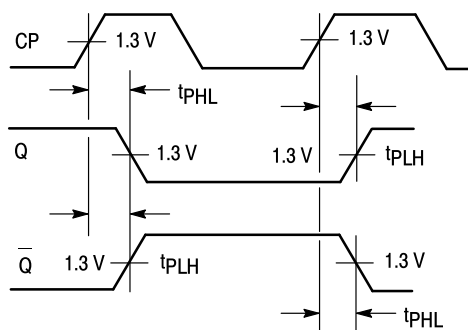
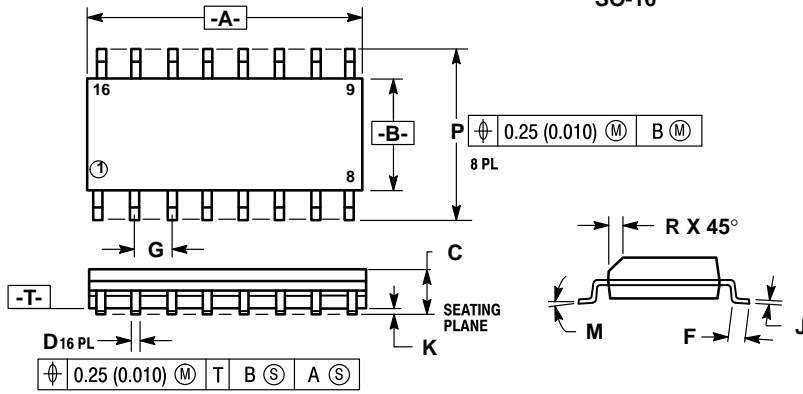


Figure 3

\*The shaded areas indicate when the input is permitted to change for predictable output performance.

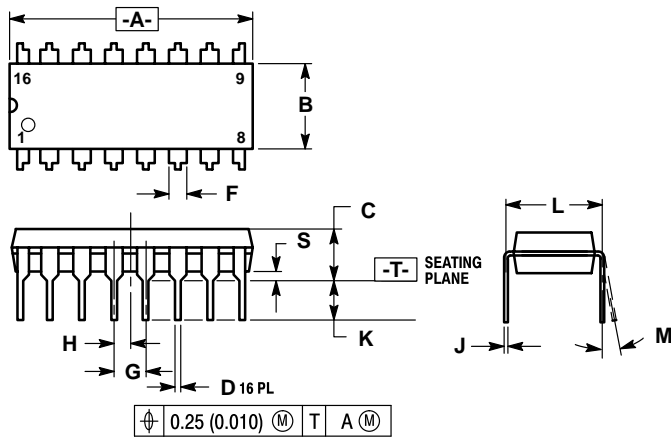
**Case 751B-03 D Suffix  
16-Pin Plastic  
SO-16**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

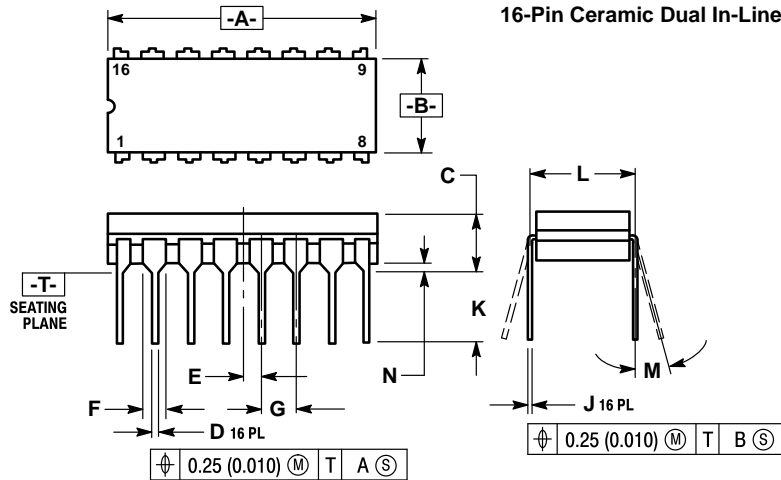
**Case 648-08 N Suffix  
16-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.
  6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

**Case 620-09 J Suffix  
16-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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