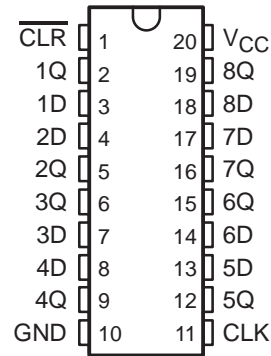


SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

SCBS185B – FEBRUARY 1991 – REVISED JANUARY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

SN54ABT273 . . . J OR W PACKAGE
SN74ABT273 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

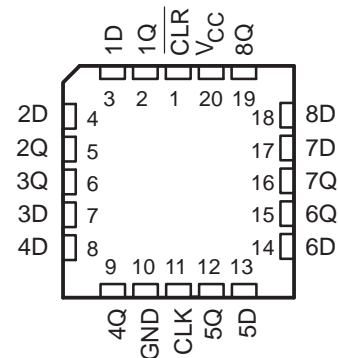


description

The 'ABT273 are 8-bit positive-edge-triggered D-type flip-flops with a direct clear (CLR) input. They are particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D input signal has no effect at the output.

SN54ABT273 . . . FK PACKAGE
(TOP VIEW)



The SN54ABT273 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT273 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q_0



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

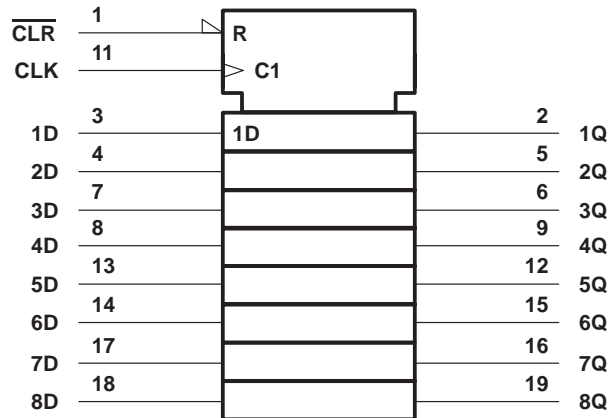
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SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

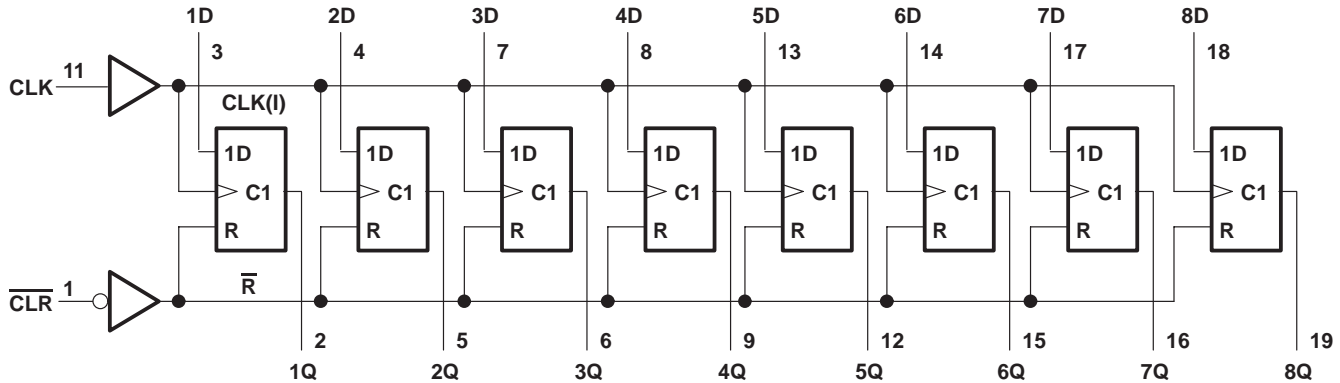
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT273	96 mA
SN74ABT273	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions (see Note 3)

		SN54ABT273		SN74ABT273		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT273		SN74ABT273		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2			
I _{OH} = -32 mA		2*					2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*			0.55		
V _{hys}			100						mV
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	μA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-200§	-50	-200§	-50	-200§	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1	400§	400§		400§	μA
		Outputs low		24	30	30		30	mA
ΔI _{CC¶}	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This data sheet limit may vary among suppliers.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT273		SN74ABT273		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	MHz
t _w	Pulse duration	CLK high or low	3.3	3.3	3.3	3.3	3.3	ns
		$\overline{\text{CLR}}$ low	3.3	3.3	3.3	3.3		
t _{su}	Setup time before CLK↑	Data high	2	2	2	2	ns	
		Data low	2.5	2.5	2.5	2.5		
		$\overline{\text{CLR}}$ high	2	2	2	2		
t _h	Hold time after CLK↑	Data high or low	1.2†	1.4†	1.2†	1.2†	ns	

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C		SN54ABT273		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
t _{PLH}	CLK	Q	2.5	6	2.5	7	ns
t _{PHL}			3.3	6.8	3.3	7.5	
t _{PHL}	$\overline{\text{CLR}}$	Q	2.5	7.5†	2.5	8.2	ns

† This data sheet limit may vary among suppliers.

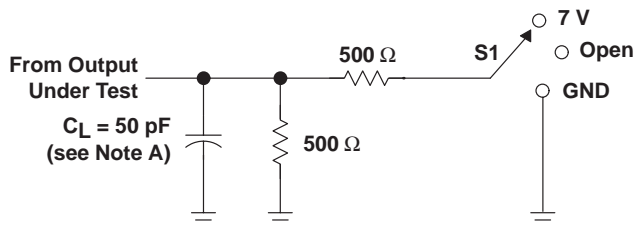
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C		SN74ABT273		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
t _{PLH}	CLK	Q	2.5	6	2.5	6.5	ns
t _{PHL}			3.3	6.8	3.3	7.3	
t _{PHL}	$\overline{\text{CLR}}$	Q	2.5	6.7†	2.5	7.4†	ns

† This data sheet limit may vary among suppliers.

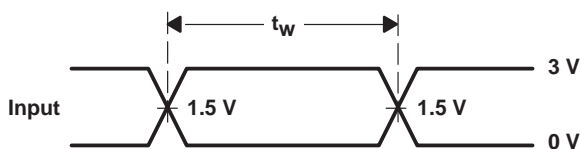


PARAMETER MEASUREMENT INFORMATION

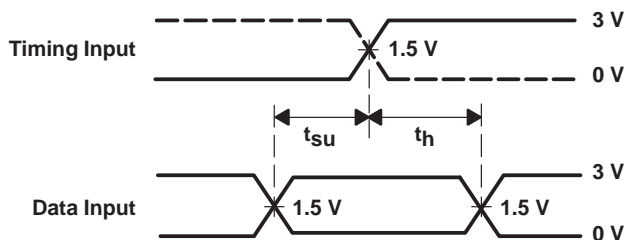


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

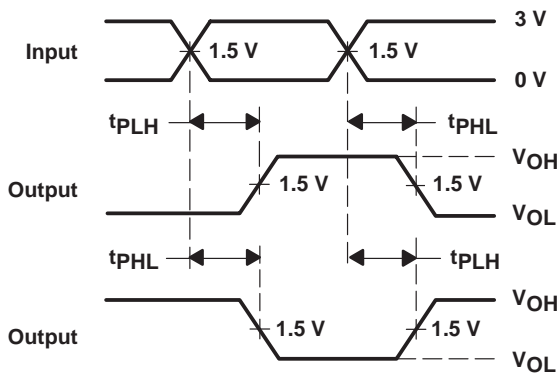
LOAD CIRCUIT



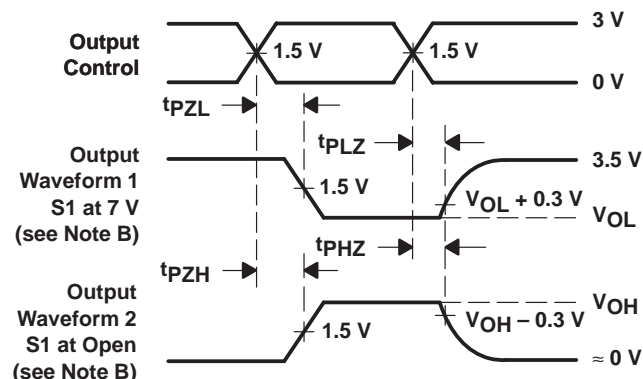
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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