2-Bit By 4-Bit Parallel Binary Multipliers

FEATURES

- Fast Multiplication . . . 5-Bit Product in 26ns Typ
- Power Dissipation . . . 110mW Typical
- Latch Outputs for Synchronous Operation
- Expandable for m-Bit-by-n-Bit Applications
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families
- Diode-Clamped Inputs Simplify System Design

DESCRIPTION

These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

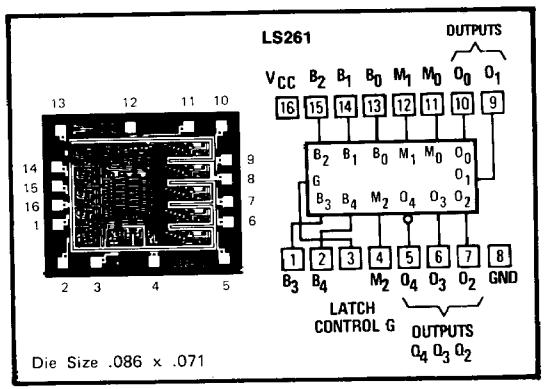
The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most-significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

The 9LS/54L261 is characterized for operation over the full military temperature range of −55°C to 125°C; the 9LS/74LS261 for operation from 0°C to 70°C.

PIN-OUT DIAGRAM



FUNCTION TABLE

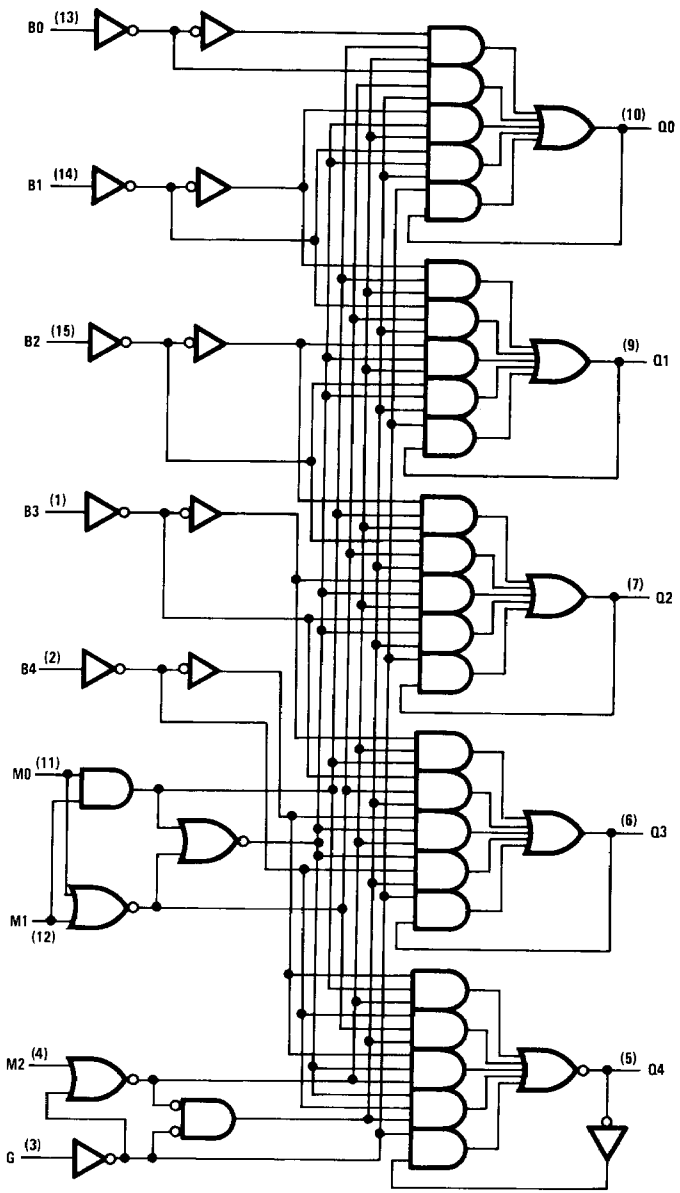
INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER			$\bar{Q}4$	Q3	Q2	Q1	Q0
	M2	M1	M0					
L	X	X	X	$Q4_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\bar{B}4$	B4	B3	B2	B1
H	L	H	L	$\bar{B}4$	B4	B3	B2	B1
H	L	H	H	$\bar{B}4$	B3	B2	B1	B0
H	H	L	L	B4	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$	$\bar{B}0$
H	H	L	H	B4	$\bar{B}4$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$
H	H	H	L	B4	$\bar{B}4$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant

$\bar{Q}4_0 \ldots Q0_0$ = The logic level of the same output before the high-to-low transition of G.

B4 . . . B0 = The logic level of the indicated multiplicand (B) input

LOGIC DIAGRAM



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_w		25			25			ns
Setup time, t_{setup}	Any M input	17↓			17↓			ns
	Any B input	15↓			15↓			
Hold time, t_{hold}	Any M input	0↓			0↓			ns
	Any B input	0↓			0↓			
Operating free-air temperature, T_A		-55		125	0		70	°C

↓The arrow indicates that the falling edge of the enable pulse is used for reference.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.2	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-1mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}	V_{CC}=MAX, All inputs at 0V, Outputs open			22	38		22	40	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	-55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Enable G	Any Q		25	39		22	35		25	39	ns
t_{PHL}				23	34		20	30		23	34	
t_{PLH}	Any M input	Any Q		28	44		25	40		28	44	ns
t_{PHL}				25	39		22	35		25	39	
t_{PLH}	Any B input	Any Q		30	46		27	42		30	46	ns
t_{PHL}				27	41		24	37		27	41	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Enable G	Any Q		30	44		26	40		30	44	ns
t_{PHL}				28	39		24	35		28	39	
t_{PLH}	Any M input	Any Q		33	49		29	45		33	49	ns
t_{PHL}				30	44		26	40		30	44	
t_{PLH}	Any B input	Any Q		35	51		31	47		35	51	ns
t_{PHL}				32	46		28	42		32	46	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.