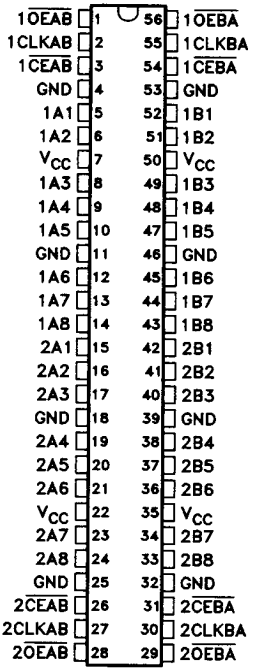
16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0238—D3560, JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16952, 54ACT16952 ... WD PACKAGE
74AC16952, 74ACT16952 ... DL PACKAGE
(TOP VIEW)



description

The 'AC16952 and 'ACT16952 are noninverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ and 2$\overline{OEAB}$), clock-enable (1$\overline{CEAB}$ and 2$\overline{CEAB}$), and clock (1CLKAB and 2CLKAB) inputs. When 1$\overline{CEAB}$ (or 2$\overline{CEAB}$) is high, data storage is inhibited and the registers retain their previous states. When 1$\overline{CEAB}$ (or 2$\overline{CEAB}$) is low, the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB). If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is also low, this stored data appears on the corresponding B outputs; if 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is high, the corresponding B outputs are in the high-impedance state. 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is controlled by 1$\overline{OEBA}$ and 2$\overline{OEBA}$, 1$\overline{CEBA}$ and 2$\overline{CEBA}$, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

PRODUCT PREVIEW

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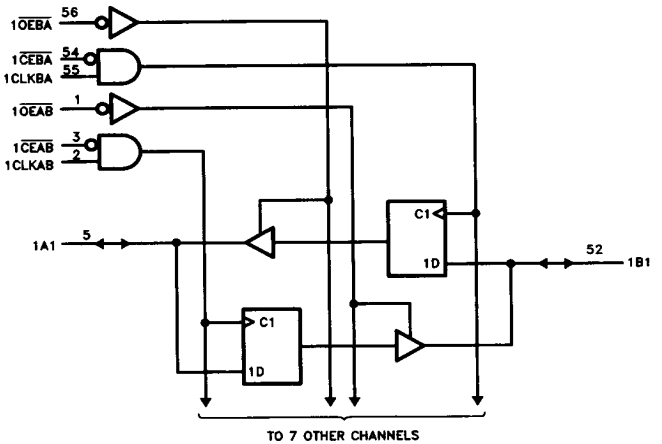
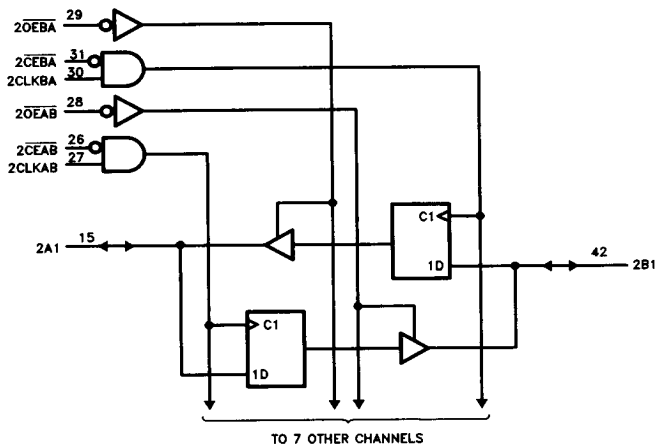
The 74AC16952 and 74ACT16952 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16952 has CMOS-compatible input thresholds. The 'ACT16952 has TTL-compatible input thresholds.

The 54AC16952 and 54ACT16952 are characterized over the full military temperature range of −55°C to 125°C. The 74AC16952 and 74ACT16952 are characterized for operation from −40°C to 85°C.

logic diagram (positive logic)





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