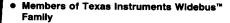
## 54AC16952, 54ACT16952 74AC16952, 74ACT16952 16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

238-D3560 JUNE 1990



- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

## description

The 'AC16952 and 'ACT16952 are noninverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1OEAB and 2OEAB), clockenable (1CEAB and 2CEAB), and clock (1CLKAB and 2CLKAB) inputs. When 1CEAB (or 2CEAB) is high, data storage is inhibited and the registers retain their previous states. When 1CEAB (or 2CEAB) is low, the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB). If 1OEAB (or 2OEAB) is also low, this stored data appears on the corresponding B outputs; if 1OEAB (or 2OEAB) is high, the corresponding B outputs are in the high-impedance state. 1OEAB (or 2OEAB) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is controlled by 1<del>OEBA</del> and 2<del>OEBA</del>, 1<del>CEBA</del> and 2<del>OEBA</del>, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

54AC16952, 54ACT16952 ... WD PACKAGE 74AC16952, 74ACT16952 ... DL PACKAGE (TOP VIEW)

10EAB	, U	56	10EBA
1CLKAB	2	55	1CLKBA
1 CEAB	3	54	1 CEBA
GND [	4	53	GND
1A1	5	52	1B1
1A2 [	6	51	1B2
V <sub>cc</sub> [	7	50	]V <sub>cc</sub>
1A3 [	8	49	1B3
1A4 [	9	48	1 <b>B4</b>
1A5 [	10	47	] 1B5
GND [	11	46	GND
1A6 🗀	12	45	1B6
1A7 🗌	13	44	1B7
1A8 🗌	14	43	1B8
2A1	15	42	281
2A2 🗌	16	41	2B2
2A3 🗌	17	40	2B3
GND [	18	39	GND
2A4 🗌	19	38	2B4
2A5 🗌	20	37	2B5
2A6 🗌	21	36	2B6
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A7 🗍	23	34	287
2A8 📗	24	33	288
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA

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3-163

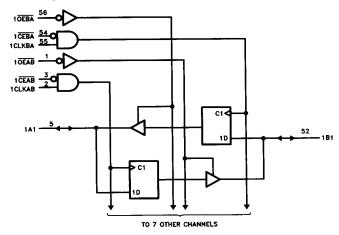
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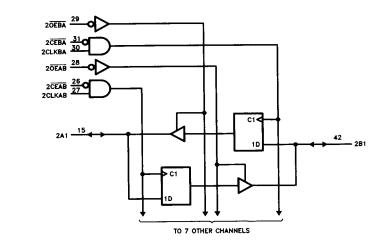
The 74AC16952 and 74ACT16952 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16952 has CMOS-compatible input thresholds. The 'ACT16952 has TTL-compatible input thresholds.

The 54AC16952 and 54ACT16952 are characterized over the full military temperature range of  $-55^{\circ}$ C to 125°C. The 74AC16952 and 74ACT16952 are characterized for operation from  $-40^{\circ}$ C to 85°C.

## logic diagram (positive logic)







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3-164

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