SMART®
Modular Technologies

SM5091610U4PUUU

November 21, 1996

16MByte (16M x 9) DRAM Module - 16Mx1 based
30-pin SIMM

Features

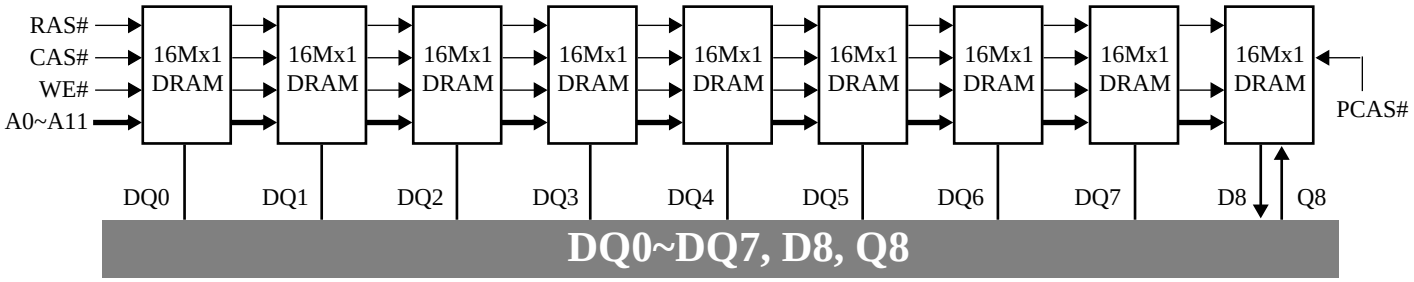
- Standard : JEDEC
- Configuration : Parity
- Access Time : 60/70/80ns
- Operation Mode : FPM
- Operating Voltage : 3.3/5.0V
- Refresh : 4K
- Device Physicals : 300mil SOJ/TSOP
- Lead Finish : Gold/Solder
- Length x Height : 3.500" x 0.830"
- No. of sides : Double-sided

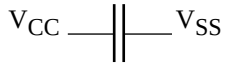
Part Numbers

SM509161004PUUU : FPM, 5.0V
SM509161014PUUU : FPM, 3.3V

Note: Refer last page for all "U" options.

Functional Diagram





Decoupling capacitors
to all devices.

(All specifications of this device are subject to change without notice.)

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Pin Name

A0~A11	Addresses
DQ0~DQ7	Data Inputs/Outputs
D8	Parity Data In
Q8	Parity Data Out
PCAS#	Parity CAS
CAS#	Column Address Strobe
RAS#	Row Address Strobe
WE#	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{CC}	16	DQ4
2	CAS#	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	WE#
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	A11
10	DQ2	25	DQ7
11	A4	26	Q8
12	A5	27	RAS#
13	DQ3	28	PCAS#
14	A6	29	D8
15	A7	30	V_{CC}

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Vcc=3.3V	Vcc=5.0V	
Voltage on any pin relative to V_{SS}	V_T	- 0.5 to +4.6	- 1.0 to +7.0	V
Power Dissipation	P_T	9	9	W
Operating Temperature	T_{opr}	0 to +70	0 to +70	°C
Storage Temperature	T_{stg}	- 55 to +150	- 55 to +150	°C
Short Circuit Output Current	I_{OS}	50	50	mA

Recommended DC Operating Conditions
(T_A = 0 to +70°C)

Parameter	Symbol	Vcc=3.3V			Vcc=5.0V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} +0.3	2.4	-	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	-1.0	-	0.8	V

Capacitance
(V_{CC} = 3.3V±10%/5.0V±10%, T_A = +25°C)

Parameter	Symbol	Max	Unit
Input Capacitance (Address)	C_{I1}	55	pF
Input Capacitance (RAS#, WE#)	C_{I2}	73	pF
Input Capacitance (CAS#)	C_{I3}	66	pF
Input Capacitance (PCAS#)	C_{I4}	17	pF
Input Capacitance (D8)	C_{I5}	17	pF
Output Capacitance (Q8)	C_{O1}	17	pF
Input/Output Capacitance (DQ0~DQ7)	$C_{I/O}$	17	pF

Notes : Capacitance is sampled per Mil-Std-883.

DC Characteristics (cont'd)

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	60ns		70ns		80ns		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{CC}+0.3V$	-90	90	-90	90	-90	90	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le V_{CC}$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	Low I_{out} = 2mA	-	0.4	-	0.4	-	0.4	V

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	60ns		70ns		80ns		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{CC}+0.5V$	-90	90	-90	90	-90	90	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le V_{CC}$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	High I_{out} = -5mA	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	Low I_{out} = 4.2mA	-	0.4	-	0.4	-	0.4	V

DC Characteristics (cont'd)

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Max. 60ns	Max. 70ns	Max. 80ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling; t_{RC} = min.	720	630	540	mA	1, 2
Standby Current	I_{CC2}	LVTTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z	18	18	18	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z	9	9	9	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=VIH; RAS#, Address cycling @ t_{RC}=min.	720	630	540	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	720	630	540	mA	
Fast Page Mode Current	I_{CC5}	RAS#=VIL, CAS#, Address cycling @ t_{PC}=min.	630	540	450	mA	1, 3

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Max. 60ns	Max. 70ns	Max. 80ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling; t_{RC} = min.	720	630	540	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z	18	18	18	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z	9	9	9	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address cycling @ t_{RC}=min.	720	630	540	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	720	630	540	mA	
Fast Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address cycling @ t_{PC}=min.	630	540	450	mA	1, 3

Notes: 1. Values depend on output load condition when the device is selected. Maximum values are specified at the output open condition.
2. Address can be changed once or less while RAS# = V_{IL} .
3. Address can be changed once or less while CAS# = V_{IH} .

AC Characteristics

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	60ns		70ns		80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Common to Read and Write Cycles									
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	10	-	15	-	15	-	ns	
CAS# pulse width	t_{CAS}	15	10000	18	10000	20	10000	ns	
CAS# to output in Low-Z	t_{CLZ}	0	-	0	-	0	-	ns	3
CAS# to RAS# precharge time	t_{CRP}	5	-	5	-	5	-	ns	
CAS# hold time	t_{CSH}	60	-	70	-	80	-	ns	
RAS# to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	10
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
RAS# pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
Random read/write cycle time	t_{RC}	110	-	130	-	150	-	ns	
RAS# to CAS# delay time	t_{RCD}	20	40	20	50	20	60	ns	4
RAS# precharge time	t_{RP}	40	-	50	-	60	-	ns	
RAS# hold time	t_{RSH}	15	-	18	-	20	-	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
Read Cycle									
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Access time from CAS#	t_{CAC}	-	15	-	18	-	20	ns	3, 4, 5
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	6
Access time from RAS#	t_{RAC}	-	60	-	70	-	80	ns	3, 4
Column address to RAS# lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command hold time referenced to CAS#	t_{RCH}	0	-	0	-	0	-	ns	8
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time referenced to RAS#	t_{RRH}	0	-	0	-	0	-	ns	8
Write Cycle									
Write command to CAS# lead time	t_{CWL}	15	-	15	-	20	-	ns	
Data-in hold time	t_{DH}	10	-	15	-	15	-	ns	9
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	9
Write command to RAS# lead time	t_{RWL}	20	-	20	-	25	-	ns	
Write command hold time	t_{WCH}	10	-	10	-	15	-	ns	
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
Write command pulse width	t_{WP}	10	-	10	-	15	-	ns	

AC Characteristics (cont'd)

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

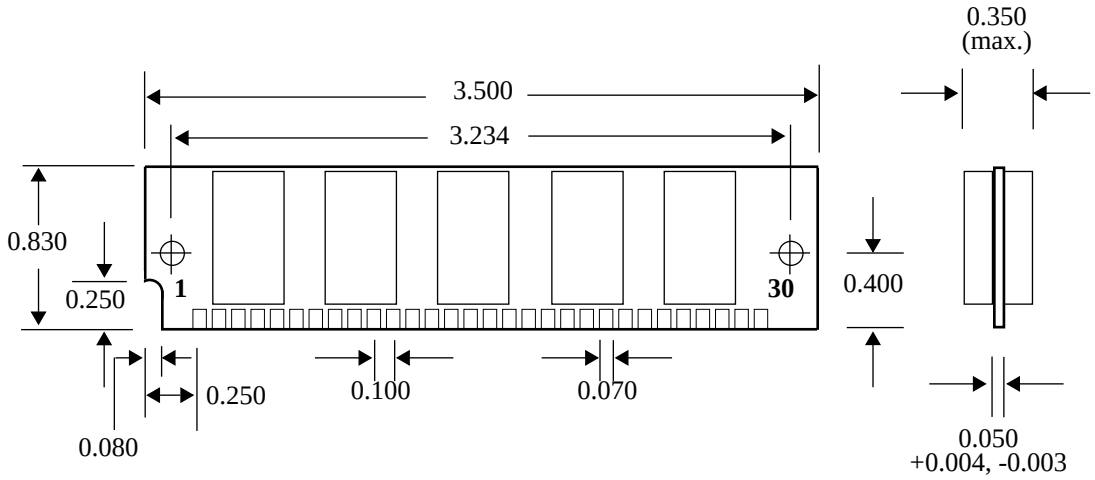
Parameter	Symbol	60ns		70ns		80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page Mode Cycle									
Access time from CAS# precharge	t_{ACP}	-	35	-	40	-	45	ns	3, 11
CAS# precharge time	t_{CP}	10	-	10	-	10	-	ns	
Fast page mode cycle time	t_{PC}	40	-	45	-	50	-	ns	
RAS# pulse width	t_{RASP}	60	200000	70	200000	80	200000	ns	12
RAS# hold time from CAS# precharge	t_{RHCP}	35	-	40	-	45	-	ns	
Refresh Cycle									
CAS# hold time (CBR refresh)	t_{CHR}	10	-	15	-	15	-	ns	1
CAS# set-up time (CBR refresh)	t_{CSR}	5	-	5	-	5	-	ns	1
Refresh period	t_{REF}								
4K refresh		-	64	-	64	-	64	ms	
RAS# precharge to CAS# hold time	t_{RPC}	5	-	5	-	5	-	ns	

Notes:
1. An initial pause of atleast 200µs is required after power-up followed by any eight RAS# cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) limit can be met; t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS# leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA} , t_{CAC} or $t_{ACP.}$
12. t_{RASP} defines RAS# pulse width in fast page mode cycles.
13. $t_{AR,}$ $t_{WC,}$ t_{DHR} are referenced to t_{RAD}(max).

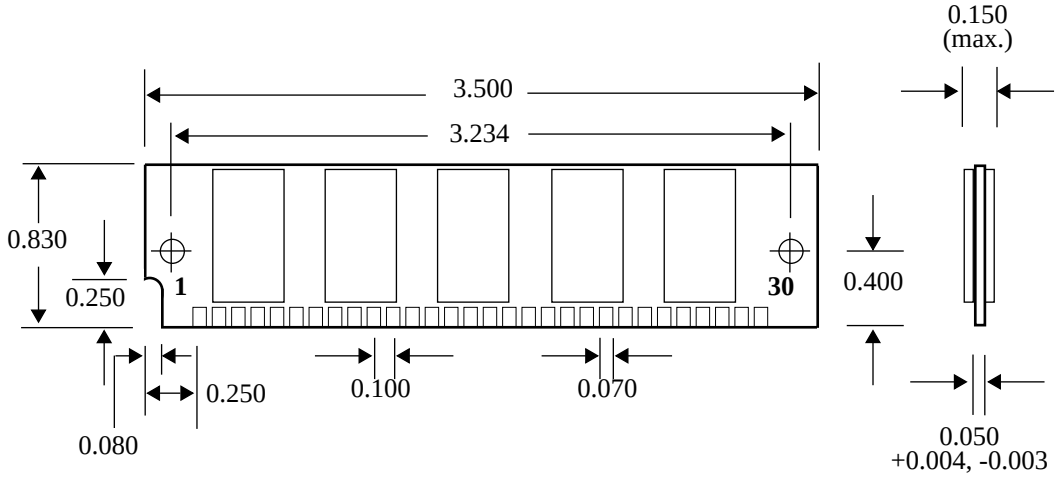
Physical Dimensions

30-pin SIMM Module

SOJ Based



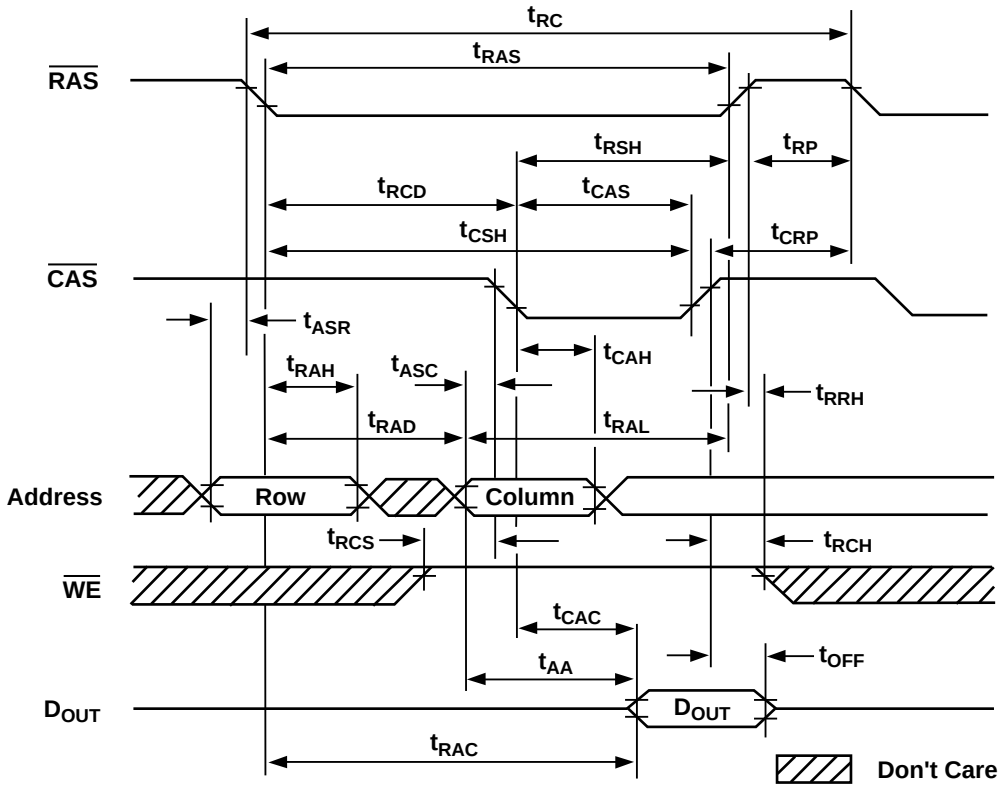
TSOP Based



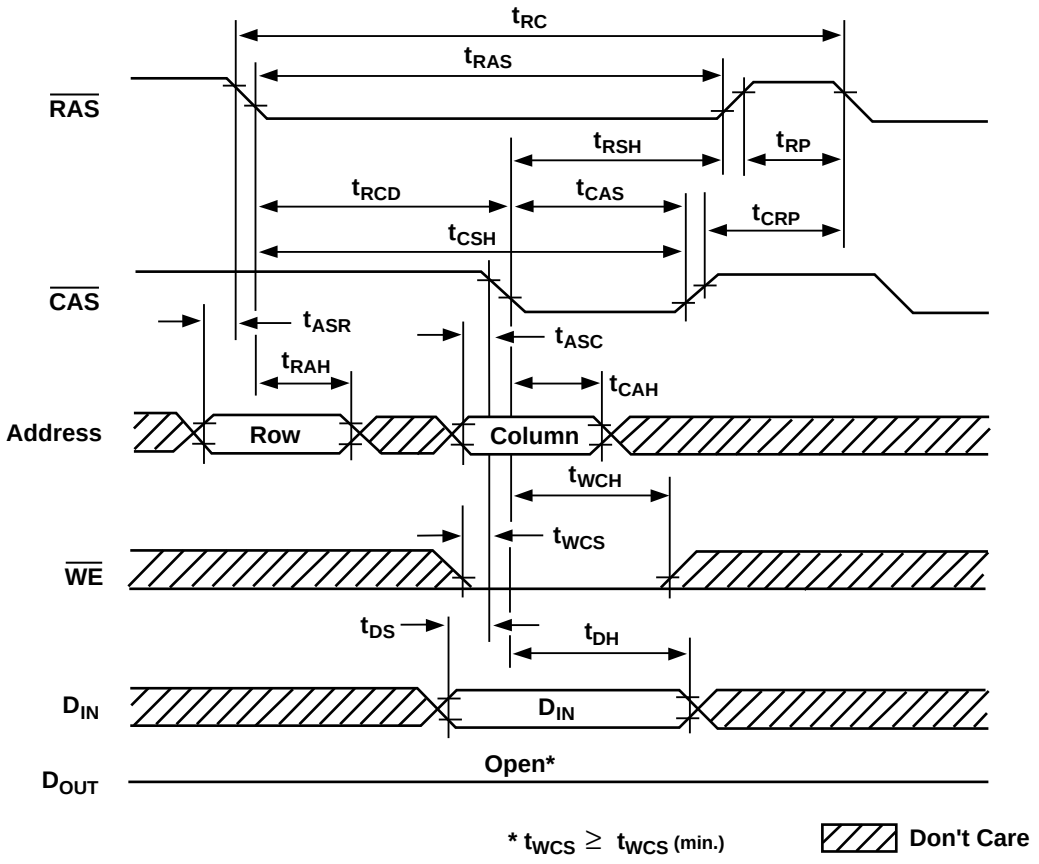
(All dimensions are in inches with ±0.005” tolerance unless specified otherwise.)

Timing Waveforms

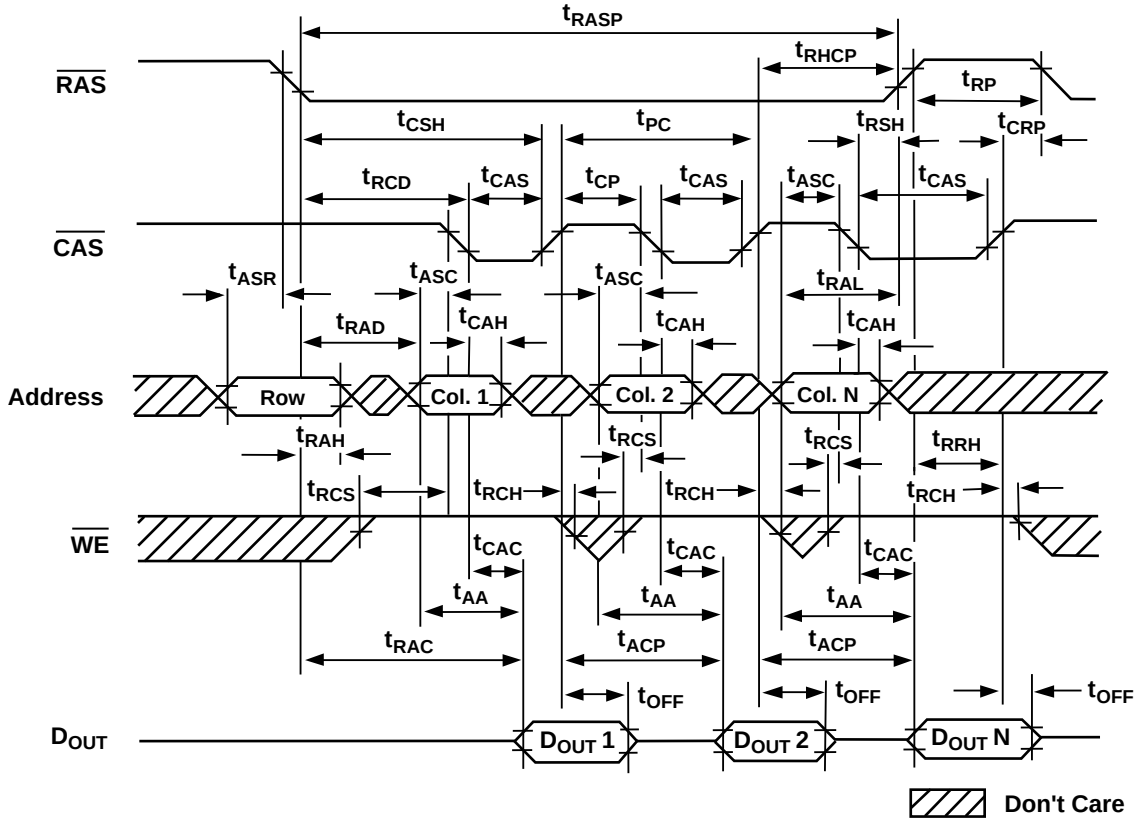
Read Cycle



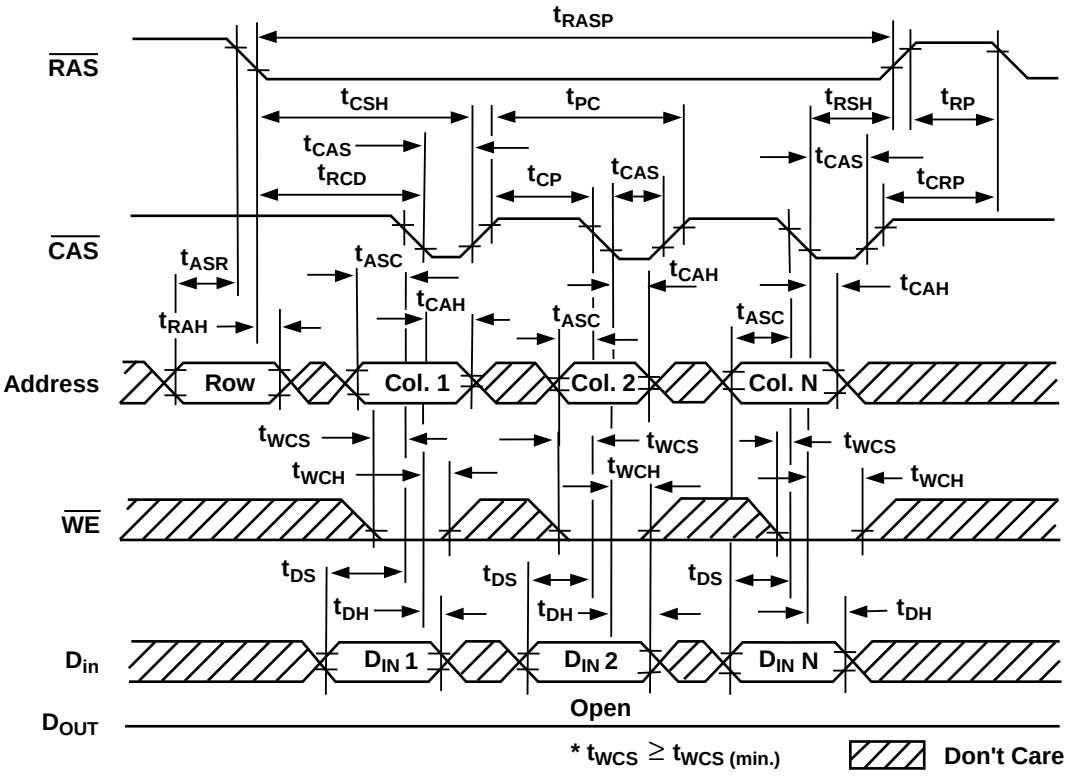
Write Cycle (Early Write)



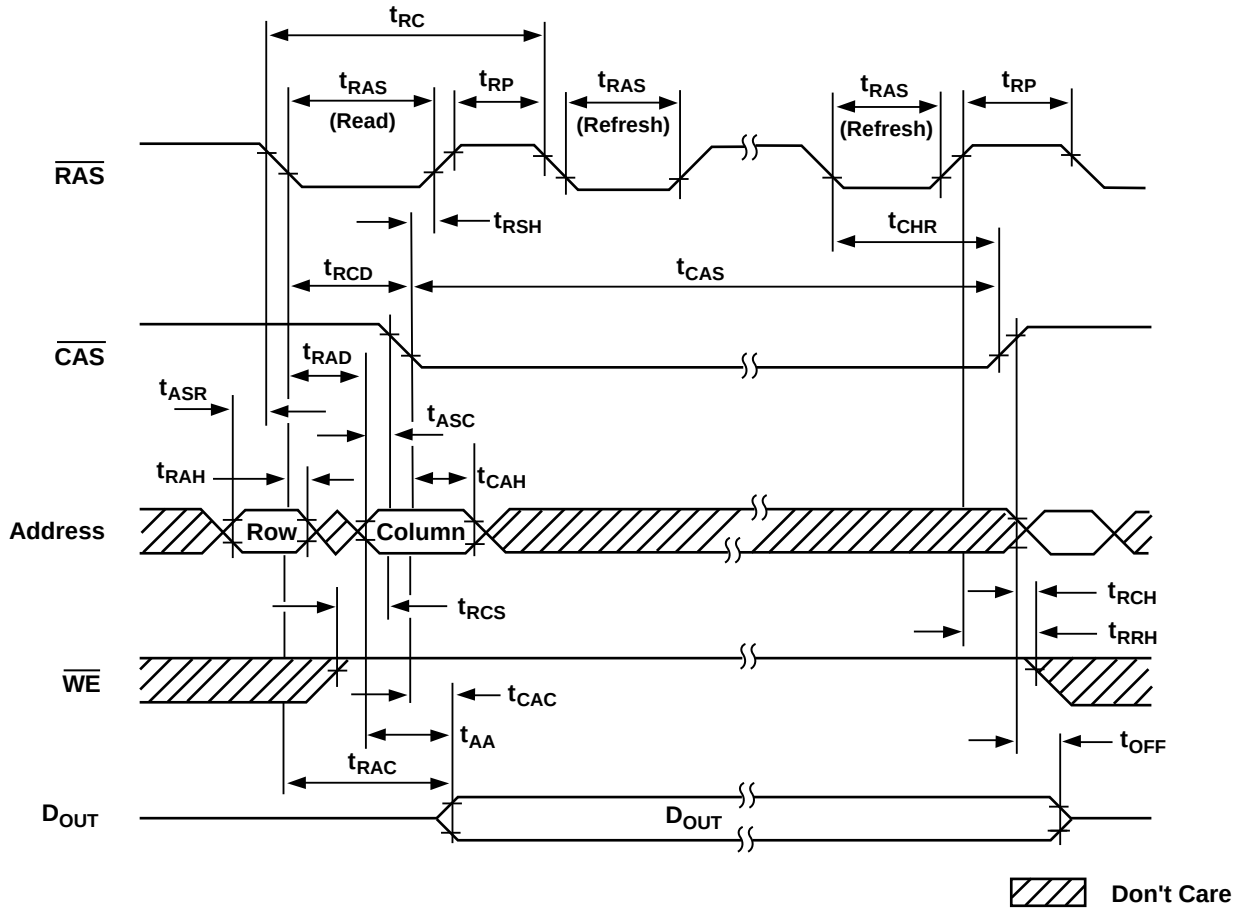
Fast Page Mode Read Cycle



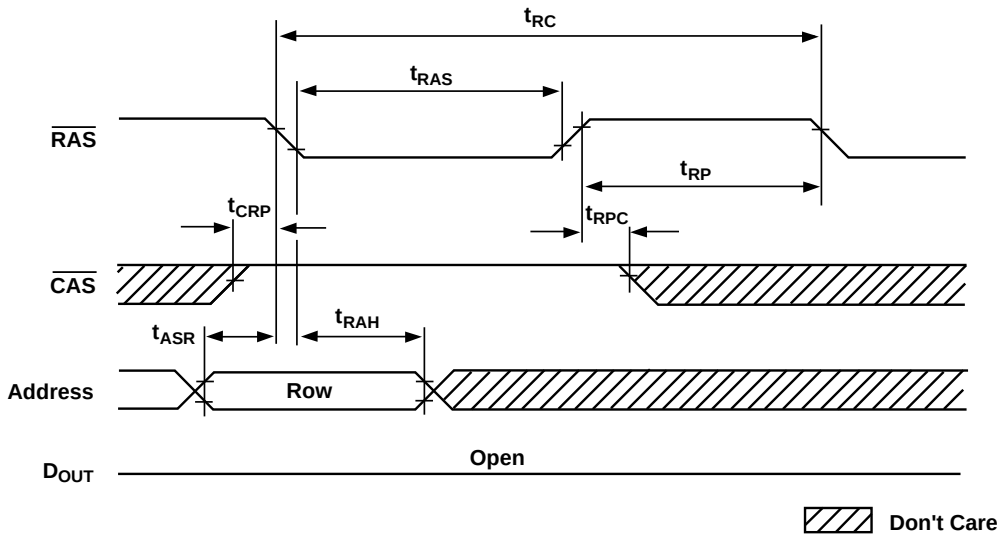
Fast Page Mode Write Cycle (Early Write)



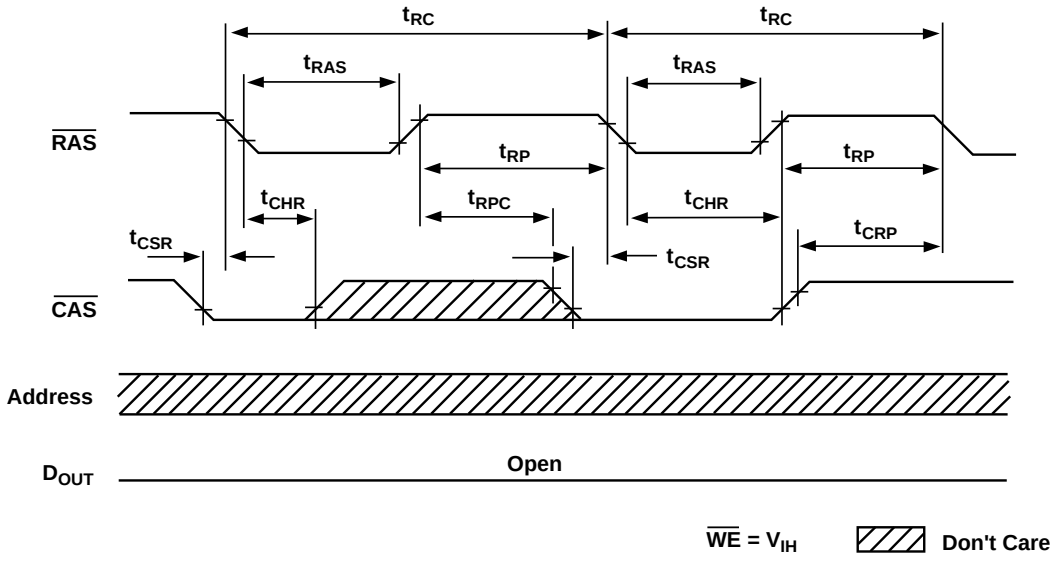
Hidden Refresh Cycle



RAS# Only Refresh Cycle



CAS#-Before-RAS# Refresh Cycle



Ordering Information

SM	5	09	16	1	0	U	4	P	U	U	U
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)

(1) **SMART**
Modular Technologies

(2) **Product Category**
5 : DRAM SIMM / DIMM

(3) **Module Data Bus Width**
09 : x9

(4) **Module Address Depth**
16 : 16M

(5) **Device Data Width**
1 : x1

(6) **Special Device Feature**
0 : Standard

(7) **Voltage / Mode**
0 : 5.0V / Fast Page Mode
1 : 3.3V / Fast Page Mode

(8) **Refresh / Power**
4 : 4K Ref. / Standard Power

(9) **Module Configuration**
P : Parity

(10) **Device Physicals**
3 : SOJ DRAMs (300mil)
5 : TSOP DRAMs (300mil)

(11) **Module Lead Finish**
S : Solder
G : Gold

(12) **Module Access Speed**
6 : 60ns
7 : 70ns
8 : 80ns

Note : “U” in the part number should be replaced by user specified option.

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