1 M × 1-Bit Dynamic RAM — HYB 511000BJ-50/-60/-70
Low Power 1 M × 1-Bit Dynamic RAM — HYB 511000BJL-50/-60/-70

Advanced Information

- 1 048 576 words by 1-bit organization
- Fast access and cycle time
  50 ns access time
  95 ns cycle time (-50 version)
  60 ns access time
  130 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
  45 ns (-70 version)
- Low power dissipation
  max. 495 mW active (-50 version)
  max. 440 mW active (-60 version)
  max. 385 mW active (-70 version)
  max. 5.5 mW standby
  max. 1.1 mW standby for L-version
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using “early write” operation
- Read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden-refresh, fast page mode capability and test mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms
  512 refresh cycles/64 ms
  for L-version only
- Plastic Packages: P-SOJ-26/20-1

Ordering Information

Type	Ordering Code	Package	Description
HYB 511000BJ-50	Q67100-Q1056	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 511000BJ-60	Q67100-Q518	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 511000BJ-70	Q67100-Q519	P-SOJ-26/20-1	DRAM (access time 70 ns)
HYB 511000BJL-50	on request	P-SOJ-26/20-1	DRAM (access time 50 ns)
HYB 511000BJL-60	Q67100-Q526	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 511000BJL-70	Q67100-Q527	P-SOJ-26/20-1	DRAM (access time 70 ns)

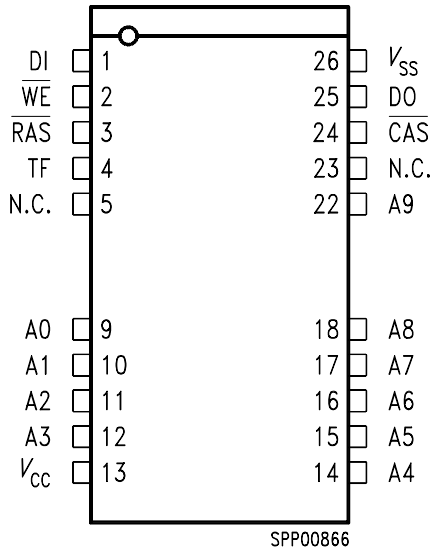
The HYB 511000BJ/BJL is the new generation dynamic RAM organized as 1 048 576 words by 1-bit. The HYB 511000BJ/BJL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 511000BJ/BJL to be packaged in a standard plastic P-SOJ-26/20. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. “Test Mode” function is implemented. The HYB 511000BJL are specially selected for low power battery backup applications.

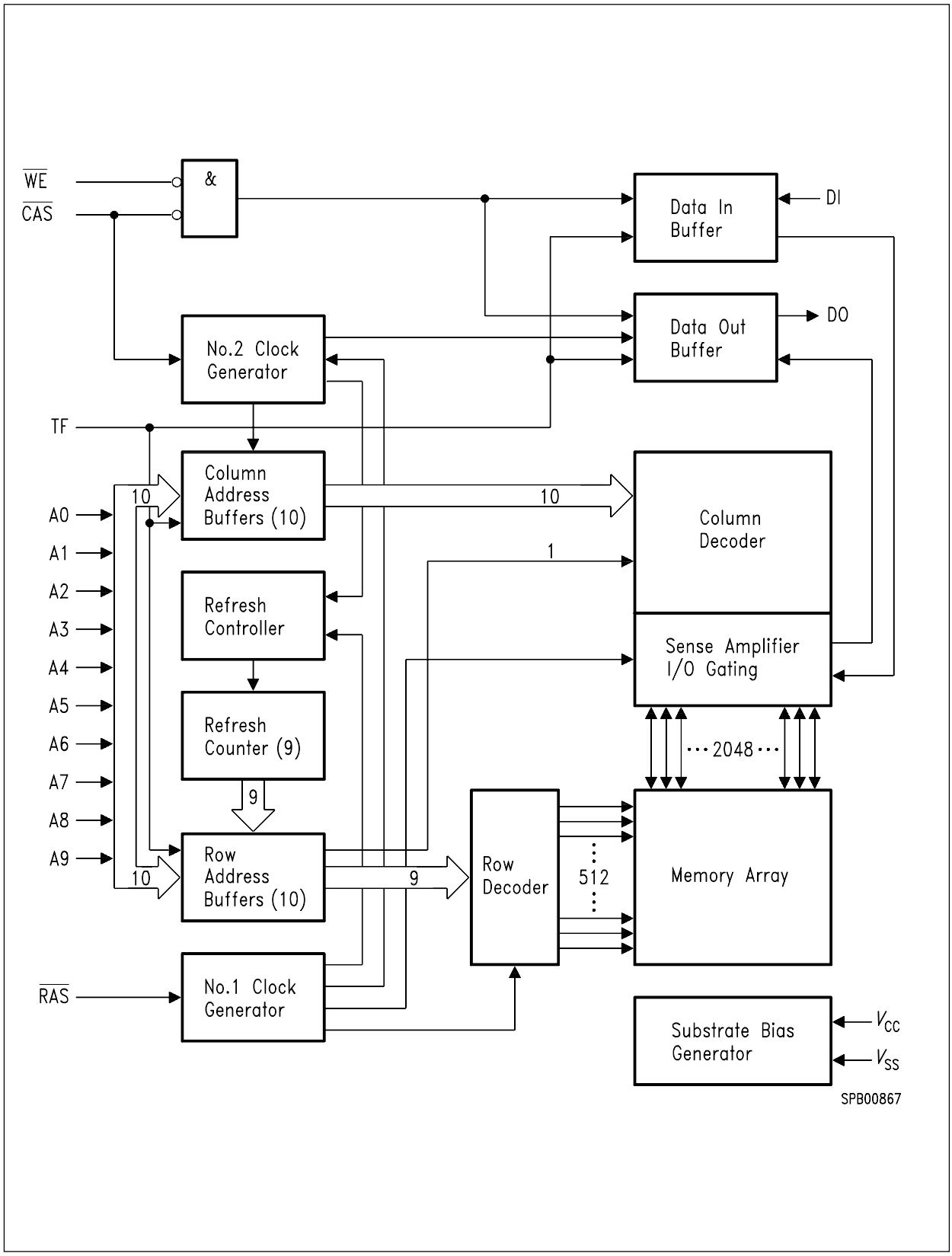
Pin Definitions and Functions

Pin No.	Function
A0-A9	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
TF	Test Function
N.C.	No Connection

Pin Configuration
(top view)

SOJ-26/20-1





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C

Storage temperature range ..... – 55 to + 150 °C

Soldering temperature ..... 260 °C

Soldering time ..... 10 s

Input/output voltage ..... – 1 to + 7 V

Test Function Input voltage ..... – 1 to + 10.5 V

Power supply voltage ..... – 1 to + 7 V

Power dissipation ..... 0.6 W

Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
Test enable input high voltage	$V_{IH(TF)}$	V_{CC} + 4.5	10.5	V	1)
Test disable input low voltage	$V_{IL(TF)}$	– 1.0	V_{CC} + 1.0	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input except TF (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -50 version -60 version -70 version ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – – –	 90 80 70	 mA mA mA	 2) 3) 2) 3) 2) 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (cont'd)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles: -50 version	I_{CC3}	–	90	mA	2)
-60 version		–	80	mA	2)
-70 version		–	70	mA	2)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)					
Average V_{CC} supply current during fast page modes: -50 version	I_{CC4}	–	70	mA	2) 3)
-60 version		–	60	mA	2) 3)
-70 version		–	50	mA	2) 3)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current	I_{CC5}	–	1	mA	1)
L-Version		–	200	µA	1)
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)					
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				
-50 version		–	90	mA	2)
-60 version		–	80	mA	2)
-70 version		–	70	mA	2)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
For L-version only: Battery backup current: average power supply current, battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A9 = V_{CC} – 0.2 V or 0.2 V, DI = V_{CC} – 0.2 V or 0.2 V open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min. ~ 1 µs)	I_{CC7}	–	300	µA	2)
Input leakage current (only TF) (0 V ≤ V_{IN} (TF) ≤ V_{CC} + 0.5 V) All other pins not under test = 0 V	$I_{ITF(L)}$	– 10	+ 10	µA	1)
Test function input current (V_{CC} + 4.5 ≤ V_{IN} (TF) ≤ 10.5 V)	I_{TF}	–	1	mA	1)

AC Characteristics [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	ns
Read-write cycle time	t_{RWC}	115	–	130	–	155	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns
Fast page mode read-write cycle time	t_{PRWC}	55	–	60	–	70	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	50	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	25	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	15	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10.000	60	10.000	70	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	100.000	60	100.000	70	100.000	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (FPM)	t_{RHCP}	30	–	35	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ delay time (FPM RMW)	t_{CPWD}	30	–	35	–	45	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10.000	15	10.000	20	10.000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	35	20	45	20	50	ns

AC Characteristics (cont'd) [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	25	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9)]	t_{DH}	10	–	15	–	15	–	ns
Refresh period	t_{REF}	–	8	–	8	–	8	ms
Refresh period for L-version only	t_{REF}	–	64	–	64	–	64	ms

AC Characteristics (cont'd) [4) 13)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-50		-60		-70		
		min.	max.	min.	max.	min.	max.	
Write command setup time [10)]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WE}$ delay time [10)]	t_{CWD}	15	–	15	–	20	–	ns
$\overline{RAS}$ to $\overline{WE}$ delay time [10)]	t_{RWD}	50	–	60	–	70	–	ns
Column address to $\overline{WE}$ delay time [10)]	t_{AWD}	25	–	30	–	35	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	5	–	5	–	5	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	10	–	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	25	–	30	–	40	–	ns
Test mode enable setup time referenced to $\overline{RAS}$	t_{TES}	0	–	0	–	0	–	ns
Test mode enable hold time referenced to $\overline{RAS}$	t_{TEHR}	0	–	0	–	0	–	ns
Test mode enable hold time referenced to $\overline{CAS}$	t_{TEHC}	0	–	0	–	0	–	ns

Capacitance

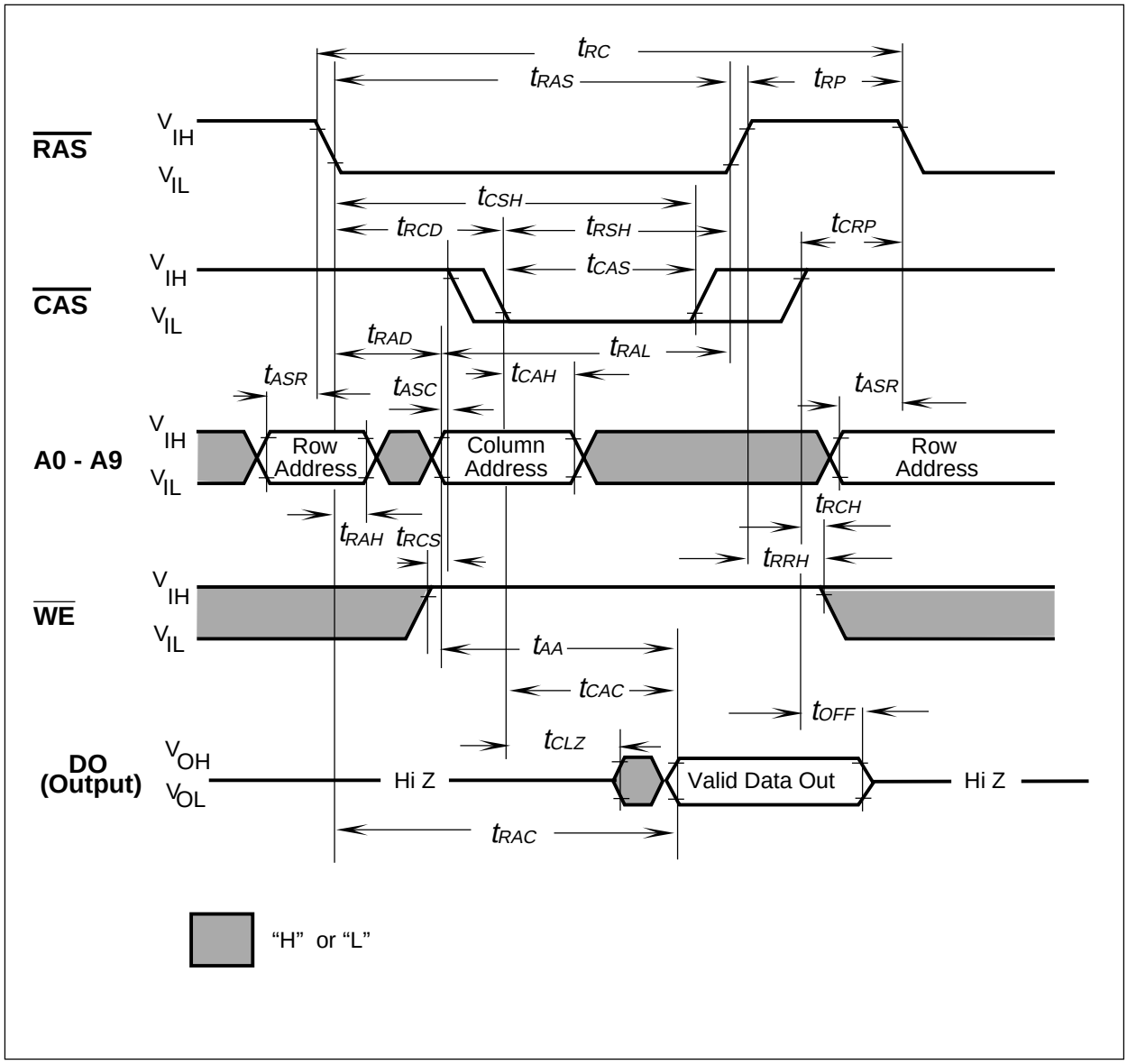
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, DI)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, TF)	C_{I2}	–	7	pF
Output capacitance (DO)	C_O	–	7	pF

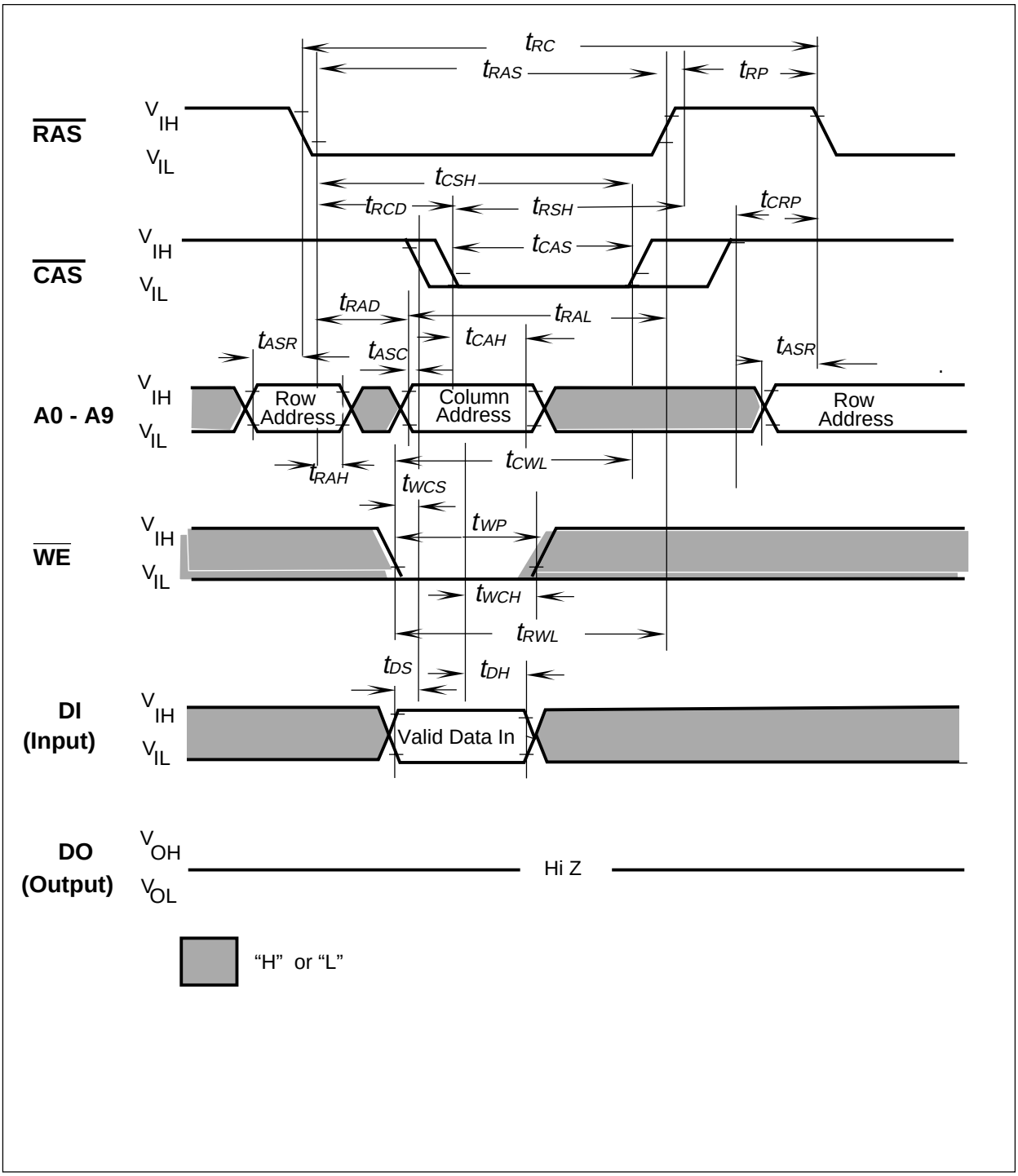
Notes :

1) All voltages are referenced to V_{SS} .
2) I_{CC1} , I_{CC3} , I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{WE}}$ leading edge in read-write cycles.
10) t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.
11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC} .
12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .
13) AC measurements assume t_T = 5ns.

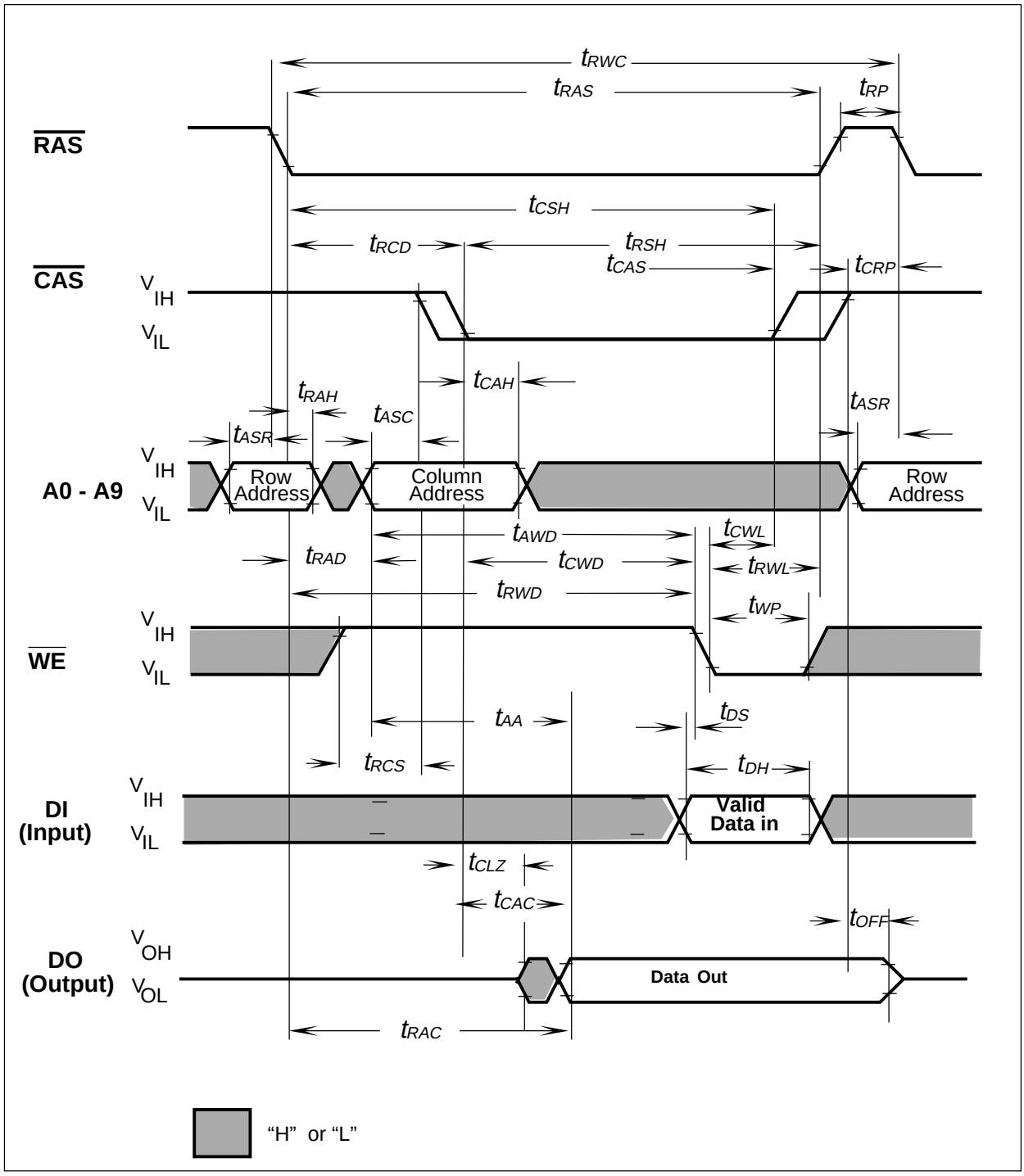
Waveforms



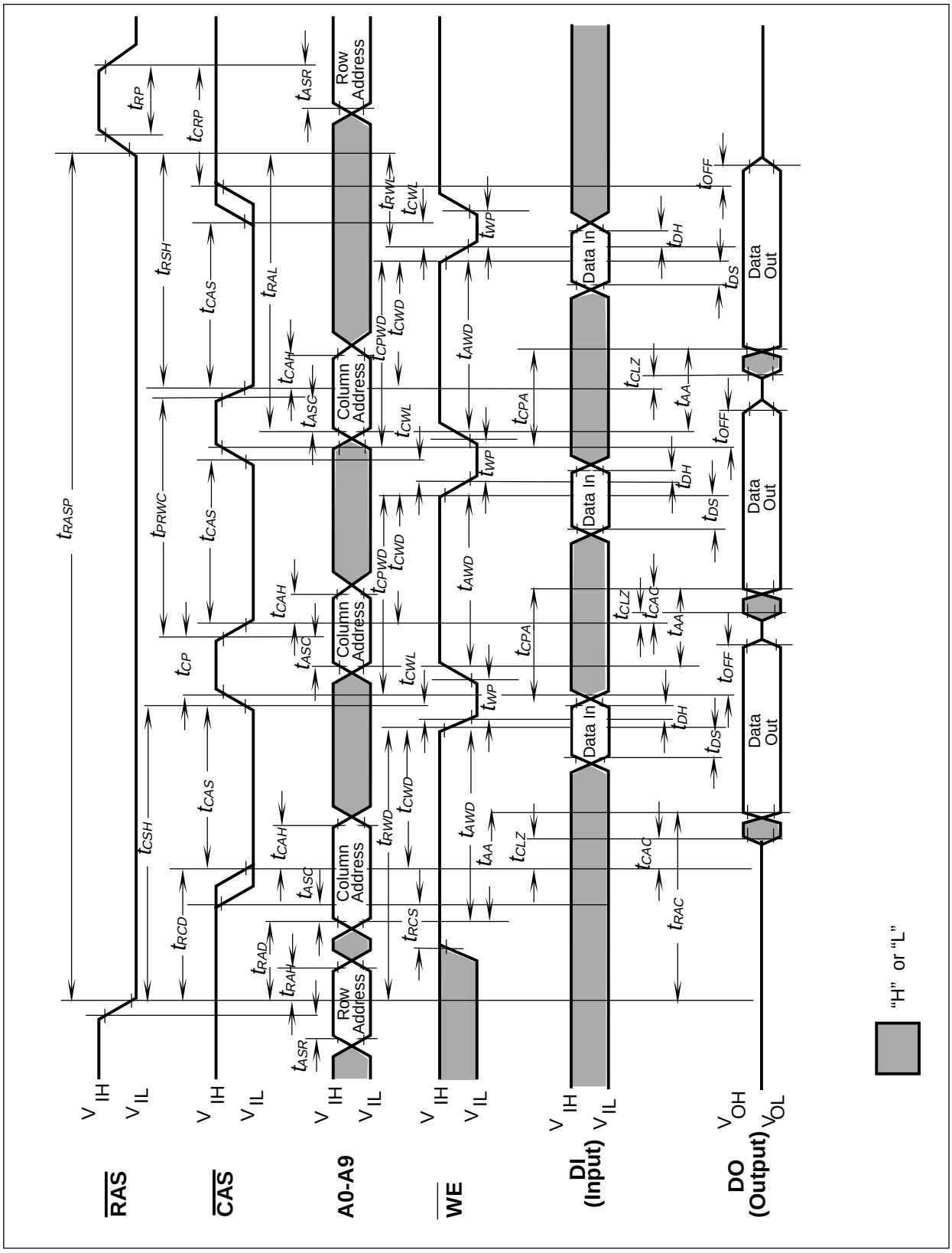
Read Cycle



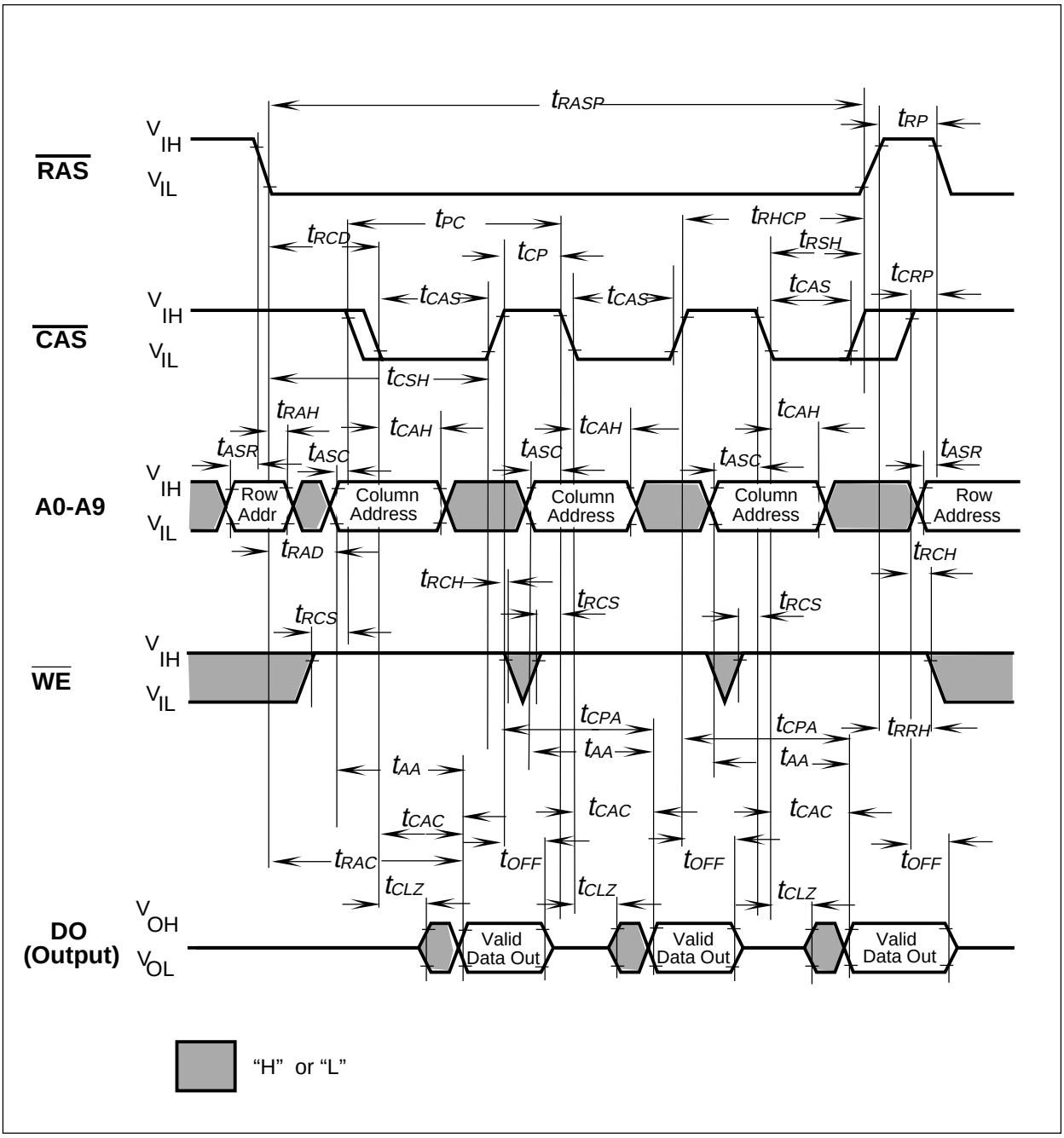
Write Cycle (Early Write)



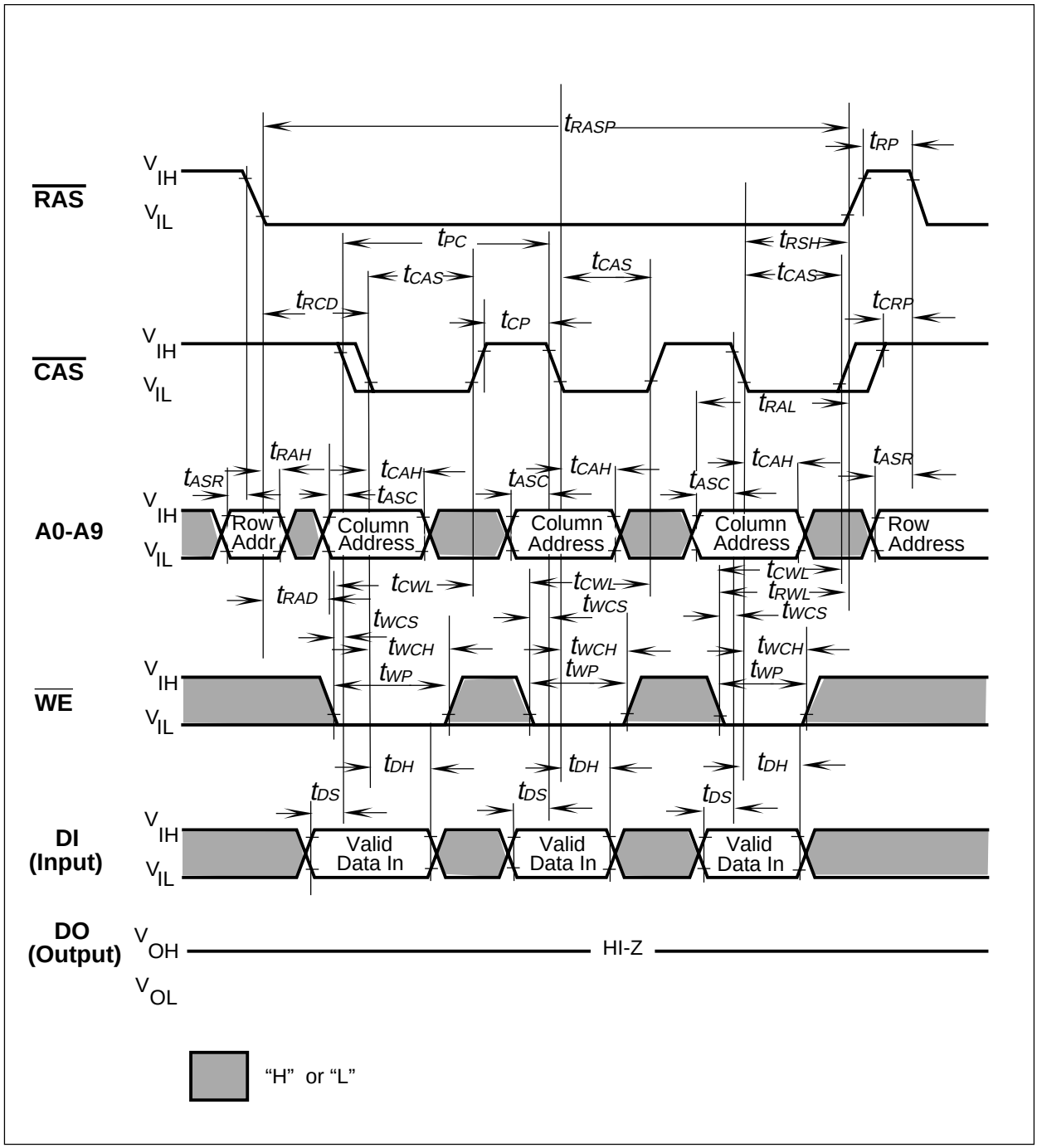
Read-Write (Read-Modify-Write) Cycle



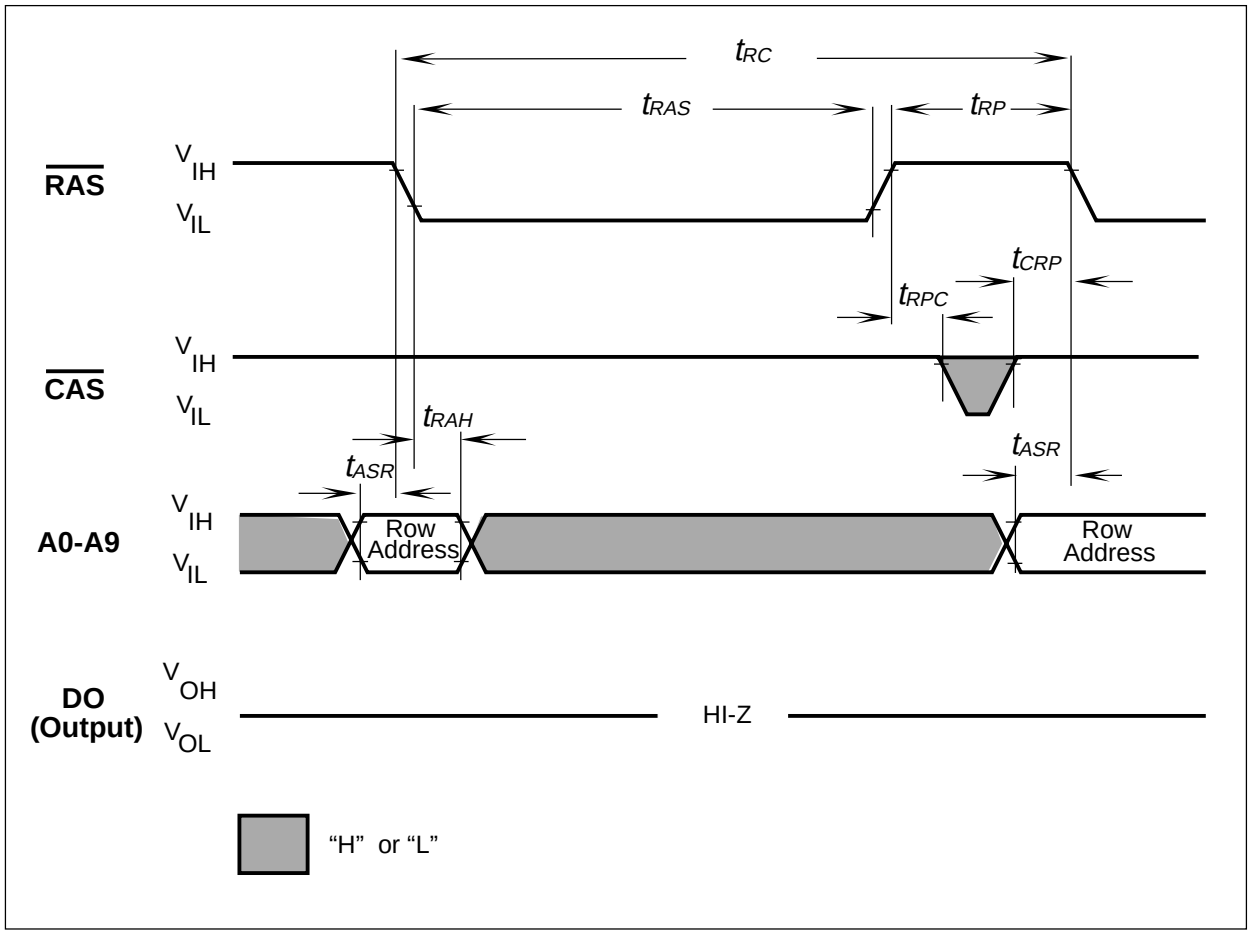
Fast Page Mode Read-Modify-Write Cycle



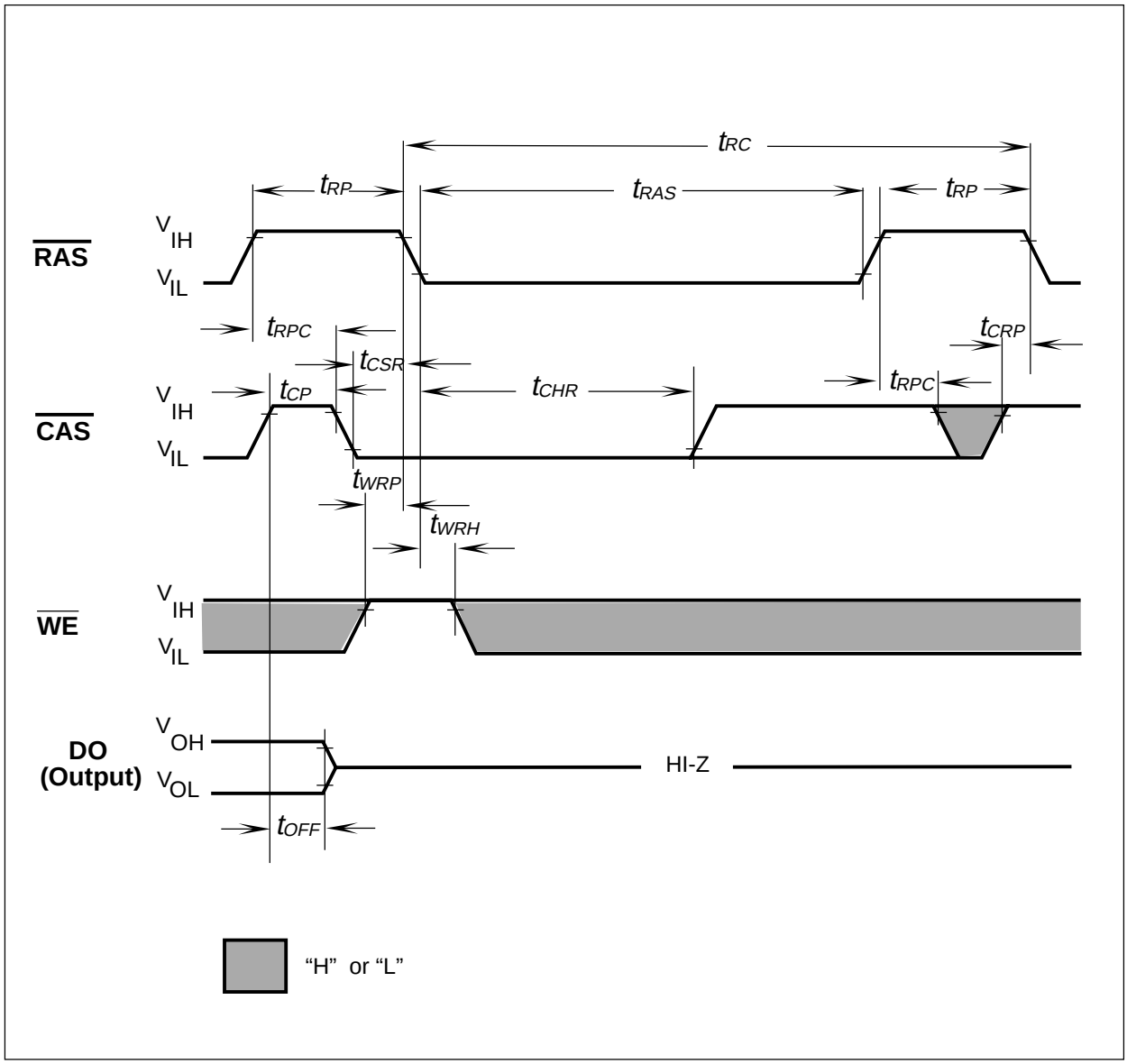
Fast Page Mode Read Cycle



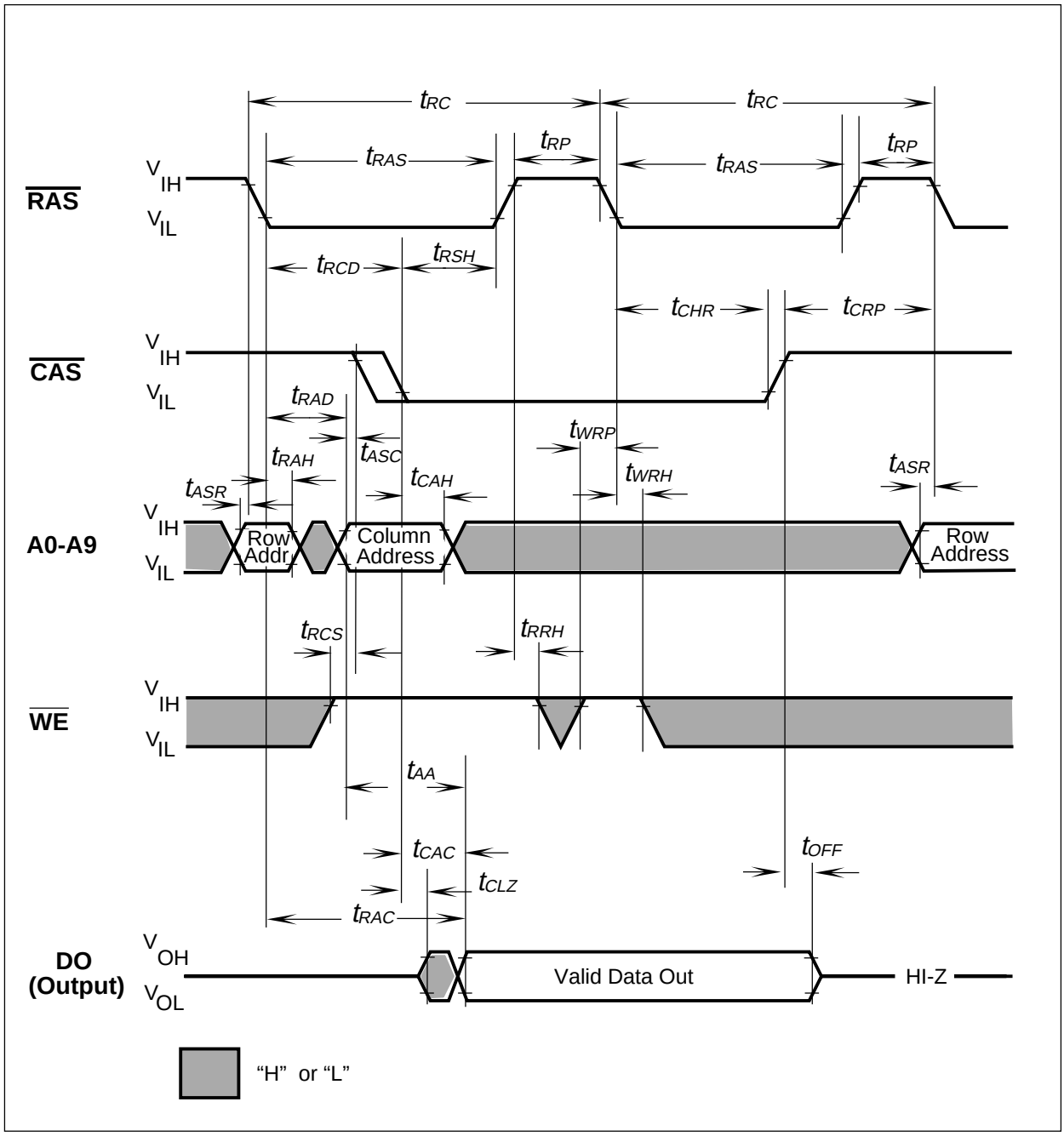
Fast Page Mode Early Write Cycle



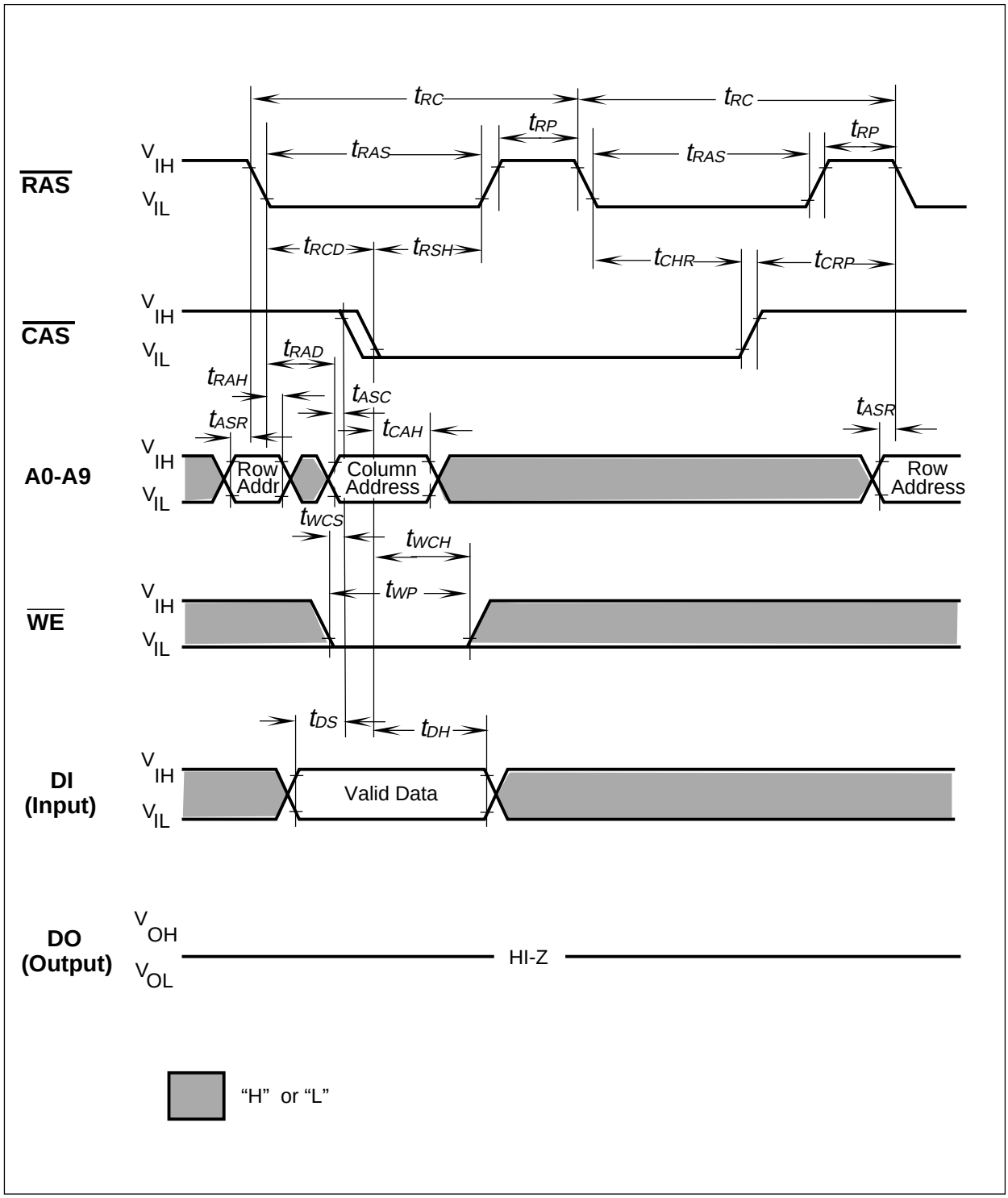
$\overline{\text{RAS}}$-Only Refresh Cycle



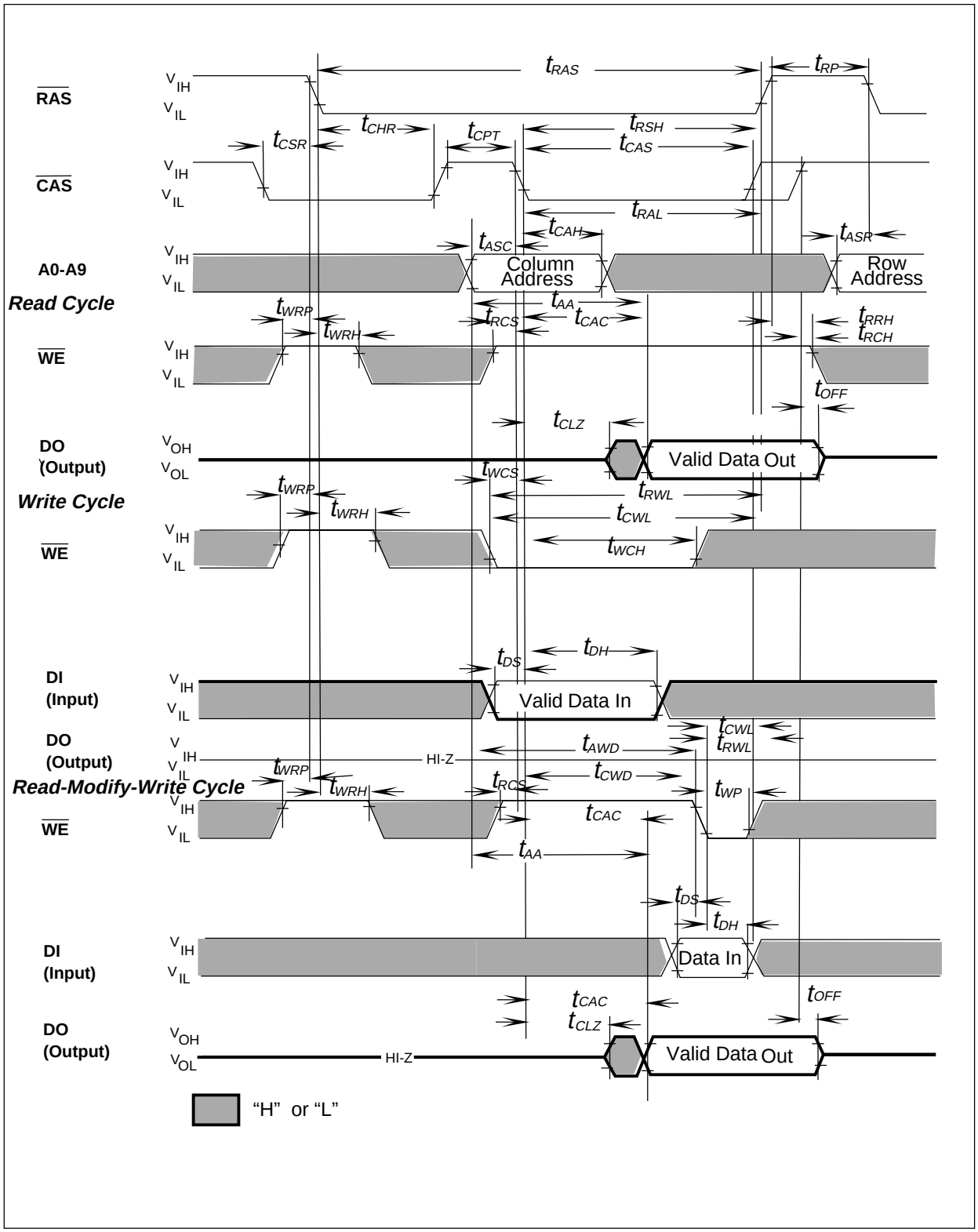
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



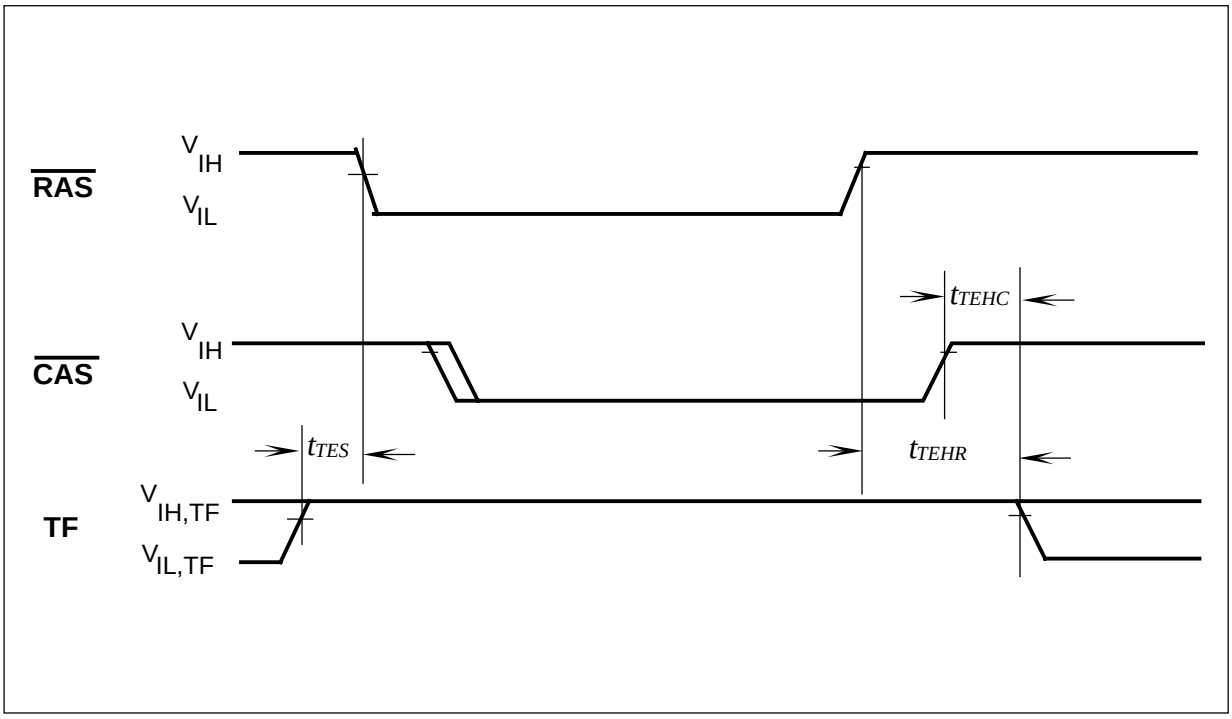
CAS-Before-RAS Refresh Counter Test Cycle

Test Mode

The HYB 511000B/BL is the RAM organized 1 048 576 words by 1-bit, it is internally organized 262 144 words by 4-bit. In “Test Mode”, data would be written into a number of sectors (4 sectors) in parallel and retrieved the same way. If upon reading, all bits are equal (all “H” or “L”), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. The next figure shows the block diagram including its truth table when “Test Mode” is used.

In test mode, 1M DRAM can be tested as if it were 256K DRAM by the following method.

“Test Mode” function is performed on any of the timing cycles including fast page mode when “TF” pin is held on “super voltage (V_{CC} + 4.5 V (V_{CC} = 5 V ± 10 %), max. voltage = 10.5 V)” for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see next figure). The address input of A9 is ignored in the “Test Mode”. On the other hand, normal operation requires the “TF” pin be connected to V_{IL}(TF) level, or left unconnected on the printed wiring board. The “Test Mode” function reduces test times (1/4; in case of using N test pattern).



Test Mode Cycle