

HM53462 Series

65,536-Word x 4-Bit Multiport CMOS Video RAM (with Logic Operation Mode)

DESCRIPTION

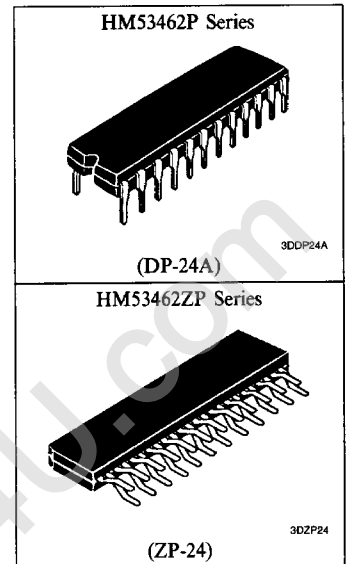
The HM53462 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2 μ m CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

FEATURES

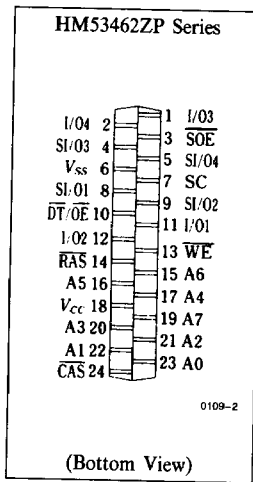
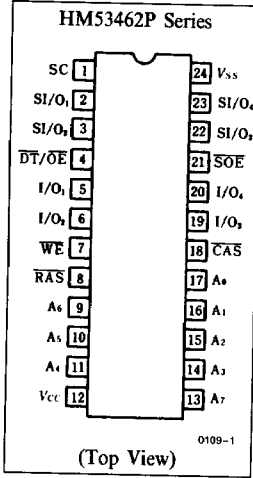
- Multiport Organization
(RAM; 64k-word x 4-bit and SAM; 256-word x 4-bit)
- Double Layer Polysilicon/Polycide N-Well CMOS Process
- Single 5V ($\pm 10\%$)
- Low Power
 - Active RAM 380 mW (max)
 - SAM 220 mW (max)
 - Standby 40 mW (max)
- Access Time
 - RAM 100 ns/120 ns/150 ns
 - SAM 40 ns/40 ns/60 ns
- Cycle Time
 - Random Read or Write Cycle Time (RAM) 190 ns/220 ns/260 ns
 - Serial Read or Write Cycle Time (SAM) 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles 4 ms
- Refresh Function
 - RAS Only Refresh
 - CAS Before RAS Refresh
 - Hidden Refresh
- Bidirectional Data Transfer Operation (RAM \leftrightarrow SAM)
- Fast Serial Access Operation Asynchronized with RAM Port except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability
- Logic Operation Capability between D_{in} and D_{out}
- SAM Organization Can Be Changed to 1024 x 1

ORDERING INFORMATION

| Part No. | Access Time | Package |
|--------------|-------------|----------------|
| HM53462P-10 | 100 ns | 400 mil 24-pin |
| HM53462P-12 | 120 ns | Plastic DIP |
| HM53462P-15 | 150 ns | (DP-24A) |
| HM53462ZP-10 | 100 ns | 24-pin |
| HM53462ZP-12 | 120 ns | Plastic DIP |
| HM53462ZP-15 | 150 ns | (ZP-24) |



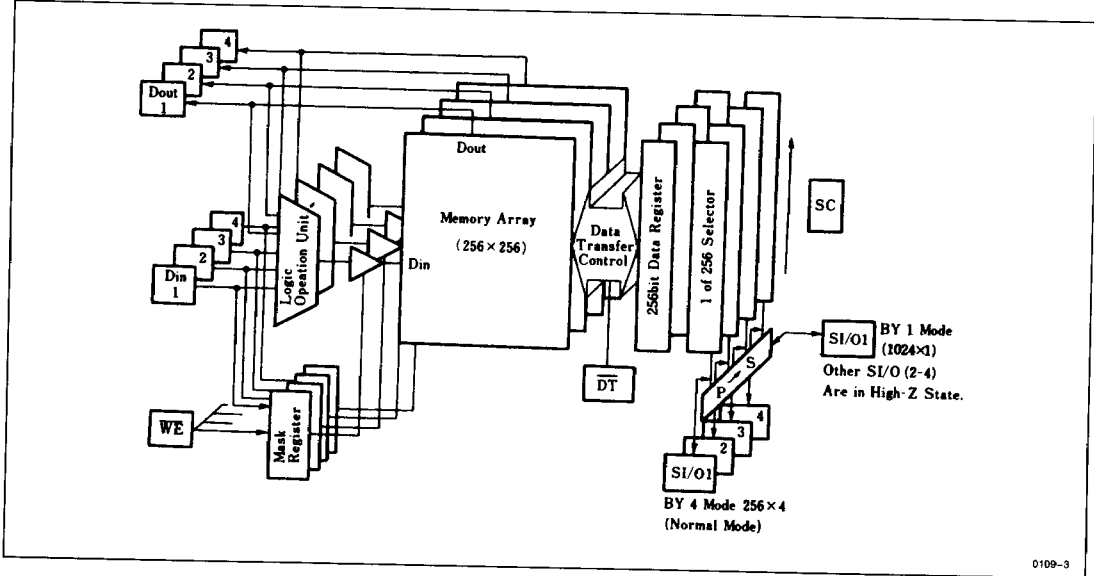
■ PIN OUT



■ PIN DESCRIPTION

| Pin Name | Function |
|--------------------------------------|-----------------------------|
| A ₀ -A ₇ | Address Input |
| I/O ₁ -I/O ₄ | RAM Port Data Input/Output |
| SI/O ₁ -SI/O ₄ | SAM Port Data Input/Output |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| SC | Serial Clock |
| WE | Write Enable |
| DT/OE | Data Transfer/Output Enable |
| SOE | SAM Port Enable |
| V _{CC} | Power Supply |
| V _{SS} | Ground |

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|--|------------------|----------------|------|
| Voltage on Any Pin Relative to V _{SS} | V _T | - 1.0 to + 7.0 | V |
| Power Supply Voltage Relative to V _{SS} | V _{CC} | - 0.5 to + 7.0 | V |
| Operating Temperature | T _{opr} | 0 to + 70 | °C |
| Storage Temperature | T _{stg} | - 55 to + 125 | °C |
| Short Circuit Output Current | I _{out} | 50 | mA |
| Power Dissipation | P _T | 1.0 | W |

■ INPUT/OUTPUT CAPACITANCE

| Parameter | Symbol | Typ | Max | Unit | Note |
|-----------|------------------|-----|-----|------|------|
| Address | C ₁₁ | — | 5 | pF | |
| Clocks | C ₁₂ | — | 5 | pF | |
| I/O, SI/O | C _{I/O} | — | 7 | pF | |

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--------------------|-----------------|-------|-----|-----|------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V | |
| Input High Voltage | V _{IH} | 2.4 | — | 6.5 | V | |
| Input Low Voltage | V _{IL} | - 0.5 | — | 0.8 | V | 2 |

- Notes: 1. All voltages referenced to V_{SS}.
 2. - 3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

| RAM Port | Symbol | SAM Port | | HM53462 -10 | HM53462 -12 | HM53462 -15 | Unit | Note |
|---|-------------------|----------|--------|----------------|----------------|----------------|------|------|
| | | Standby | Active | | | | | |
| Operating Current \overline{RAS} , \overline{CAS} Cycling t _{RC} = min | I _{CC1} | — | × | 70 | 60 | 50 | mA | |
| | I _{CC7} | × | — | 110 | 100 | 80 | mA | |
| Standby Current \overline{RAS} , \overline{CAS} = V _{IH} | I _{CC2} | — | × | 7 | 7 | 7 | mA | |
| | I _{CC8} | × | — | 40 | 40 | 30 | mA | |
| RAS Only Refresh Current CAS = V _{IH} , RAS Cycling t _{RC} = min | I _{CC3} | — | × | 60 | 50 | 40 | mA | |
| | I _{CC9} | × | — | 100 | 90 | 70 | mA | |
| Page Mode Current \overline{RAS} = V _{IL} , CAS Cycling t _{PC} = min | I _{CC4} | — | × | 50 | 40 | 35 | mA | |
| | I _{CC10} | × | — | 90 | 80 | 65 | mA | |
| CBR Refresh Current \overline{RAS} Cycling t _{RC} = min | I _{CC5} | — | X | 60 | 50 | 40 | mA | |
| | I _{CC11} | × | — | 100 | 90 | 70 | mA | |
| Data Transfer Current RAS, CAS Cycling t _{RC} = min | I _{CC6} | — | × | 75 | 65 | 55 | mA | |
| | I _{CC12} | × | — | 115 | 105 | 85 | mA | |

| Parameter | Symbol | Min | Max | Unit | Note |
|--|-----------------|------|-----|------|------|
| Input Leakage | I _{LI} | - 10 | 10 | μA | |
| Output Leakage | I _{LO} | - 10 | 10 | μA | |
| Output High Voltage I _{OH} = - 2 mA | V _{OH} | 2.4 | — | V | |
| Output Low Voltage I _{OL} = 4.2 mA | V _{OL} | — | 0.4 | V | |



• Electrical Characteristics and Recommended AC Operating Conditions

 $(T_A = 0 \text{ to } +70^\circ\text{C}, V_{CC} = 5V \pm 10\%, V_{SS} = 0V)^1, 10, 11$

| Parameter | Symbol | HM53462-10 | | HM53462-12 | | HM53462-15 | | Unit | Note |
|---|------------|------------|-------|------------|-------|------------|-------|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | t_{RC} | 190 | — | 220 | — | 260 | — | ns | |
| Read-Modify-Write Cycle Time | t_{RWC} | 260 | — | 300 | — | 355 | — | ns | |
| Page Mode Cycle Time | t_{PC} | 70 | — | 85 | — | 105 | — | ns | |
| Access Time from $\overline{\text{RAS}}$ | t_{RAC} | — | 100 | — | 120 | — | 150 | ns | 2, 3 |
| Access Time from CAS | t_{CAC} | — | 50 | — | 60 | — | 75 | ns | 3, 4 |
| Output Buffer Turn-off Delay Referenced to $\overline{\text{CAS}}$ | t_{OFF1} | 0 | 25 | 0 | 30 | 0 | 40 | ns | 5 |
| Transition Time (Rise and Fall) | t_T | 3 | 50 | 3 | 50 | 3 | 50 | ns | 6 |
| $\overline{\text{RAS}}$ Precharge Time | t_{RP} | 80 | — | 90 | — | 100 | — | ns | |
| $\overline{\text{RAS}}$ Pulse Width | t_{RAS} | 100 | 10000 | 120 | 10000 | 150 | 10000 | ns | |
| $\overline{\text{CAS}}$ Pulse Width | t_{CAS} | 50 | 10000 | 60 | 10000 | 75 | 10000 | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | t_{RCD} | 25 | 50 | 25 | 60 | 30 | 75 | ns | 7 |
| $\overline{\text{RAS}}$ Hold Time | t_{RSH} | 50 | — | 60 | — | 75 | — | ns | |
| $\overline{\text{CAS}}$ Hold Time | t_{CSH} | 100 | — | 120 | — | 150 | — | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | t_{CRP} | 10 | — | 10 | — | 10 | — | ns | |
| Row Address Setup Time | t_{ASR} | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | t_{RAH} | 15 | — | 15 | — | 20 | — | ns | |
| Column Address Setup Time | t_{ASC} | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | t_{CAH} | 20 | — | 20 | — | 25 | — | ns | |
| Write Command Setup Time | t_{WCS} | 0 | — | 0 | — | 0 | — | ns | 8 |
| Write Command Hold Time | t_{WCH} | 25 | — | 25 | — | 30 | — | ns | |
| Write Command Pulse Width | t_{WCP} | 15 | — | 20 | — | 25 | — | ns | |
| Write Command to $\overline{\text{RAS}}$ Lead Time | t_{RWL} | 35 | — | 40 | — | 45 | — | ns | |
| Write Command to CAS Lead Time | t_{CWL} | 35 | — | 40 | — | 45 | — | ns | |
| Data-in Setup Time | t_{DS} | 0 | — | 0 | — | 0 | — | ns | 9 |
| Data-in Hold Time | t_{DH} | 25 | — | 25 | — | 30 | — | ns | 8, 9 |
| Read Command Setup Time | t_{RCS} | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time | t_{RCH} | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time Referenced to $\overline{\text{RAS}}$ | t_{RRH} | 10 | — | 10 | — | 10 | — | ns | |
| Refresh Period | t_{REF} | — | 4 | — | 4 | — | 4 | ms | |
| $\overline{\text{RAS}}$ Pulse Width (Read-Modify-Write Cycle) | t_{RWS} | 170 | 10000 | 200 | 10000 | 245 | 10000 | ns | |
| CAS to $\overline{\text{WE}}$ Delay | t_{CWD} | 85 | — | 100 | — | 125 | — | ns | 8 |
| CAS Setup Time (CAS Before $\overline{\text{RAS}}$ Refresh) | t_{CSR} | 10 | — | 10 | — | 10 | — | ns | |
| CAS Hold Time (CAS Before $\overline{\text{RAS}}$ Refresh) | t_{CHR} | 20 | — | 25 | — | 30 | — | ns | |
| $\overline{\text{RAS}}$ Precharge to CAS Hold Time | t_{RPC} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{CAS}}$ Precharge Time | t_{CP} | 10 | — | 15 | — | 20 | — | ns | |
| Access Time from $\overline{\text{OE}}$ | t_{OAC} | — | 30 | — | 35 | — | 40 | ns | |
| Output Buffer Turn-off Delay Referenced to $\overline{\text{OE}}$ | t_{OFF2} | 0 | 25 | 0 | 30 | 0 | 40 | ns | |
| $\overline{\text{OE}}$ to Data-in Delay Time | t_{ODD} | 25 | — | 30 | — | 40 | — | ns | |
| $\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$ | t_{OEH} | 10 | — | 15 | — | 20 | — | ns | |



• Electrical Characteristics and Recommended AC Operating Conditions (continued)

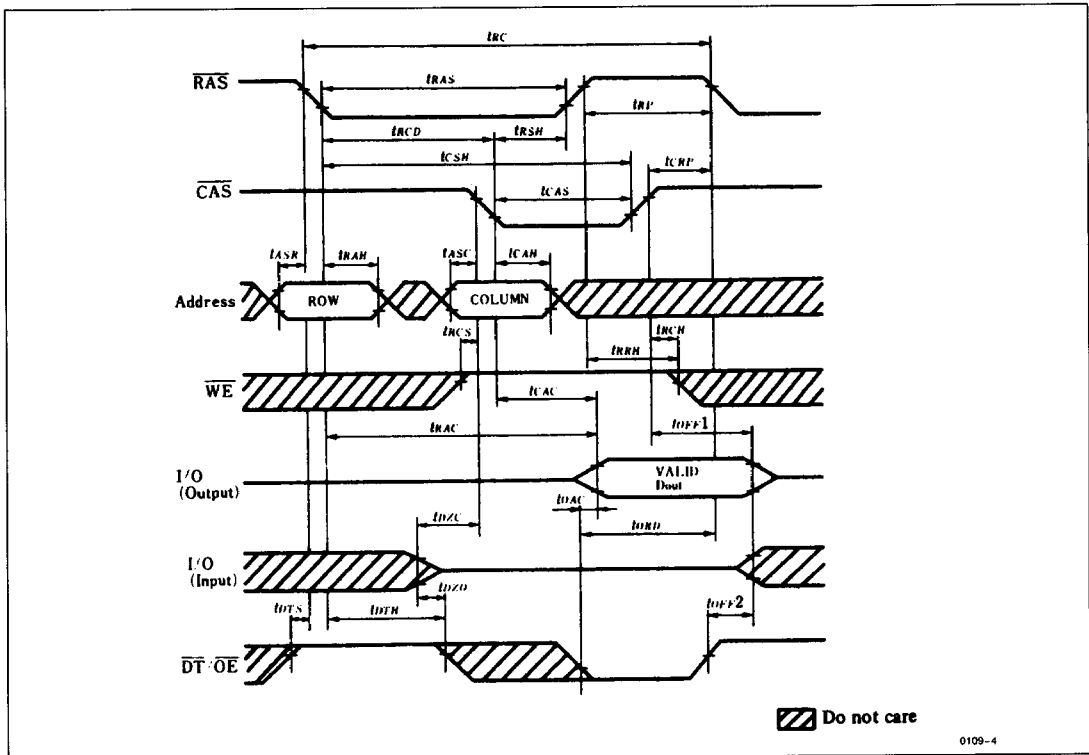
 $(T_A = 0 \text{ to } +70^\circ\text{C}, V_{CC} = 5V \pm 10\%, V_{SS} = 0V)^{1, 10, 11}$

| Parameter | Symbol | HM53462-10 | | HM53462-12 | | HM53462-15 | | Unit | Note |
|---|------------|------------|-----|------------|-----|------------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Data-in to $\overline{\text{CAS}}$ Delay Time | t_{DZC} | 0 | — | 0 | — | 0 | — | ns | |
| Data-in to $\overline{\text{OE}}$ Delay Time | t_{DZO} | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Delay Time | t_{ORD} | 35 | — | 40 | — | 45 | — | ns | |
| Serial Clock Cycle Time | t_{SCC} | 40 | — | 40 | — | 60 | — | ns | |
| Access Time from SC | t_{SCA} | — | 40 | — | 40 | — | 60 | ns | 10 |
| Access Time from $\overline{\text{SOE}}$ | t_{SEA} | — | 25 | — | 30 | — | 40 | ns | 10 |
| SC Pulse Width | t_{SC} | 10 | — | 10 | — | 10 | — | ns | |
| SC Precharge Width | t_{SCP} | 10 | — | 10 | — | 10 | — | ns | |
| Serial Data-out Hold Time after SC High | t_{SOH} | 10 | — | 10 | — | 10 | — | ns | |
| Serial Output Buffer Turn-off Delay from $\overline{\text{SOE}}$ | t_{SEZ} | 0 | 25 | 0 | 25 | 0 | 30 | ns | |
| Serial Data-in Setup Time | t_{SIS} | 0 | — | 0 | — | 0 | — | ns | |
| Serial Data-in Hold Time | t_{SIH} | 15 | — | 20 | — | 25 | — | ns | |
| $\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Setup Time | t_{DTS} | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Hold Time (Read Transfer Cycle) | t_{RDH} | 80 | — | 90 | — | 110 | — | ns | |
| $\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Hold Time | t_{DTH} | 15 | — | 15 | — | 20 | — | ns | |
| $\overline{\text{DT}}$ to $\overline{\text{CAS}}$ Hold Time | t_{CDH} | 20 | — | 30 | — | 45 | — | ns | |
| Last SC to $\overline{\text{DT}}$ Delay Time | t_{SDD} | 5 | — | 5 | — | 10 | — | ns | |
| First SC to $\overline{\text{DT}}$ Hold Time | t_{SDH} | 25 | — | 25 | — | 30 | — | ns | |
| $\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Delay Time | t_{DTR} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Setup Time | t_{WS} | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Hold Time | t_{WH} | 15 | — | 15 | — | 20 | — | ns | |
| I/O to $\overline{\text{RAS}}$ Setup Time | t_{MS} | 0 | — | 0 | — | 0 | — | ns | |
| I/O to $\overline{\text{RAS}}$ Hold Time | t_{MH} | 15 | — | 15 | — | 20 | — | ns | |
| Serial Output Buffer Turn-off Delay from $\overline{\text{RAS}}$ | t_{SRZ} | 10 | 50 | 10 | 60 | 10 | 75 | ns | |
| SC to $\overline{\text{RAS}}$ Setup Time | t_{SRS} | 30 | — | 40 | — | 45 | — | ns | |
| $\overline{\text{RAS}}$ to SC Delay Time | t_{SRD} | 25 | — | 30 | — | 35 | — | ns | |
| Serial Data Input Delay Time from $\overline{\text{RAS}}$ | t_{SID} | 50 | — | 60 | — | 75 | — | ns | |
| Serial Data Input to $\overline{\text{DT}}$ Delay Time | t_{SZD} | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{\text{SOE}}$ to $\overline{\text{RAS}}$ Setup Time | t_{ES} | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{\text{SOE}}$ to $\overline{\text{RAS}}$ Hold Time | t_{EH} | 15 | — | 15 | — | 20 | — | ns | |
| Serial Write Enable Setup Time | t_{SWS} | 0 | — | 0 | — | 0 | — | ns | |
| Serial Write Enable Hold Time | t_{SWH} | 35 | — | 35 | — | 55 | — | ns | |
| Serial Write Disable Setup Time | t_{SWIS} | 0 | — | 0 | — | 0 | — | ns | |
| Serial Write Disable Hold Time | t_{SWIH} | 35 | — | 35 | — | 55 | — | ns | |
| $\overline{\text{DT}}$ to Sout in Low-Z Delay Time | t_{DLZ} | 5 | — | 10 | — | 10 | — | ns | |

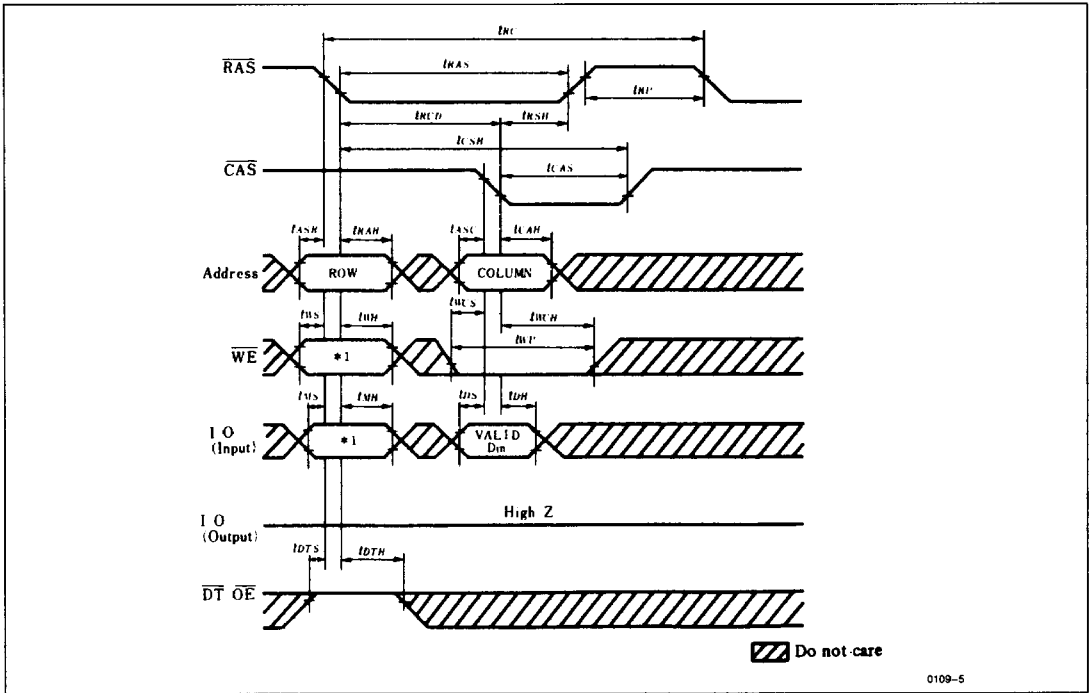
- Notes:
1. AC measurements assume $t_f = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
 5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 8. t_{WC} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WC} \geq t_{WC}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycle and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 10. Measured with a load circuit equivalent to 2 TTL and 100 pF.
 11. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of RAS, $\overline{\text{WE}} = \text{"Low"}$ and $\text{I/O}_1\text{-I/O} = \text{"High"}$), and execute one or more transport cycle for initiation of SAM port.

■ TIMING WAVEFORMS

• Read Cycle

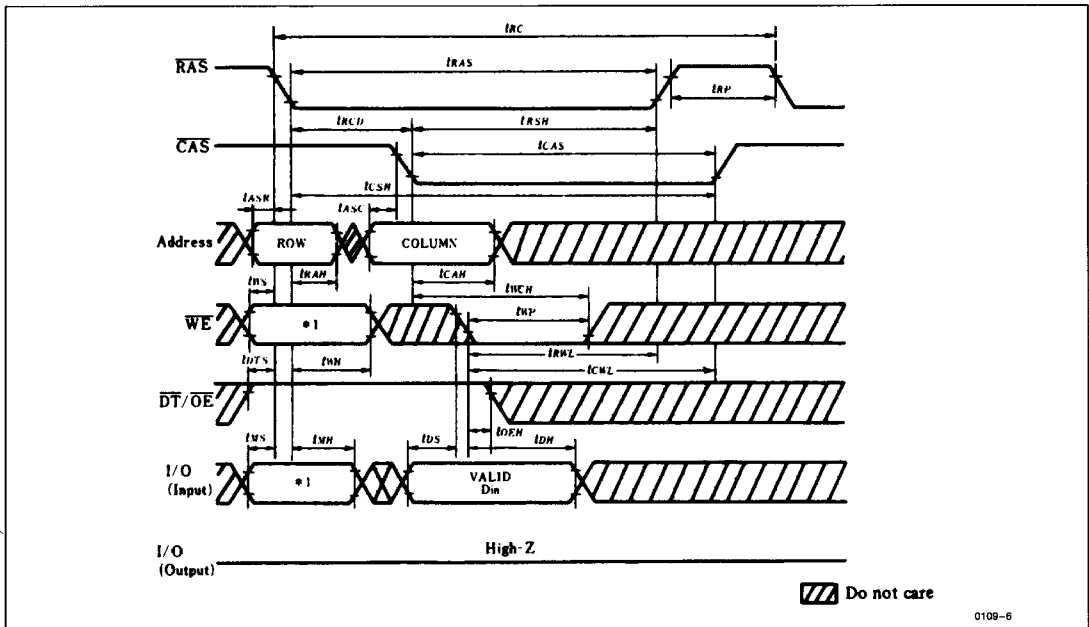


• Early Write Cycle



Notes: *1. When \overline{WE} is "H" level, then all data on the I/O can be written into the cell. When \overline{WE} is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of RAS.

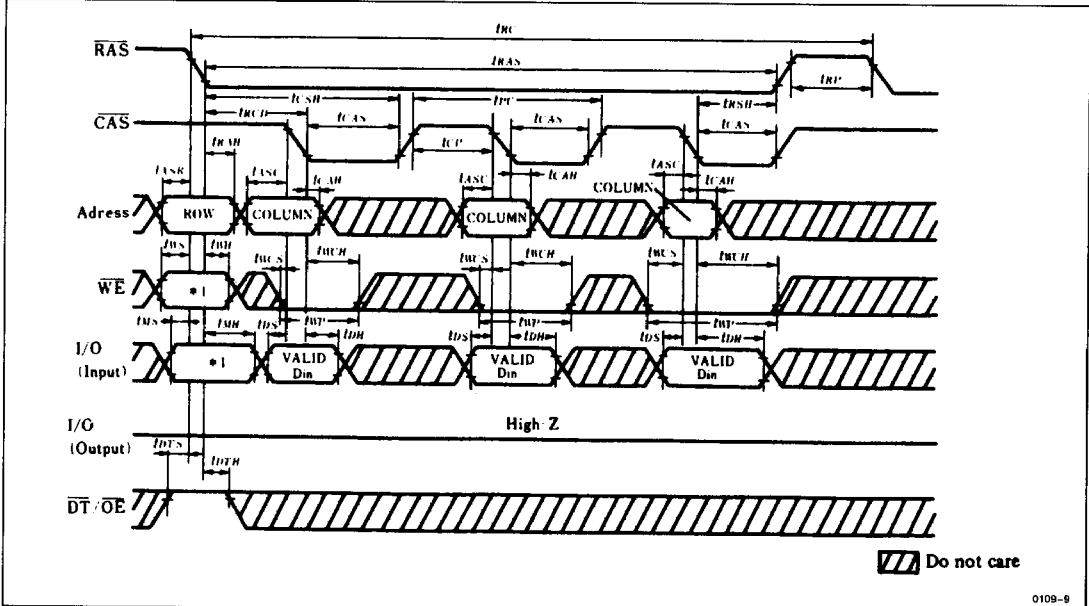
• Delayed Write Cycle



Note: *1. When \overline{WE} is "H" level, all the data on I/O₁–I/O₄ can be written into the memory cell. When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.



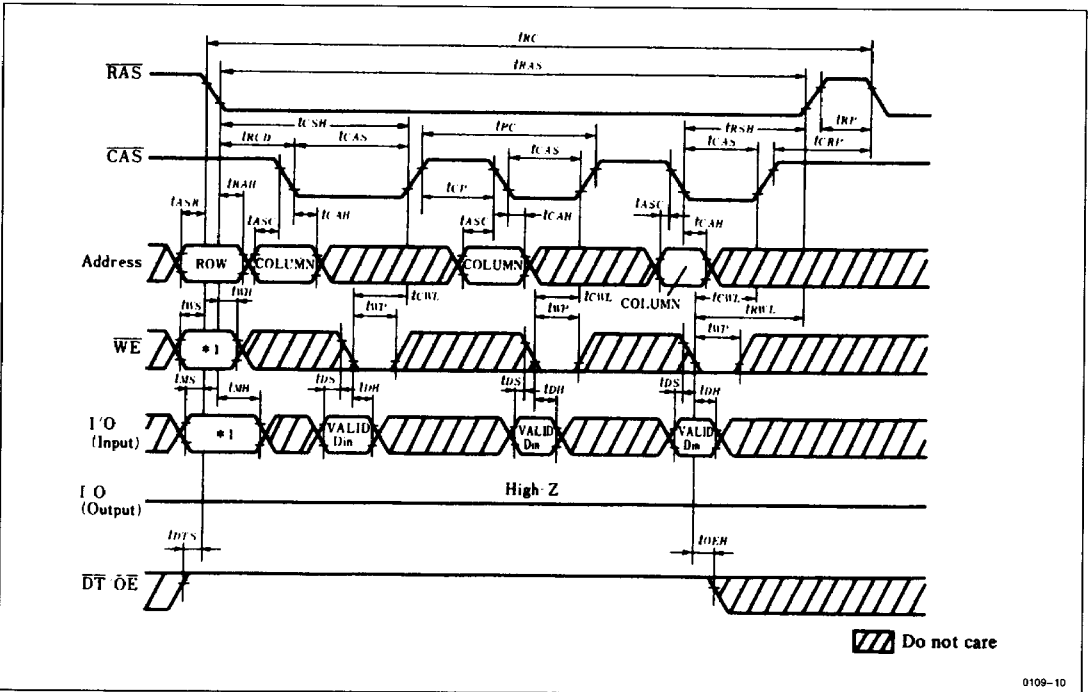
• Page Mode Write Cycle (Early Write)



0109-9

Note: *1. When \overline{WE} is "H" level, all the data on I/O₁-I/O₄ can be written into the memory cell. When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.

• Page Mode Write Cycle (Delayed Write)

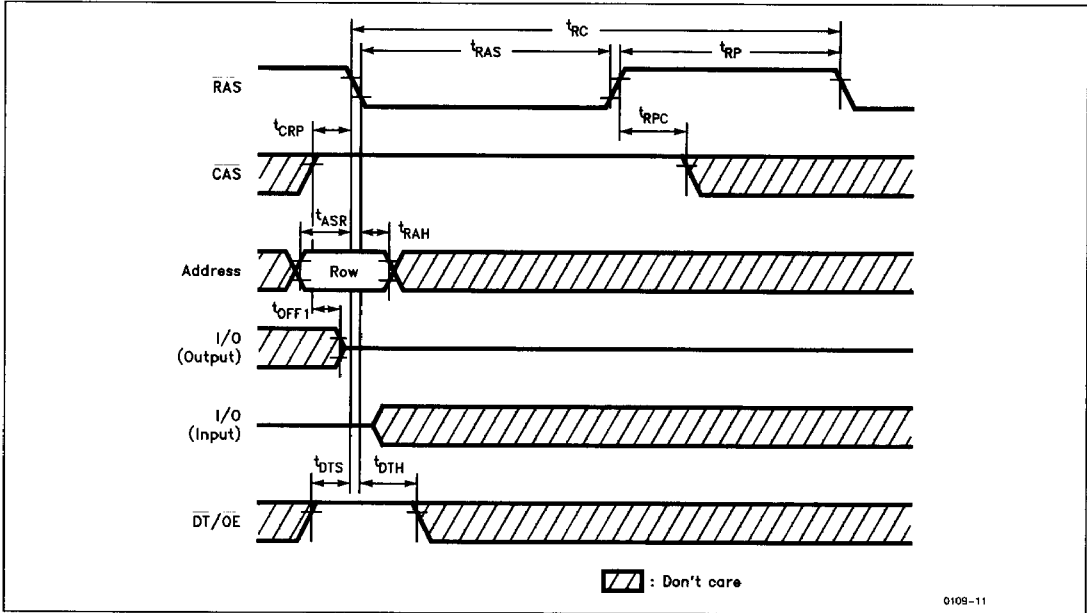


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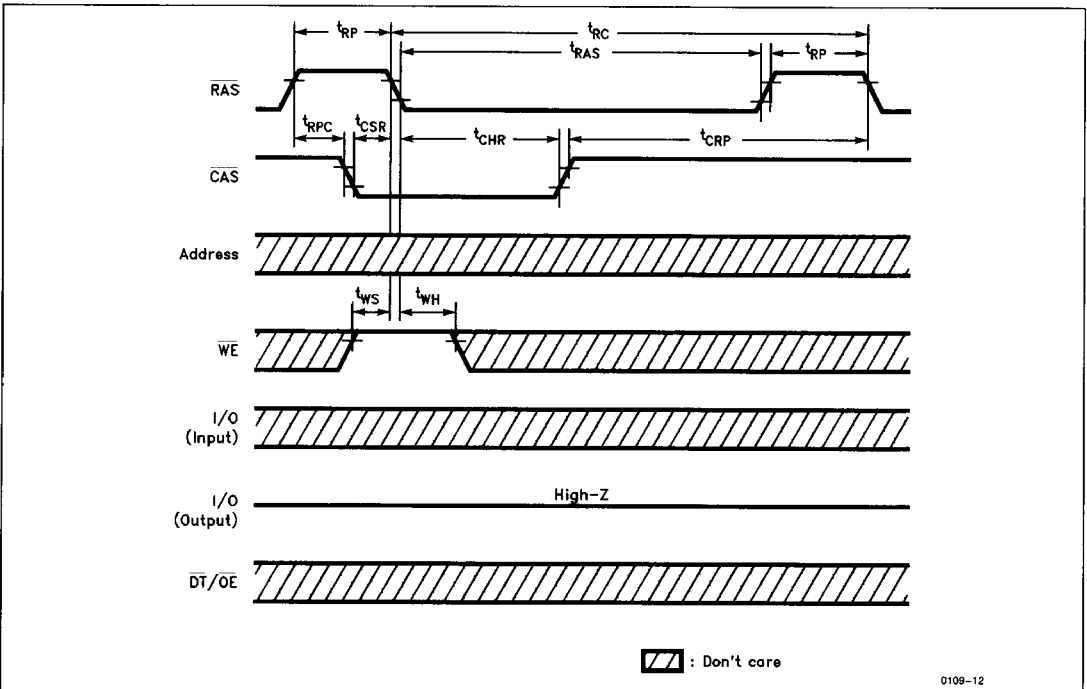
Note: *1. When \overline{WE} is "H" level, all the data on I/O₁-I/O₄ can be written into the memory cell. When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.



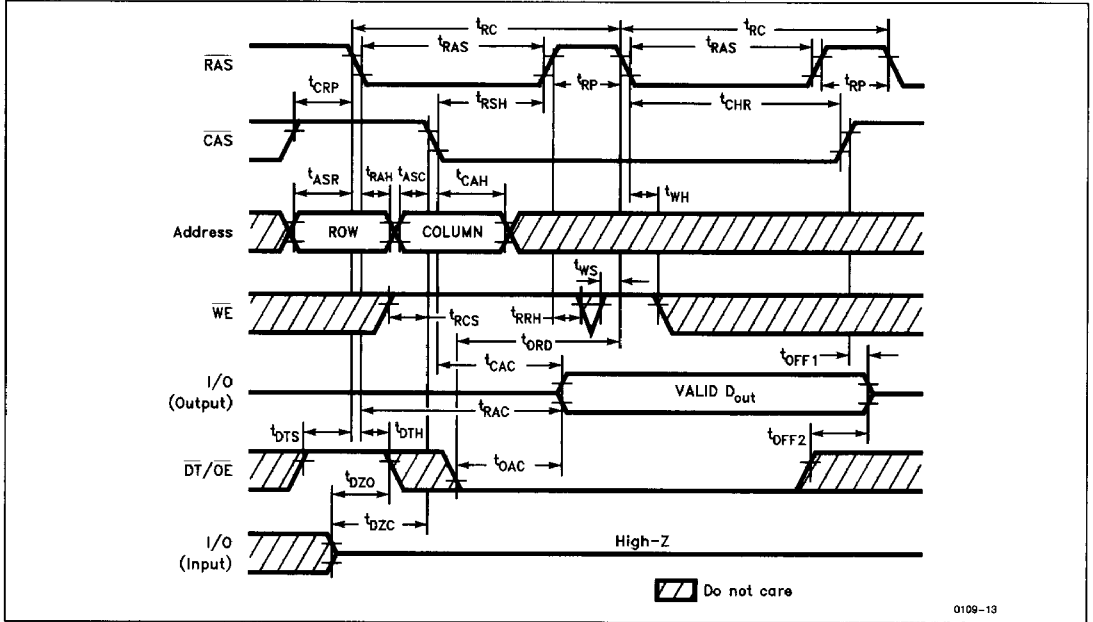
• **RAS Only Refresh Cycle**



• **CAS Before RAS Refresh Cycle**

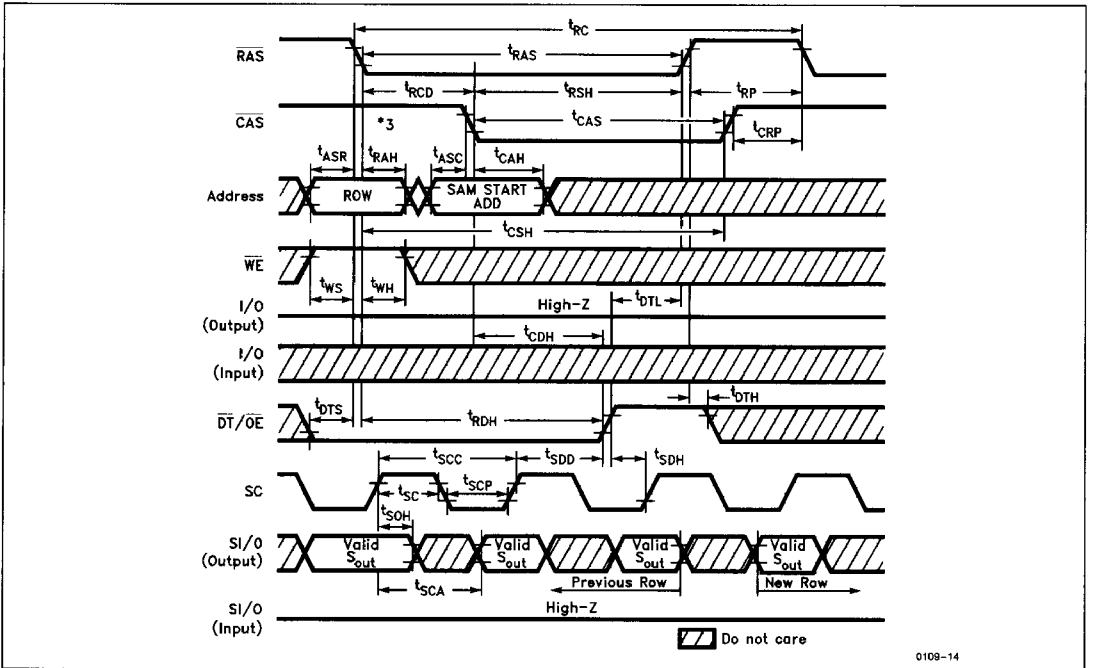


• Hidden Refresh Cycle



0109-13

• Read Transfer Cycle (1)*1, *2

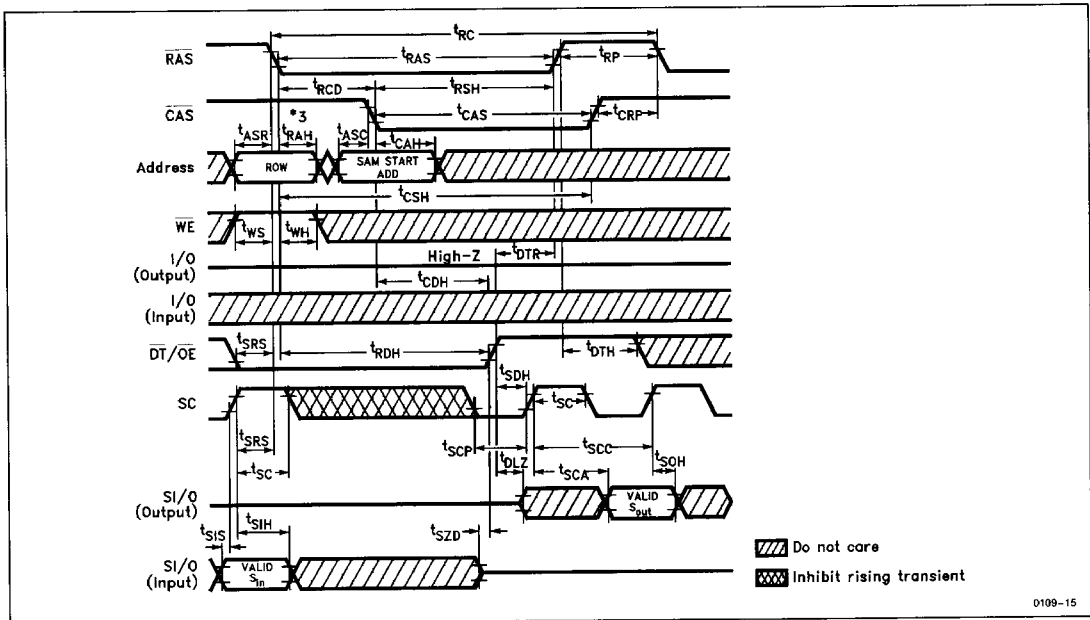


0109-14

- Notes: *1. In the case that the previous data transfer cycle was read transfer.
 *2. Assume that SOE is "Low".
 *3. CAS and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.



• Read Transfer Cycle (2)^{*1, *2}



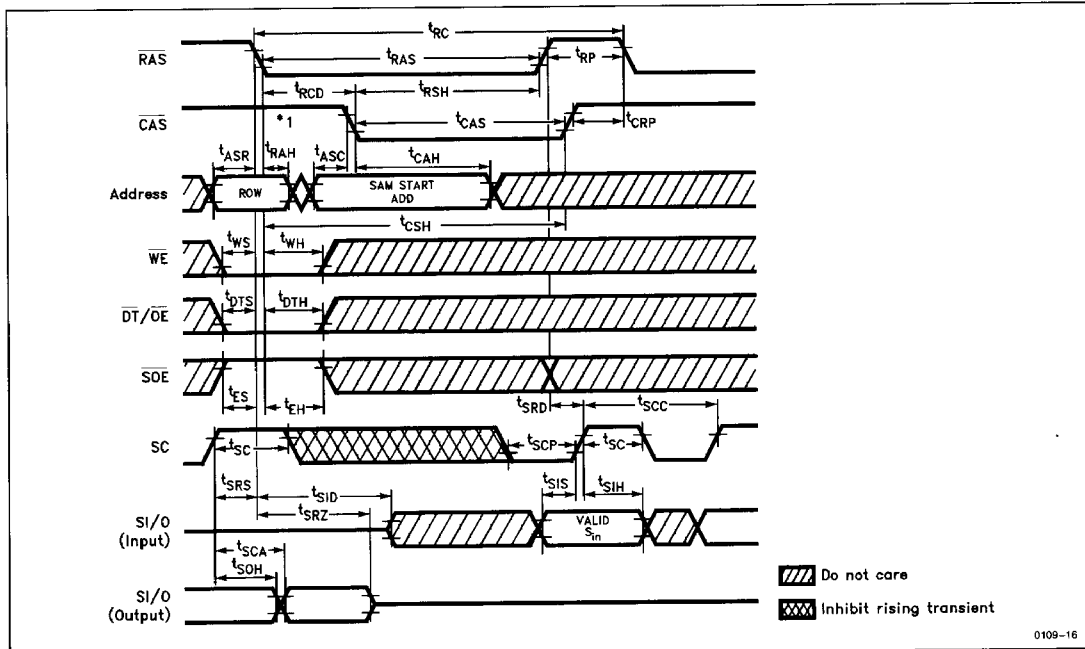
0109-15

Notes: *1. In the case that the previous data transfer cycle was read transfer.

*2. Assume that SOE is "Low".

*3. CAS and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• Pseudo Transfer Cycle

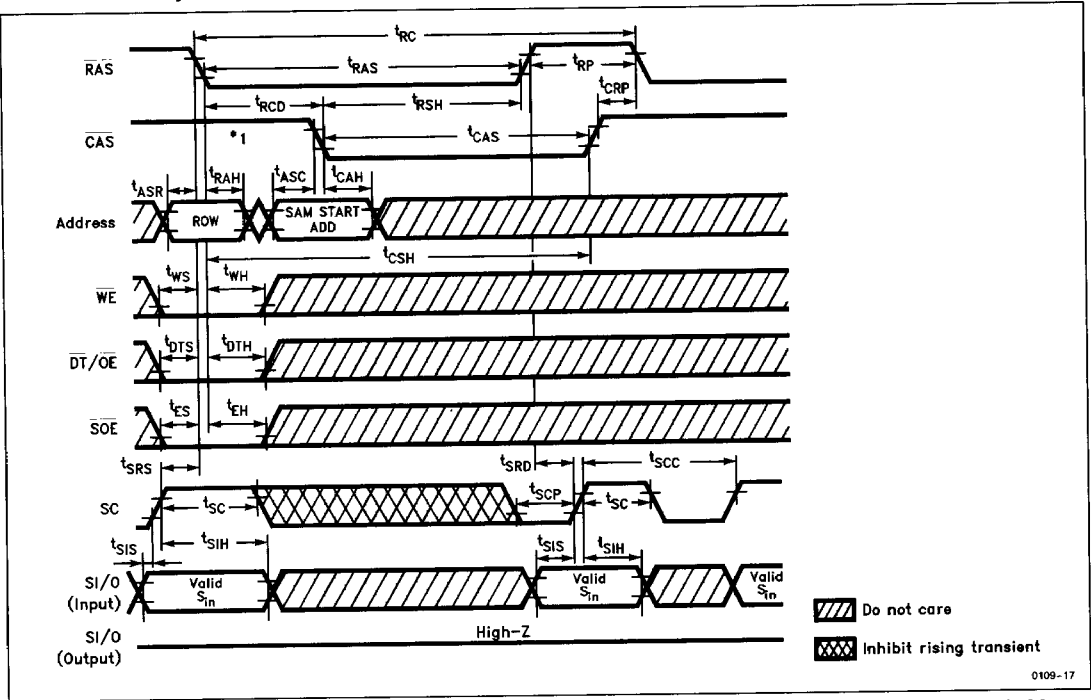


0109-16

Note: *1. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

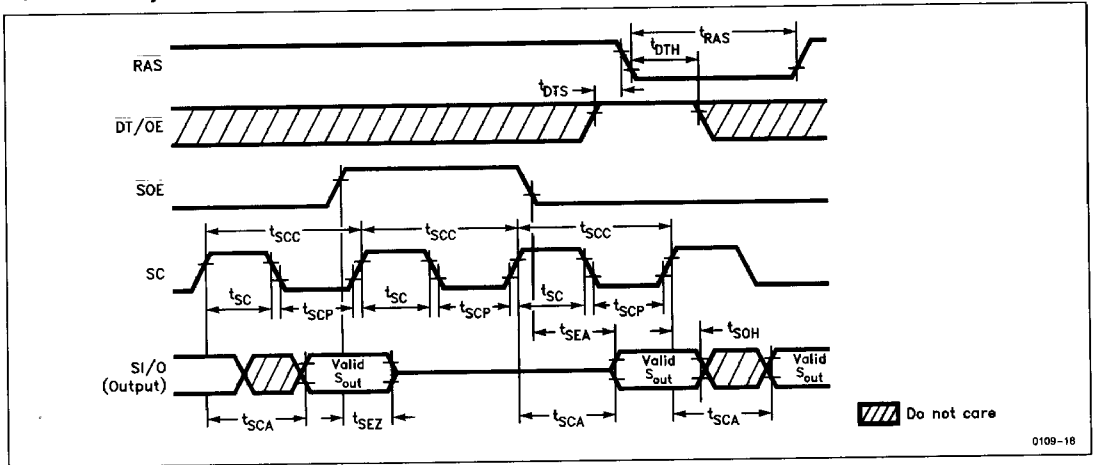


• Write Transfer Cycle

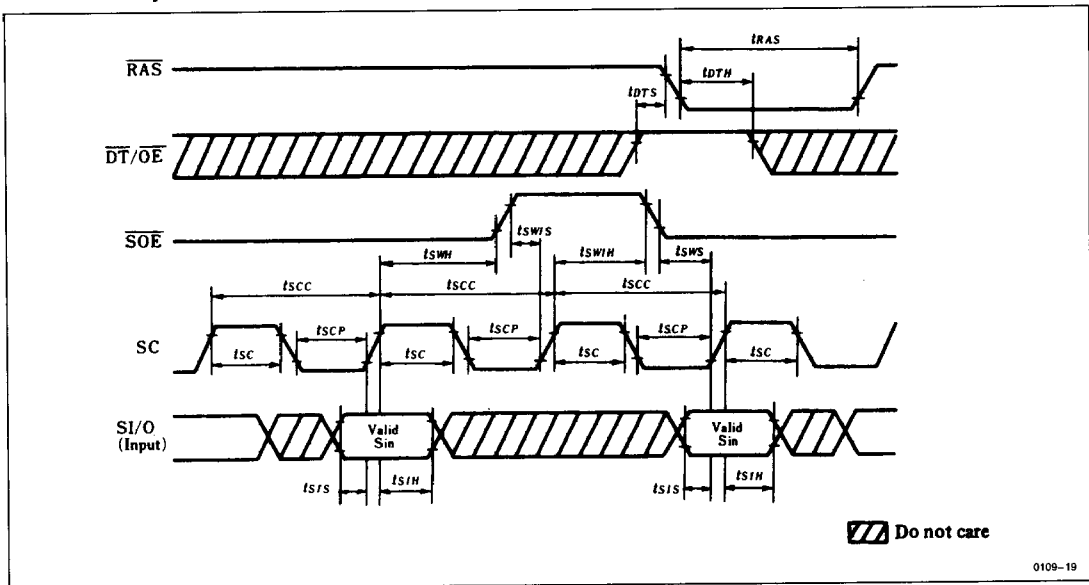


Note: *1. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Serial Read Cycle



• Serial Write Cycle



0109-19

• Electrical AC Characteristics (Logic Operation Mode)

| Parameter | Symbol | HM53462-10 | | HM53462-12 | | HM53462-15 | | Unit | Note |
|--|------------|------------|-------|------------|-------|------------|-------|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{FRC} | 230 | — | 265 | — | 310 | — | ns | |
| RAS Pulse Width in Write Cycle | t_{RFS} | 140 | 10000 | 165 | 10000 | 200 | 10000 | ns | |
| CAS Pulse Width in Write Cycle | t_{CFS} | 80 | 10000 | 95 | 10000 | 105 | 10000 | ns | |
| CAS Hold Time in Write Cycle | t_{FCSH} | 140 | — | 165 | — | 200 | — | ns | |
| RAS Hold Time in Write Cycle | t_{FRSH} | 80 | — | 95 | — | 105 | — | ns | |
| Page Mode Cycle Time (Write Cycle) | t_{FPC} | 100 | — | 120 | — | 135 | — | ns | |
| CAS Hold Time (Logic Operation Set/Reset Cycle) | t_{FCHR} | 90 | — | 100 | — | 120 | — | ns | |
| CAS Hold Time from RAS Precharge (x4 → x1 Set Cycle) | t_{PSCH} | 10 | — | 10 | — | 10 | — | ns | |



• Logic Code (FC0-3 are AX0-AX3 in Logic Operation Set Cycle)

| FC3 | FC2 | FC1 | FC0 | LOGIC | |
|-----|-----|-----|-----|---------|---|
| | | | | Symbol | Write Data |
| 0 | 0 | 0 | 0 | 0 | Zero |
| 0 | 0 | 0 | 1 | AND1 | $D_i \cdot M_i$ |
| 0 | 0 | 1 | 0 | AND2 | $\overline{D_i} \cdot M_i$ |
| 0 | 0 | 1 | 1 | X4 → X1 | — |
| 0 | 1 | 0 | 0 | AND3 | $D_i \cdot \overline{M_i}$ |
| 0 | 1 | 0 | 1 | THROUGH | D_i |
| 0 | 1 | 1 | 0 | EOR | $\overline{D_i} \cdot M_i + D_i \cdot \overline{M_i}$ |
| 0 | 1 | 1 | 1 | OR1 | $D_i + M_i$ |
| 1 | 0 | 0 | 0 | NOR | $\overline{D_i} \cdot \overline{M_i}$ |
| 1 | 0 | 0 | 1 | ENOR | $D_i \cdot M_i + \overline{D_i} \cdot \overline{M_i}$ |
| 1 | 0 | 1 | 0 | INV1 | $\overline{D_i}$ |
| 1 | 0 | 1 | 1 | OR2 | $\overline{D_i} + M_i$ |
| 1 | 1 | 0 | 0 | INV2 | $\overline{M_i}$ |
| 1 | 1 | 0 | 1 | OR3 | $D_i + \overline{M_i}$ |
| 1 | 1 | 1 | 0 | NAND | $\overline{D_i} + \overline{M_i}$ |
| 1 | 1 | 1 | 1 | 1 | ONE |

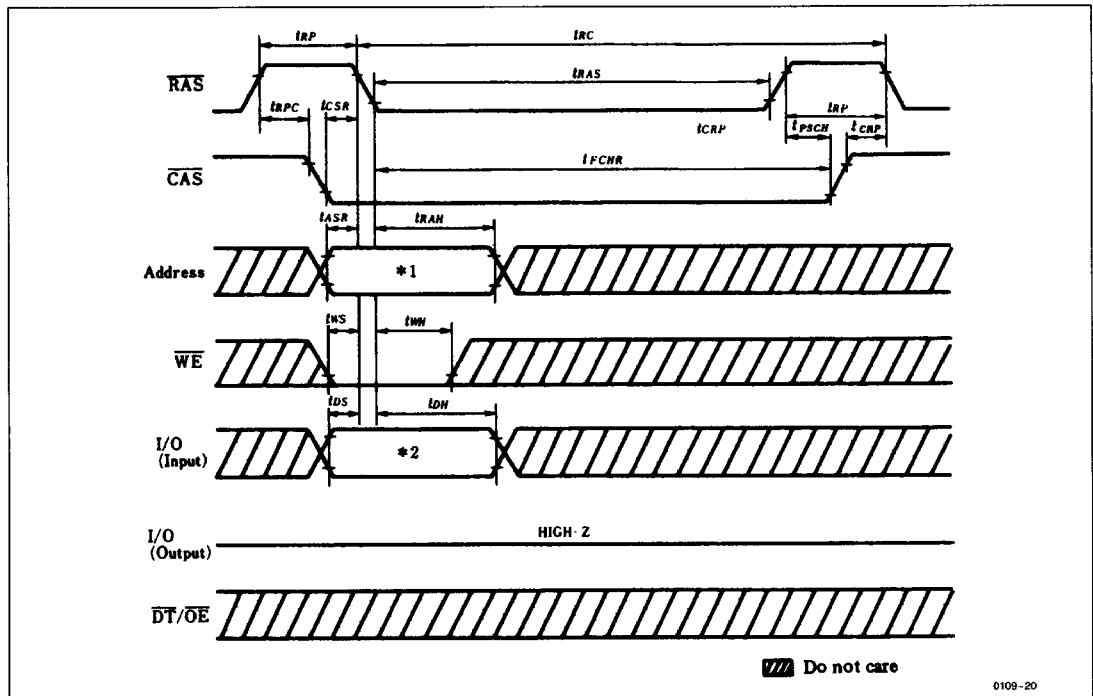
→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

D_i : External Data-in

M_i : The Data of the Memory Cell

• Logic Operation Set Reset Cycle (With \overline{CAS} Before \overline{RAS} Refresh)

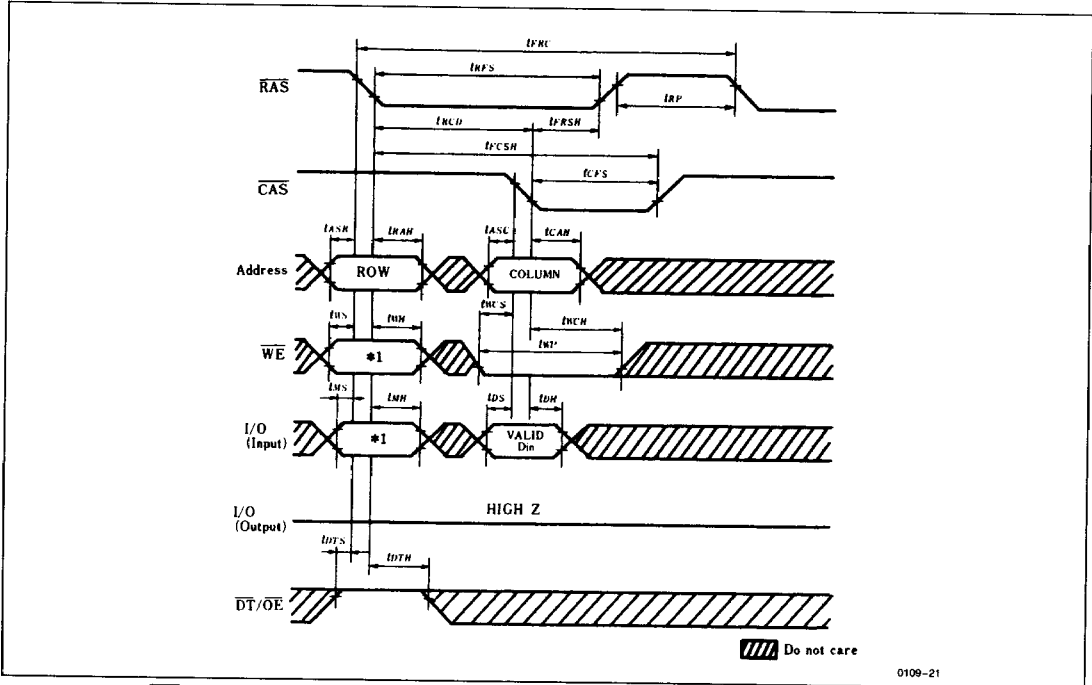


Notes: *1. Logic code A₀-A₃ (A₄-A₇: don't care)
 *2. Write mask data.



■ LOGIC OPERATION MODE

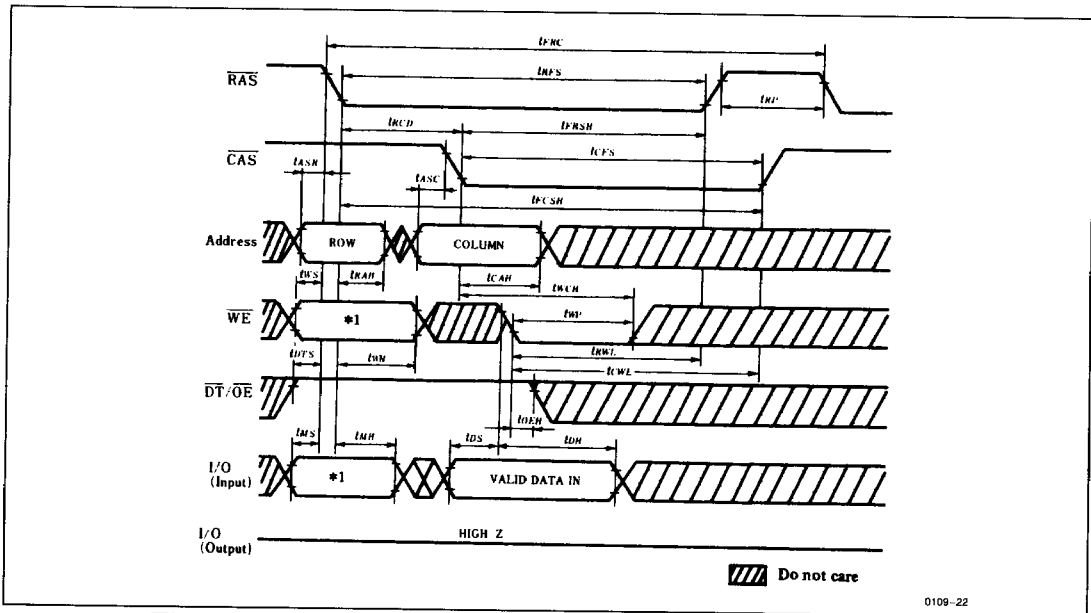
• Early Write Cycle



0109-21

Note: *1. When $\overline{\text{WE}}$ is "high", the all data on the I/O can be written into the cell. When $\overline{\text{WE}}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{\text{RAS}}$.

• Delayed Write Cycle

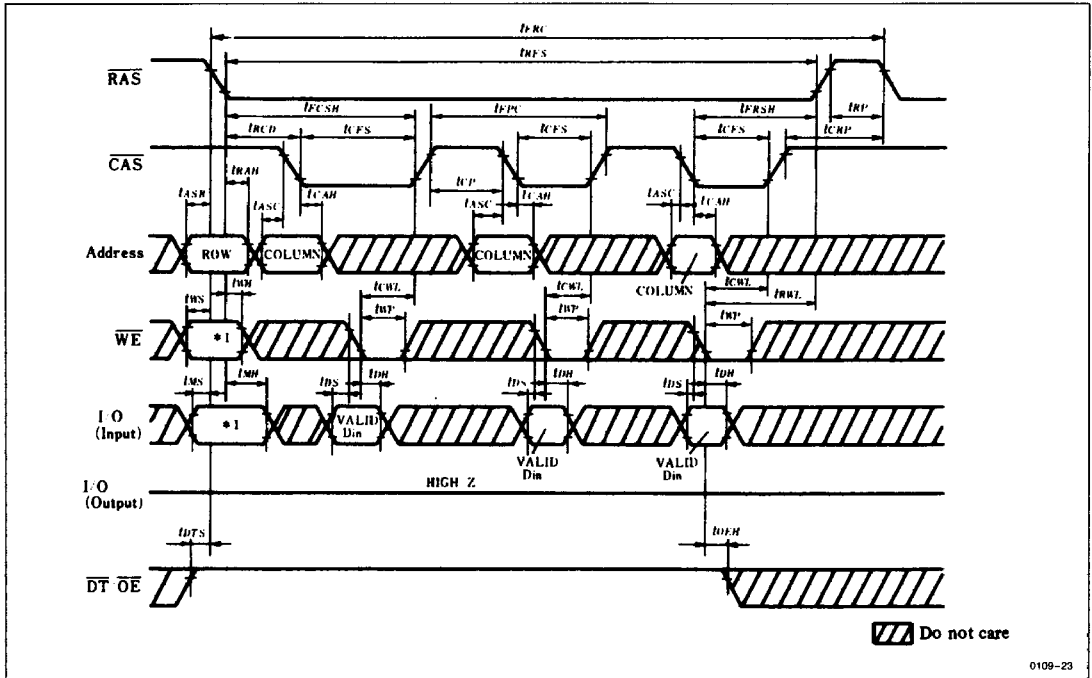


0109-22

Note: *1. When $\overline{\text{WE}}$ is "H" level, all the data on I/O₁₋₄ can be written into the memory cell. When $\overline{\text{WE}}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{\text{RAS}}$.



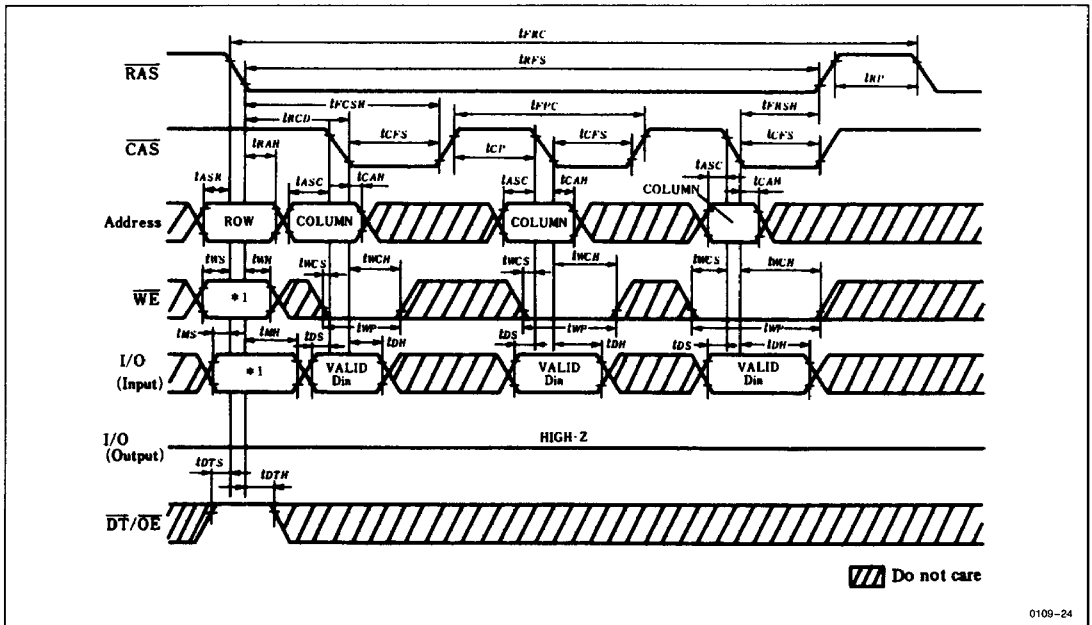
• Page Mode Write Cycle (Delayed Write)



0109-23

Note: *1. When \overline{WE} is "high", the all data on the I/O can be written into the cell. When \overline{WE} is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of RAS.

• Page Mode Write Cycle (Early Write)



0109-24

Note: *1. When \overline{WE} is "high", the all data on the I/O can be written into the cell. When \overline{WE} is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of RAS.



■ DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between D_{in} and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing \overline{CAS} and \overline{WE} low when \overline{RAS} falls (Fig. 1). The logic code and the bits to be masked are determined respectively by $AX0-3$ state and I/O_{1-4} state at the falling edge of \overline{RAS} . Furthermore, in this cycle \overline{CAS} before \overline{RAS} refresh operation is executed, too. In this case of executing the conventional \overline{CAS} before \overline{RAS} refresh operation, \overline{WE} must be high when \overline{RAS} falls.

2.1 Logic Code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is $(AX3, AX2, AX1, AX0) = (0, 0, 1, 1)$, the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1024×1 , one data transfer cycle is needed to initialize the SAM selector.

One the SAM organization is changed to 1024×1 , this code is maintained unless power is turned off.

2.2 Write Mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing \overline{WE} low at the falling edge of \overline{RAS} during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

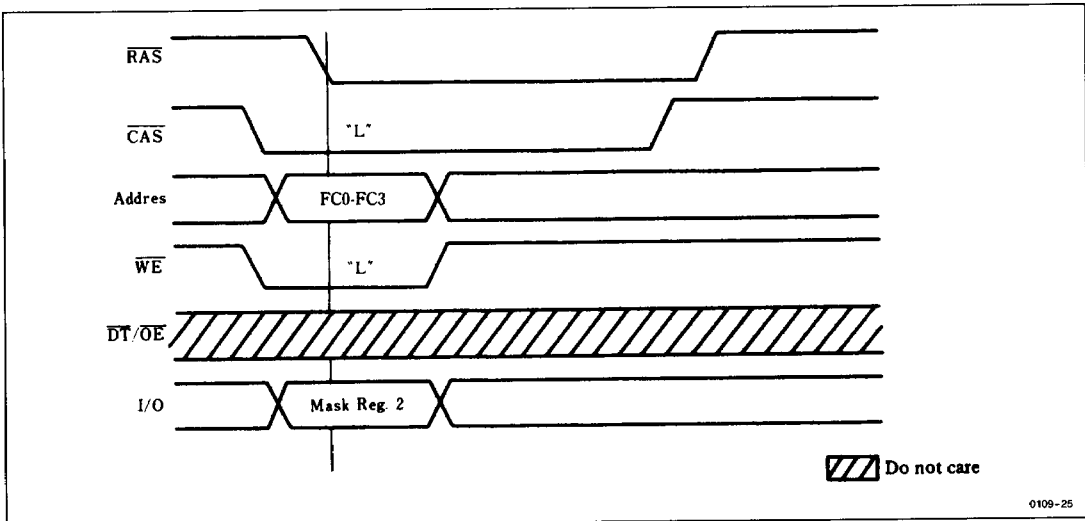


Figure 1. Logic Operation Set/Reset Cycle

• Table 1. Logic Code (FC0-FC3 are AX0-AX3 in Logic Operation Set Cycle)

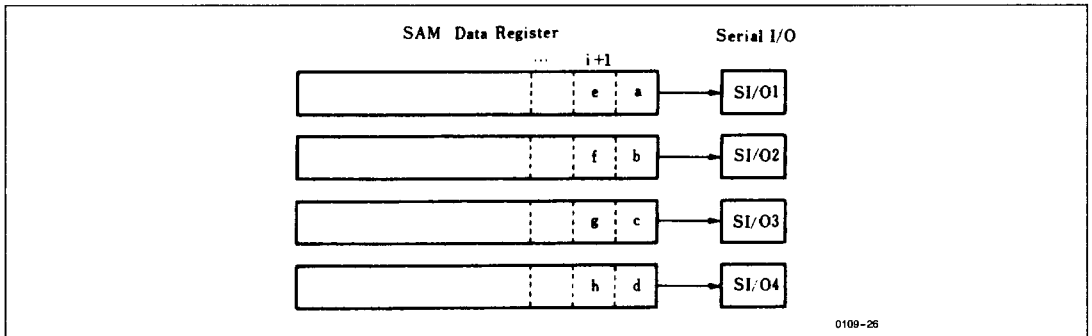
| FC3 | FC2 | FC1 | FC0 | LOGIC | |
|-----|-----|-----|-----|---------|---|
| | | | | Symbol | Write Data |
| 0 | 0 | 0 | 0 | 0 | Zero |
| 0 | 0 | 0 | 1 | AND1 | $D_i \cdot M_i$ |
| 0 | 0 | 1 | 0 | AND2 | $\overline{D_i} \cdot M_i$ |
| 0 | 0 | 1 | 1 | X4 → X1 | — |
| 0 | 1 | 0 | 0 | AND3 | $D_i \cdot \overline{M_i}$ |
| 0 | 1 | 0 | 1 | THROUGH | D_i |
| 0 | 1 | 1 | 0 | EOR | $\overline{D_i} \cdot M_i + D_i \cdot \overline{M_i}$ |
| 0 | 1 | 1 | 1 | OR1 | $D_i + M_i$ |
| 1 | 0 | 0 | 0 | NOR | $\overline{D_i} \cdot \overline{M_i}$ |
| 1 | 0 | 0 | 1 | ENOR | $D_i \cdot M_i + \overline{D_i} \cdot \overline{M_i}$ |
| 1 | 0 | 1 | 0 | INV1 | $\overline{D_i}$ |
| 1 | 0 | 1 | 1 | OR2 | $\overline{D_i} + M_i$ |
| 1 | 1 | 0 | 0 | INV2 | $\overline{M_i}$ |
| 1 | 1 | 0 | 1 | OR3 | $D_i + \overline{M_i}$ |
| 1 | 1 | 1 | 0 | NAND | $\overline{D_i} \cdot \overline{M_i}$ |
| 1 | 1 | 1 | 1 | 1 | ONE |

→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

D_i :External Data-in

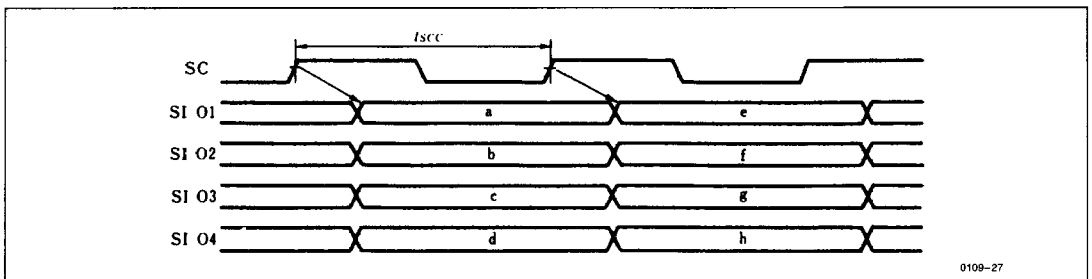
M_i :The Data of the Memory Cell



0109-26

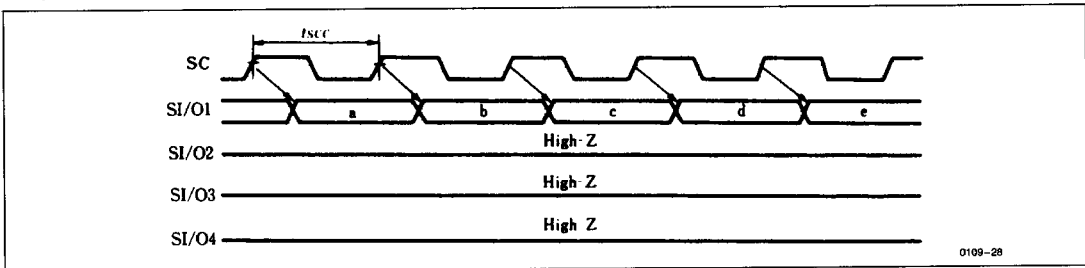
Figure 2. The Shift Way of SAM Data

1) By 4 Mode (SAM Organization: 256 x 4)



0109-27

2) By 1 Mode (SAM Organization: 1024 x 1)



0109-28

| | Logic operation set/reset cycle | Write cycle | Write cycle | Write cycle | Write cycle |
|-------|--|-------------|--|-------------|-------------|
| RAS | | | | | |
| CAS | "L" | "H" | "H" | "H" | "H" |
| WE | "L" | "H" | "L" | "H" | "H" |
| I/O1 | | "0" Write | Masked | "1" Write | "0" Write |
| I/O2 | | Masked | "1" Write | Masked | Masked |
| I/O3 | | Masked | "0" Write | Masked | Masked |
| I/O4 | | "1" Write | Masked | "0" Write | "1" Write |
| Logic | — | AND1 | THROUGH | AND1 | AND1 |
| | Mask reg.2 is set I O2,3 :Masked Assume that the logic is set to "AND1". | | Mask reg.1 is set, and valid only in this cycle. I O1,4:Masked | | |

0109-29

Figure 3. Example of Logic Operation Mode