μPD41464
65,536 x 4-Bit
Dynamic NMOS RAM

Description

The μPD41464 is a 65,536-word by 4-bit dynamic RAM designed to operate from a single + 5-volt power supply and fabricated with a double polylayer, N-channel silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry ensure minimum power dissipation, while an on-chip feature internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held by holding $\overline{CAS}$ low. Data input and output is returned to high impedance by returning $\overline{CAS}$ high. Hidden refreshing allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address, by means of $\overline{RAS}$-only refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

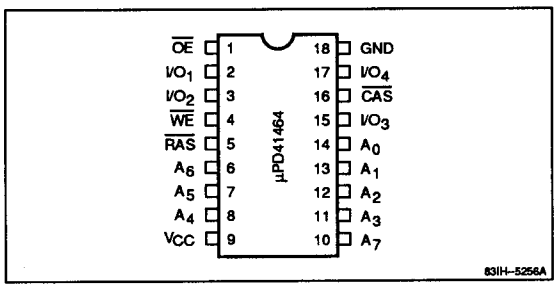
- 65,536-word by 4-bit organization
- Single + 5-volt ±10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Low power dissipation
  - —28 mA max (standby)
  - —440 mW (active, t_{RC} = t_{RC} min)
- Nonlatched, TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Standard 18-pin plastic DIP and PLCC packaging

Ordering Information

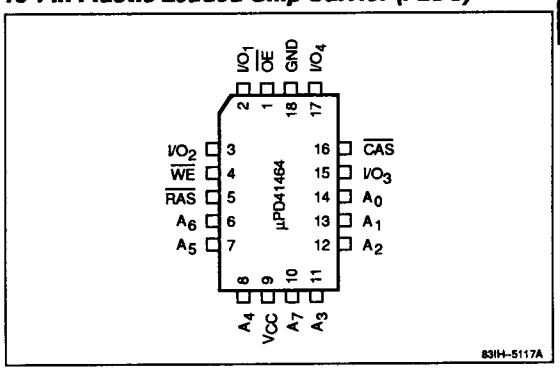
Part Number	Row Access Time (max)	Package
μPD41464C-80	80 ns	18-pin plastic DIP
C-10	100 ns	
C-12	120 ns	
μPD41464L-80	80 ns	18-pin PLCC
L-10	100 ns	
L-12	120 ns	

Pin Configurations

18-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



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Pin Identification

Name	Function
A_0 - A_7	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 through A_7
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 through I/O_4

Absolute Maximum Ratings

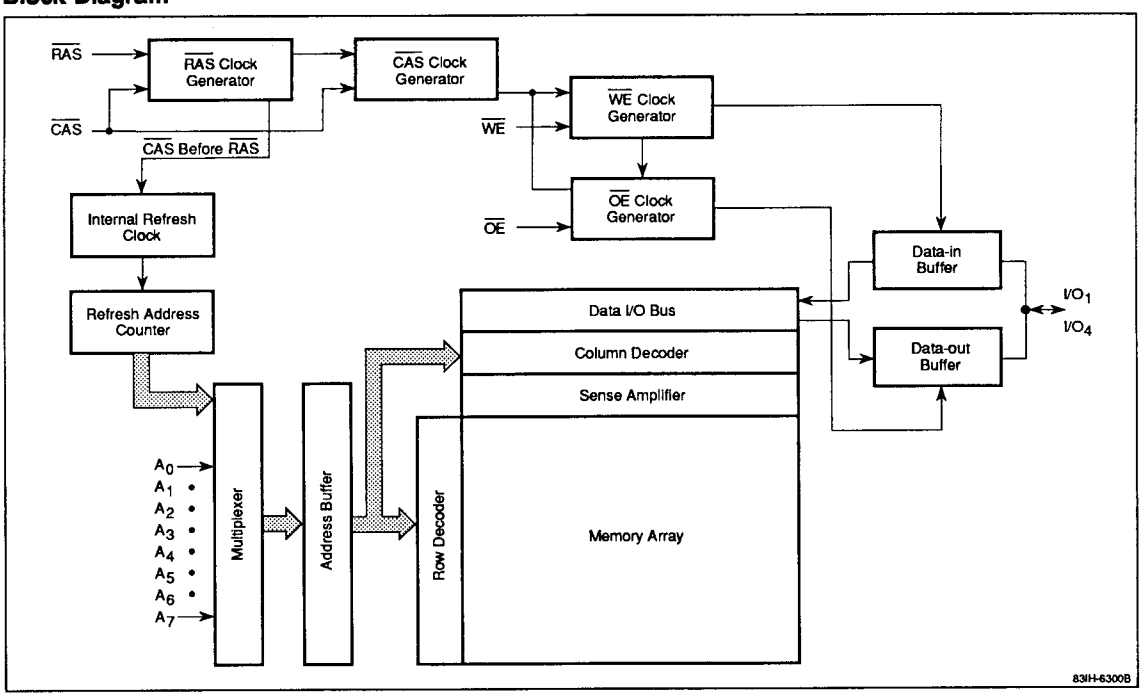
Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1	V
Input voltage, low	V_{IL}	−1		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		5.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	I/O is high-Z; $V_{I/O}$ = 0 V to V_{CC}
Output voltage, low	V_{OL}	0	0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4	V_{CC}	V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD41464-80		μPD41464-10		μPD41464-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		85		80		75	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		70		65		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, page cycle, average	I_{CC4}		60		55		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		70		70		65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	160		200		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	230		270		300		ns	(Note 6)
Page cycle time	t_{PC}	70		100		120		ns	(Note 6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		50		60	ns	(Notes 7, 9)
Ouput buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Notes 2, 3)
$\overline{RAS}$ precharge time	t_{RP}	70		90		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10000	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time for nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time for page cycle	t_{CP}	30		40		50		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		80		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD41464-80 Min	μPD41464-80 Max	μPD41464-10 Min	μPD41464-10 Max	μPD41464-12 Min	μPD41464-12 Max	Unit	Test Conditions
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		25		30		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		90		ns	
Write command pulse width	t_{WP}	20		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		40		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		40		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		25		30		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		90		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65		80		95		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	
Data delay time	t_{OED}	20		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Read or write cycle time for counter test cycle	t_{TRC}	185		220		245		ns	(Note 16)
Read or write cycle time for counter test cycle	t_{TRWC}	245		290		325		ns	(Note 16)
$\overline{CAS}$ setup time for $\overline{CAS}$-before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		25		ns	

Notes:

(1) An initial pause of 100 μs ($\overline{RAS}$ inactive) is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(2) AC measurements assume t_T = 5 ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals.

(4) All voltages are referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns and I_{CC3} = 60 mA.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns.

(7) Load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle, t_{RAC} is specified as $t_{RAC} = t_{CHR} + t_{CP} + t_{CAC} + 2t_T$ and is greater than the maximum specified value shown in this table.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

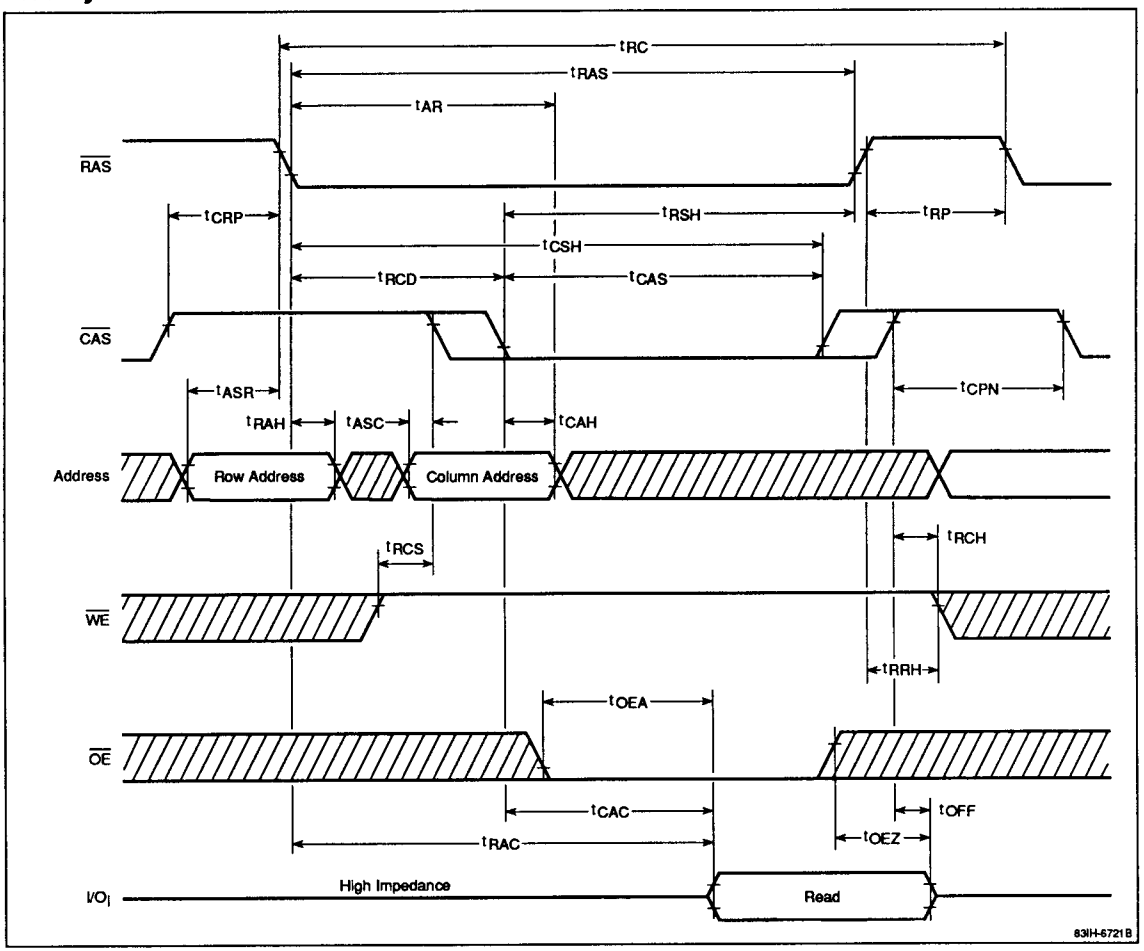
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) t_{TRC} and t_{TRWC} are applicable for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycles.

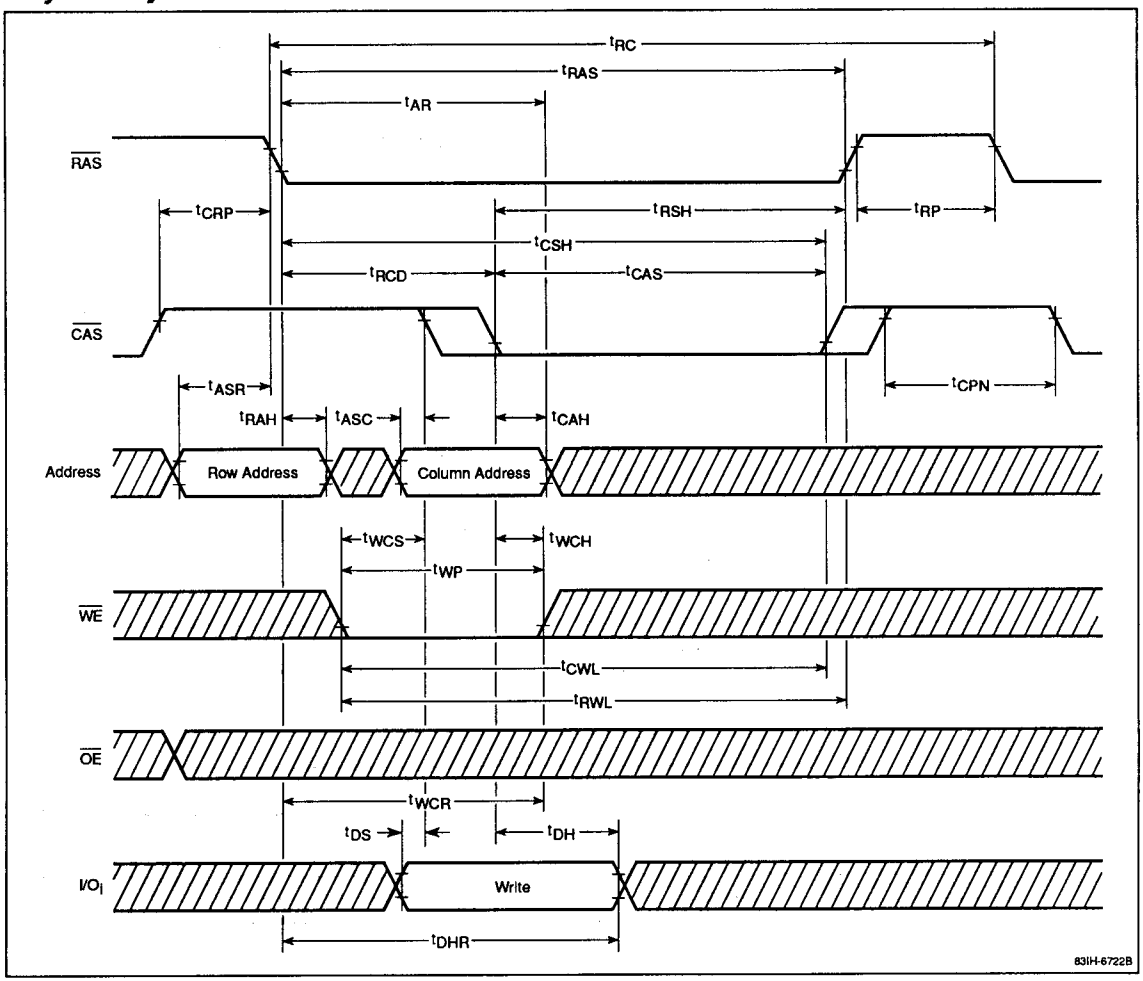
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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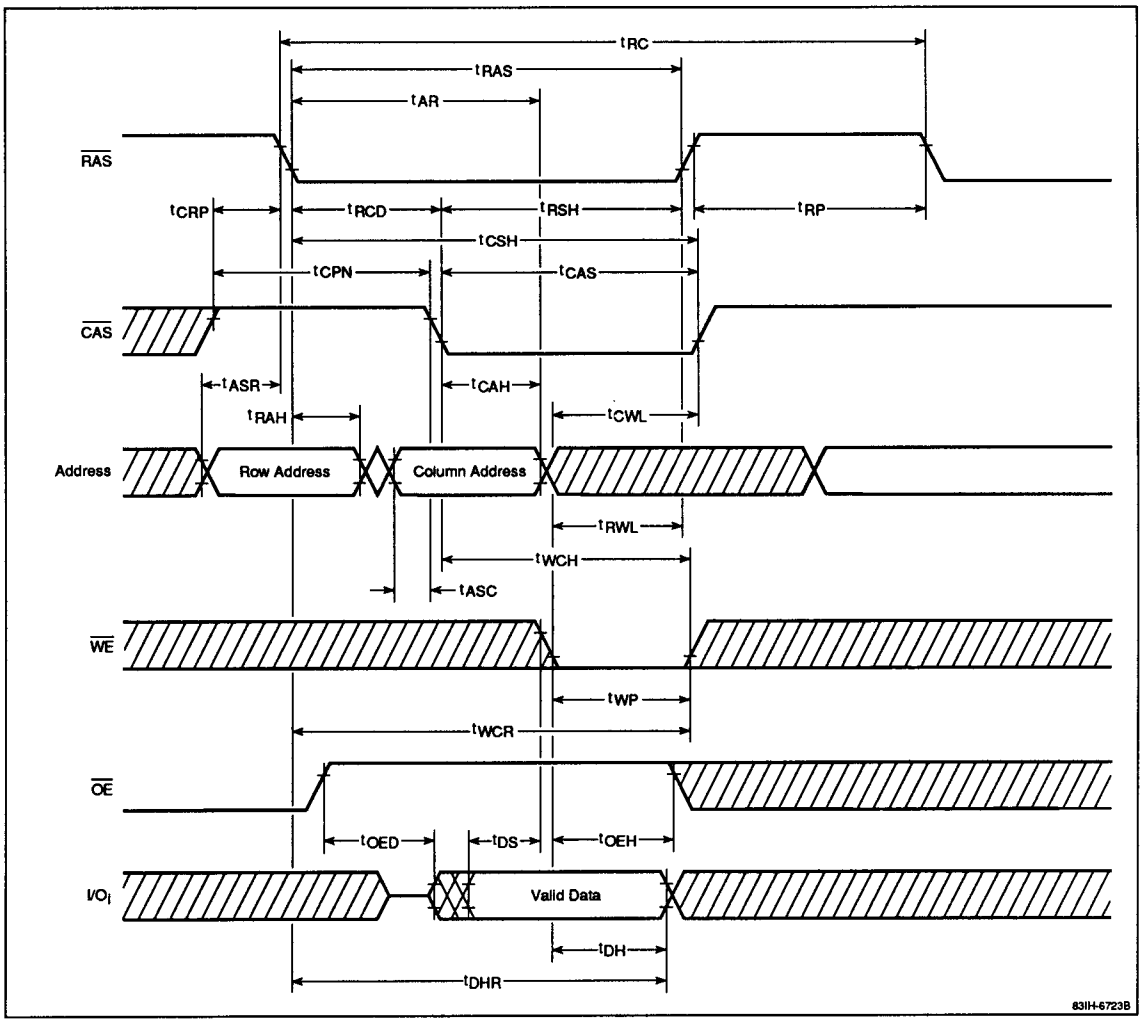
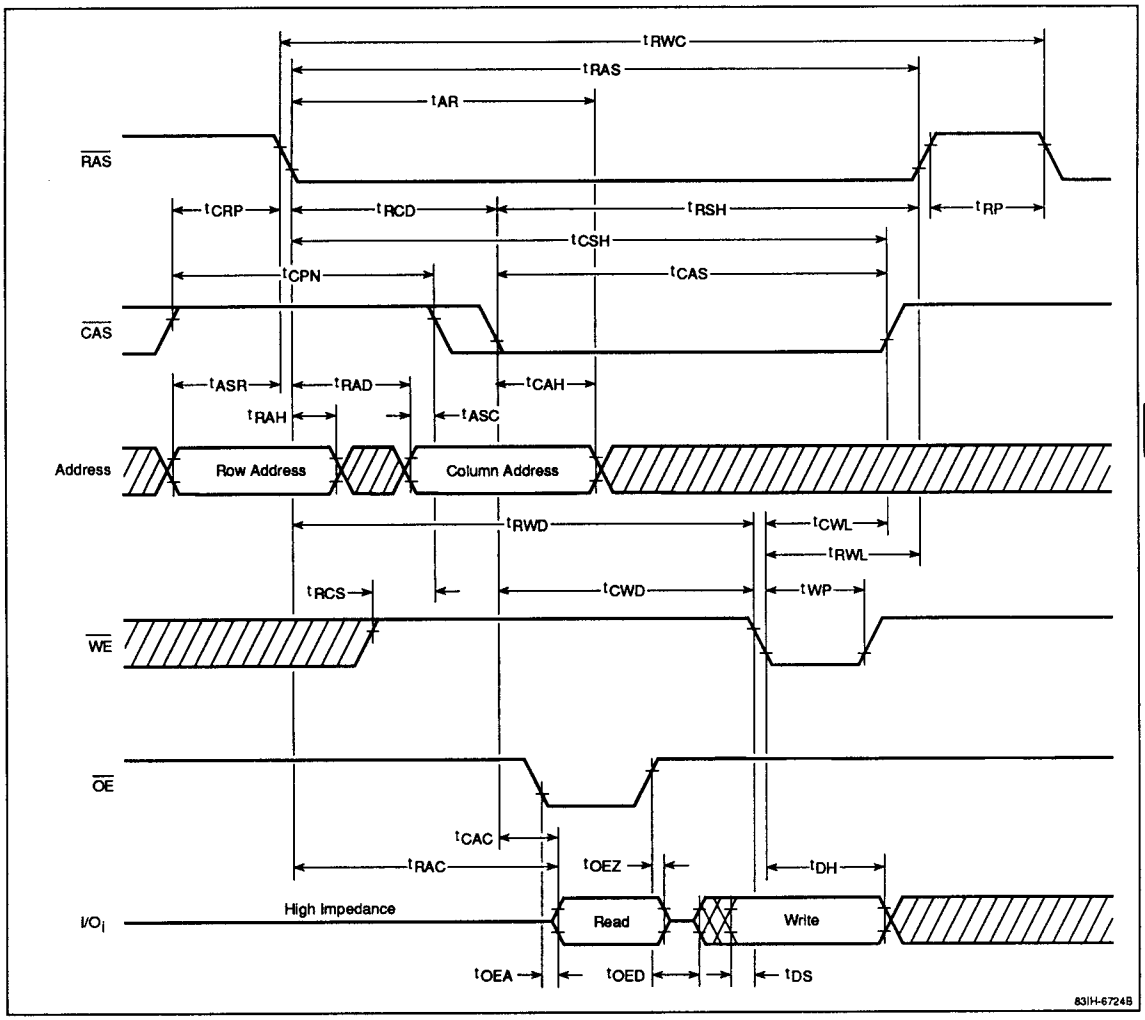
Timing Waveforms (cont)

$\overline{OE}$ -Controlled Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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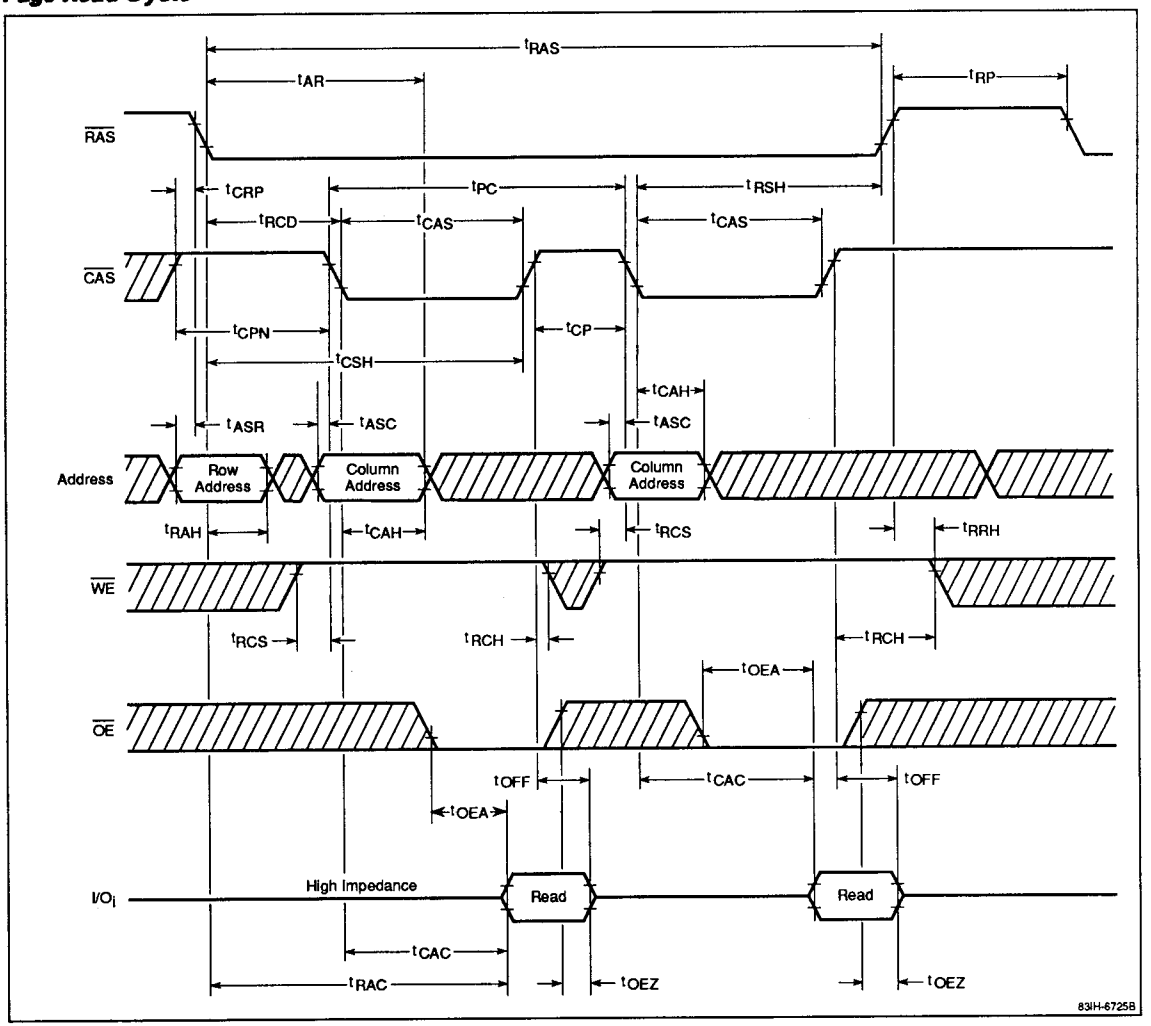
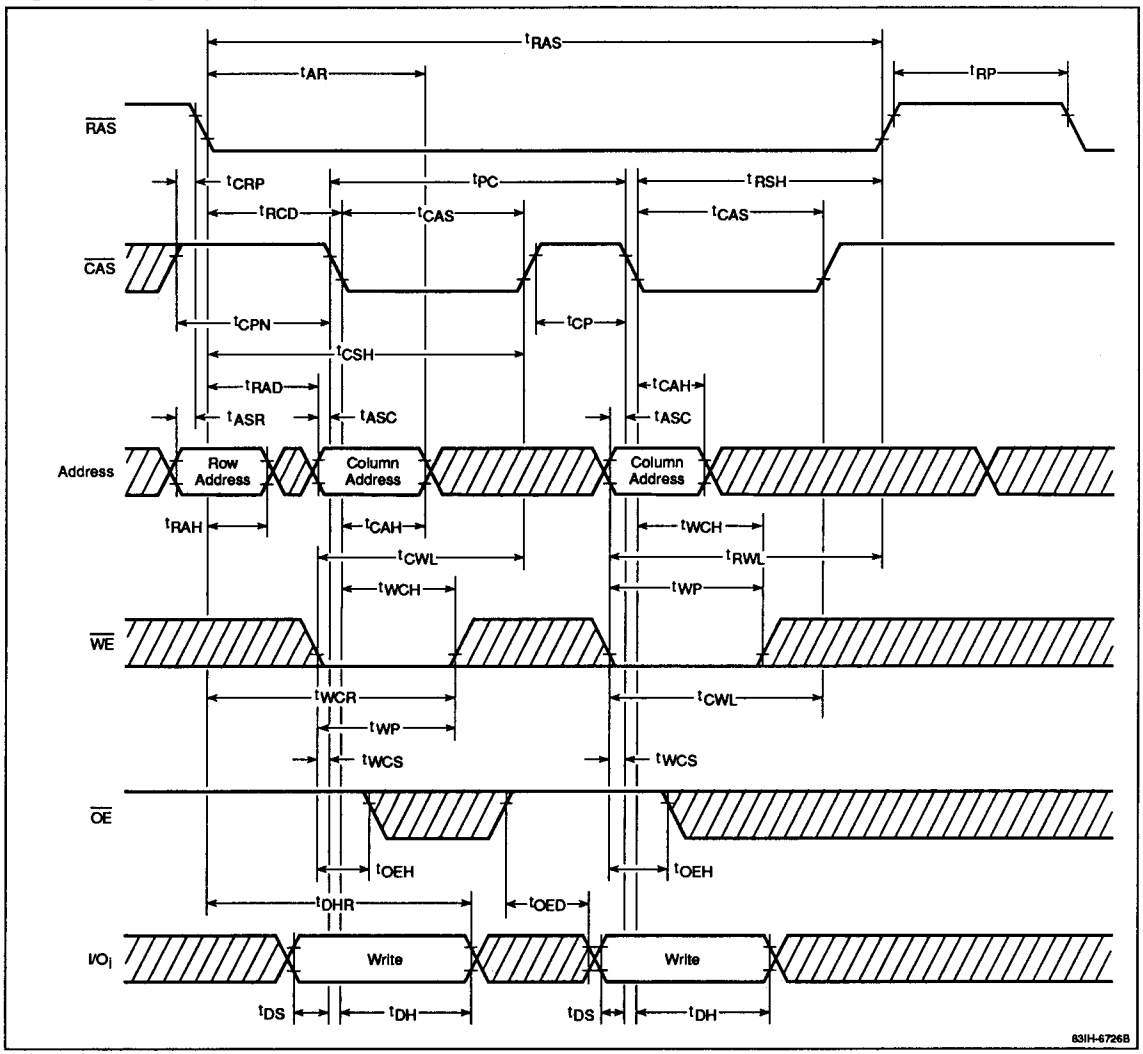
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

Page Write Cycle (Early Write)



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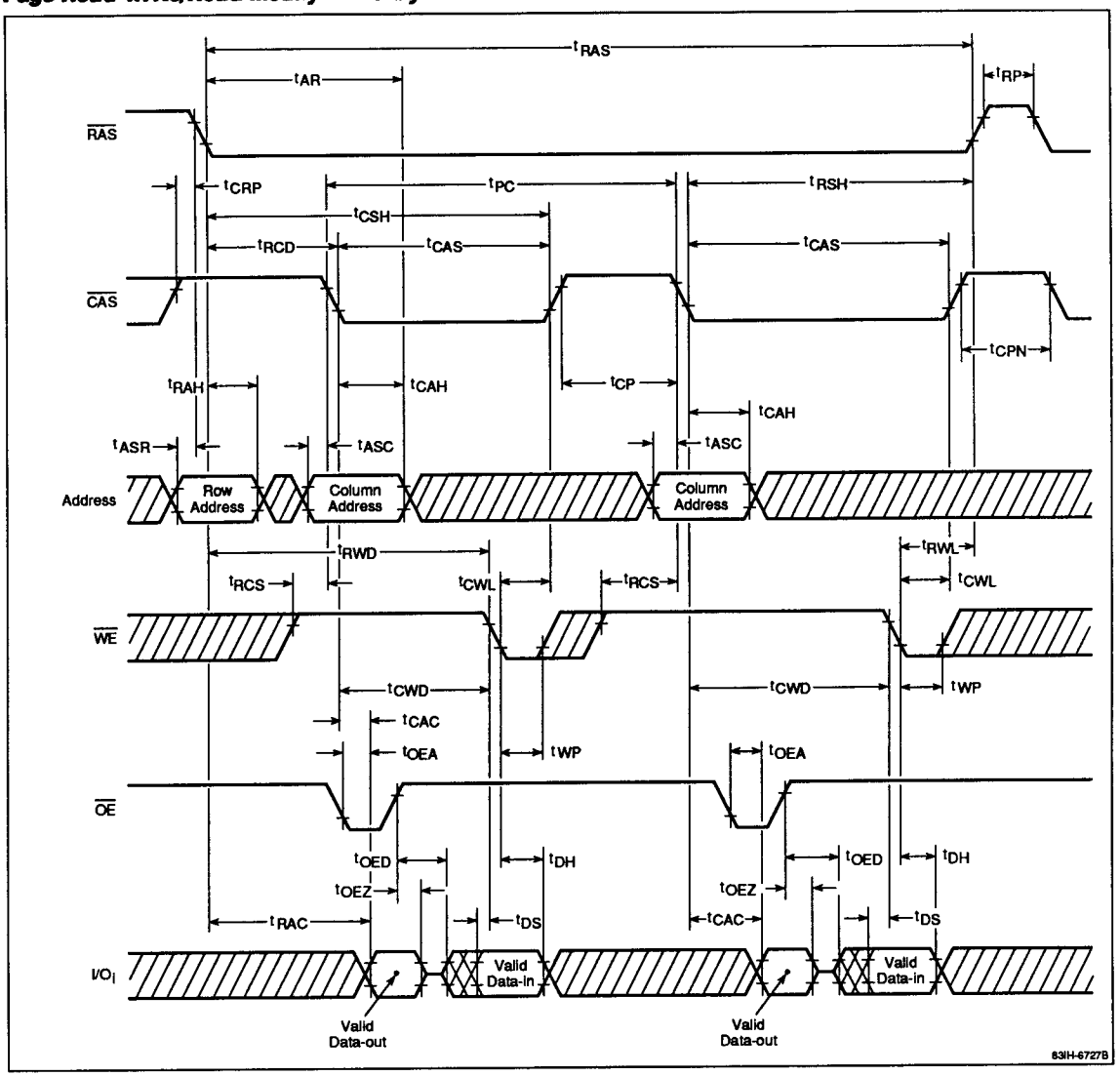
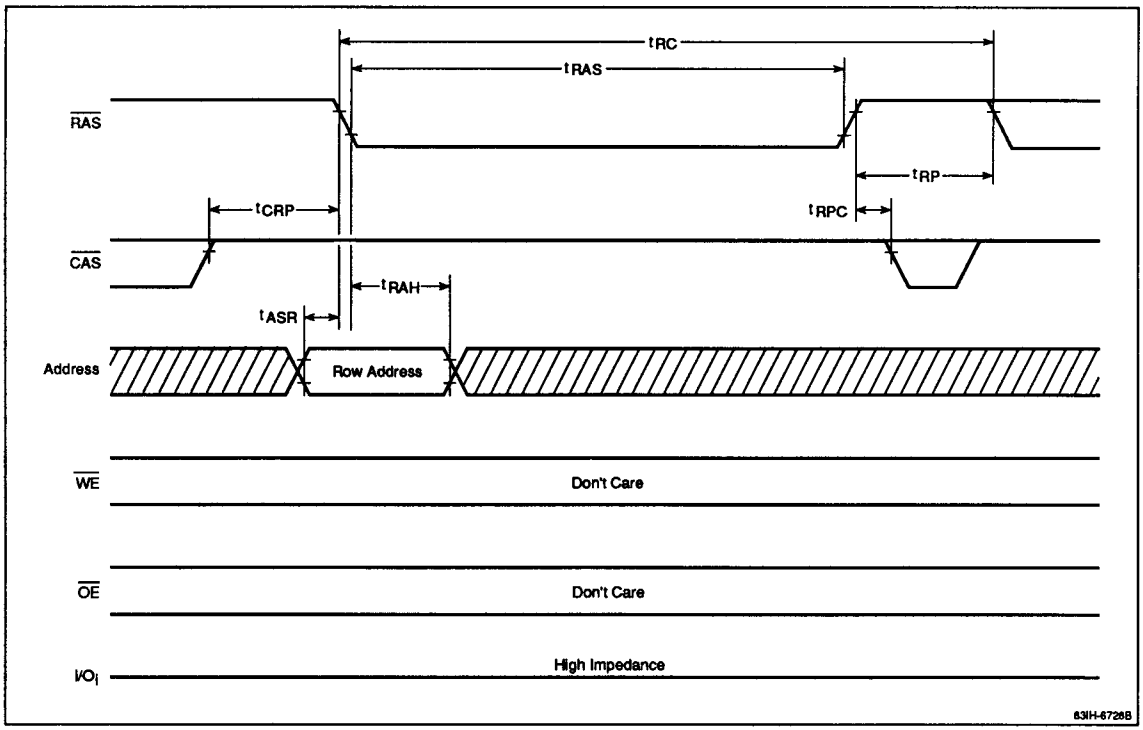
Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle



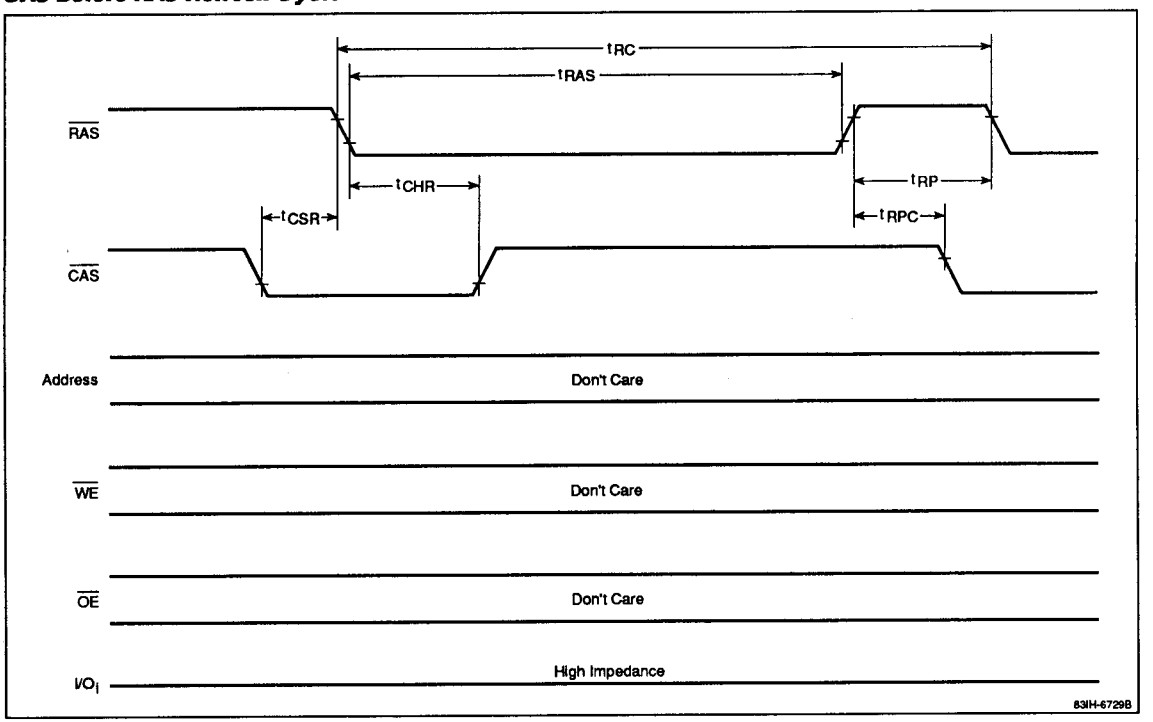
Timing Waveforms (cont)

RAS-Only Refresh Cycle



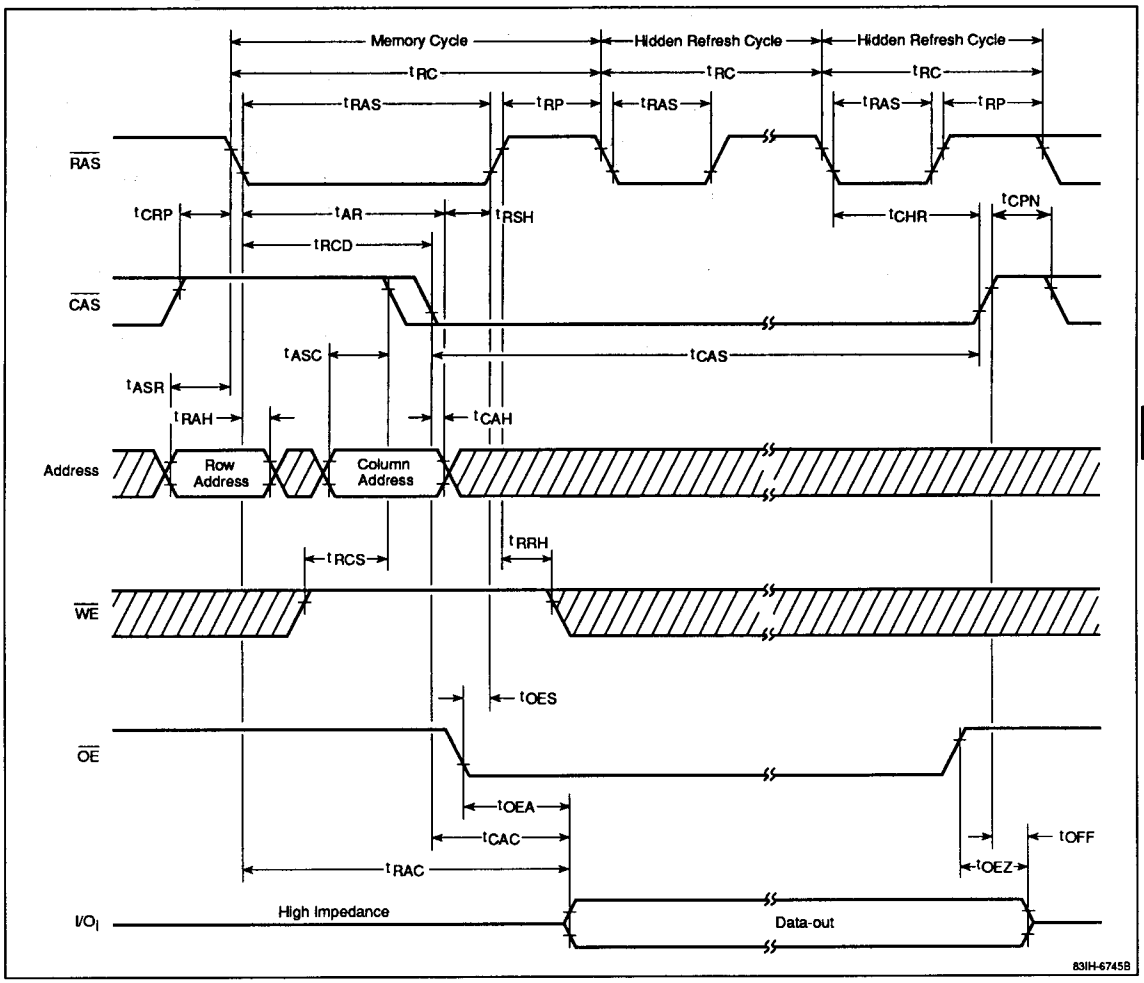
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The μPD41464 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

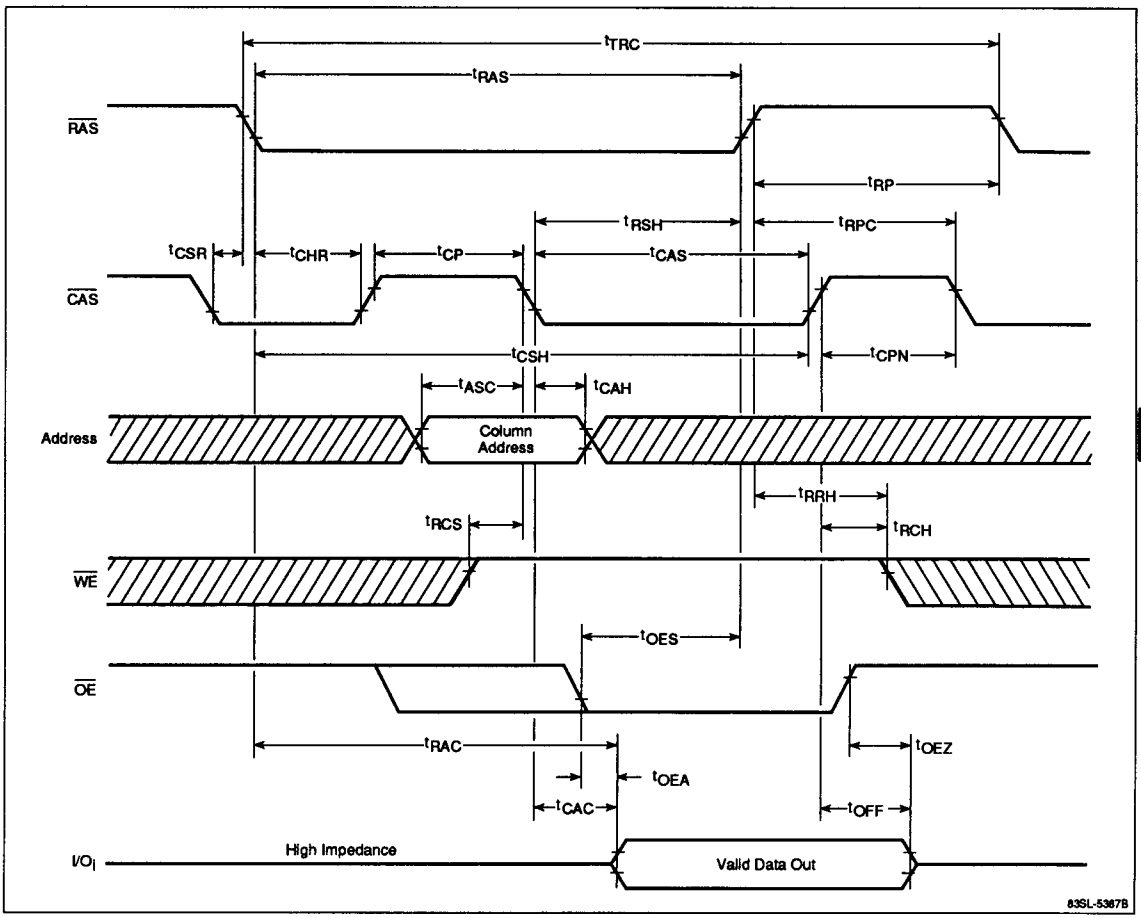
(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



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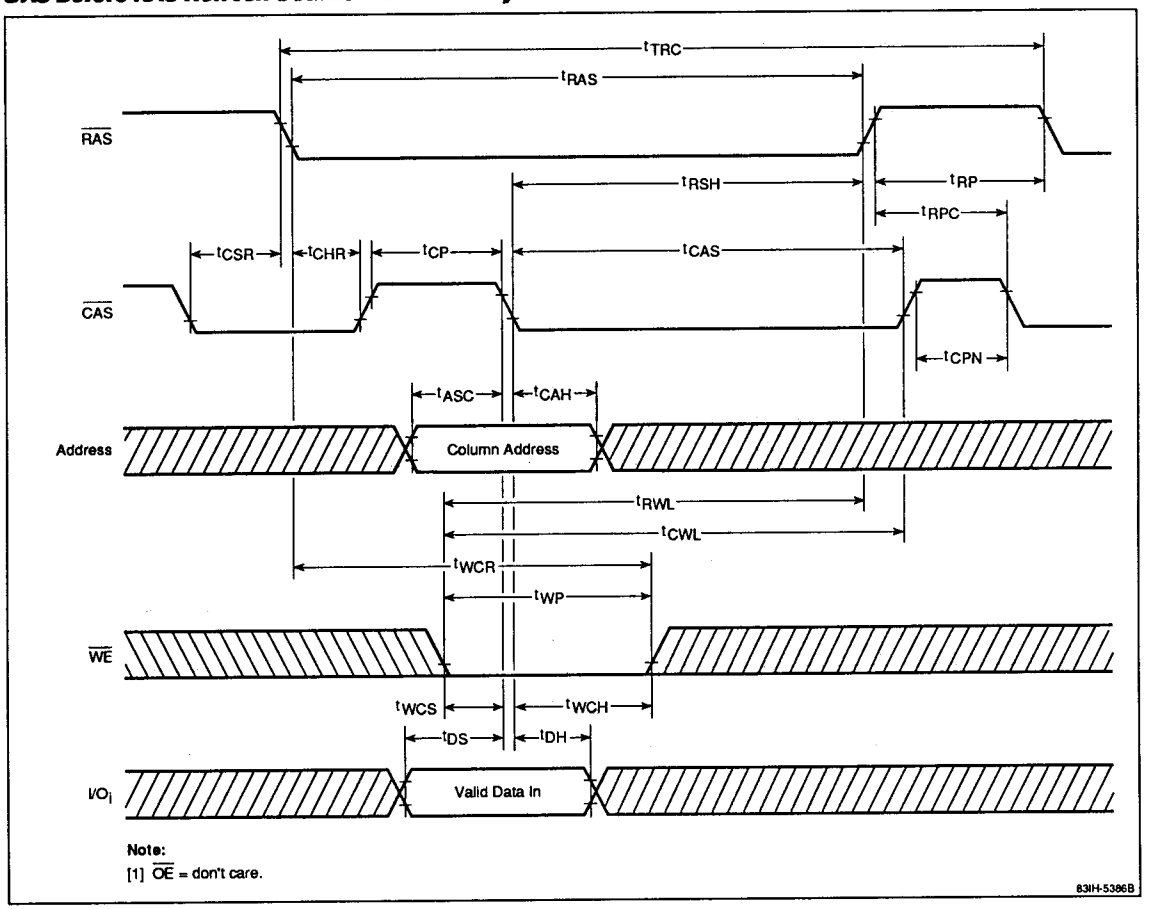
Timing Waveforms (cont)

CAS Before RAS Refresh Counter Test Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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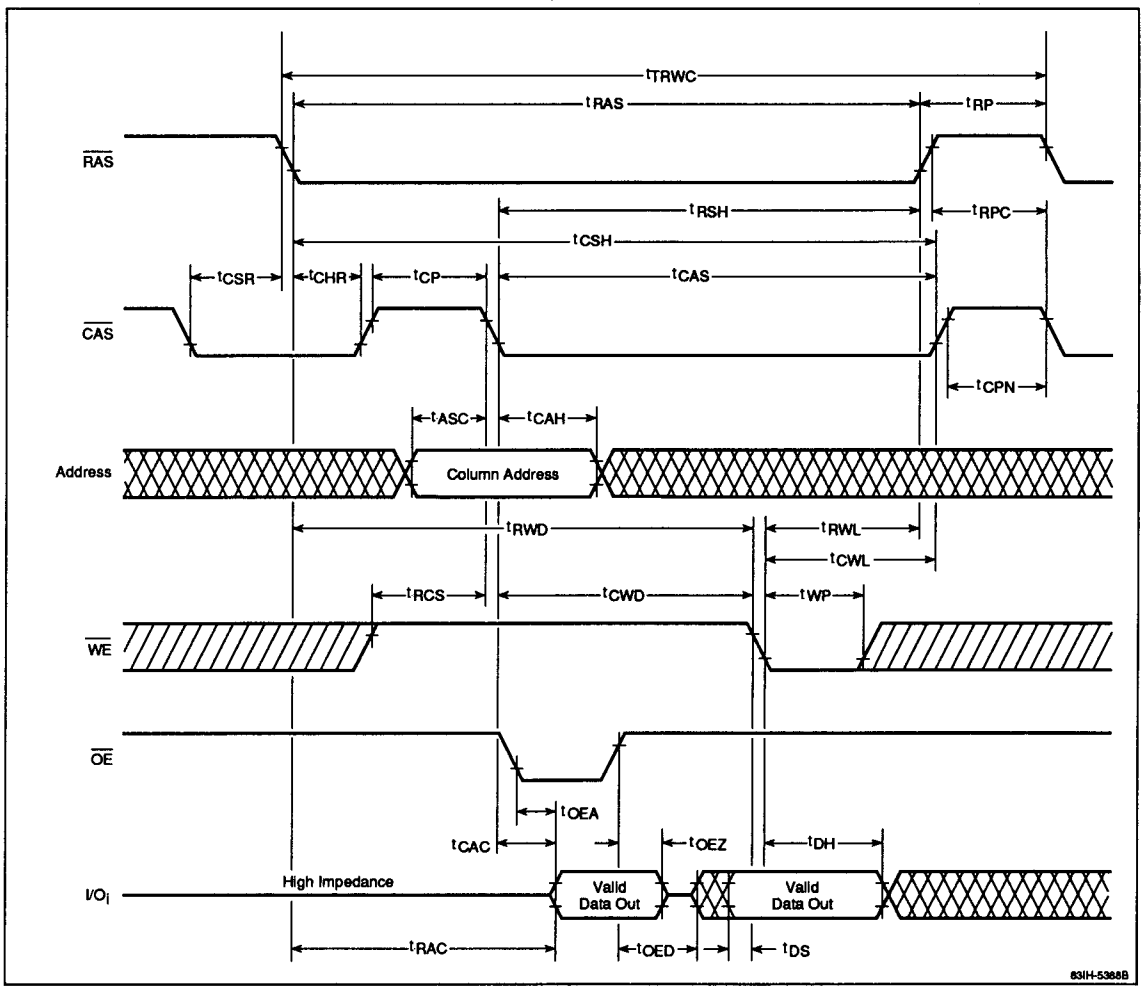
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



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