UMC

T-52-33-51

UM6522/A

Versatile Interface Adapter(VIA)

Features

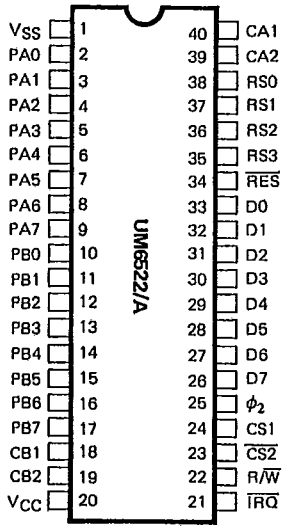
- Two 8-bit bi-directional I/O ports
- Two 16-bit programmable timer/counters
- Serial data port
- Single +5V power supply
- TTL compatible except Port A
- CMOS compatible peripheral Port A lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices
- Latched input and output registers
- 1 MHz and 2 MHz operation

General Description

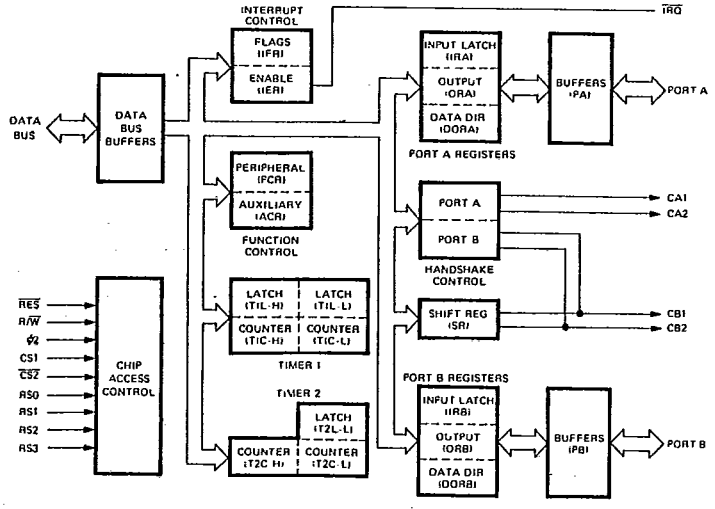
The UM6522/A Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 VOLTS
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

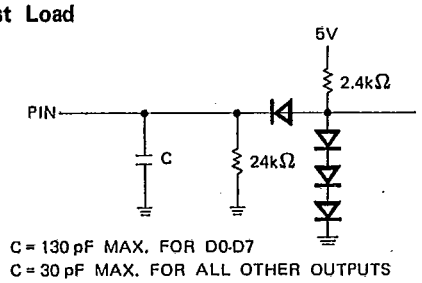
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Electrical Characteristics

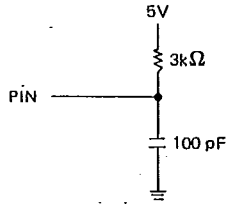
(V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	–0.3	0.4	V
I_{IN}	Input Leakage Current – V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\phi 2$	–	±2.5	μA
I_{TSI}	Off-state Input Current – V_{IN} = 0.4 to 2.4V V_{CC} = Max, D0 to D7	–	±10	μA
I_{IH}	Input High Current – V_{IH} = 2.4V PA0–PA7, CA2, PB0–PB7, CB1, CB2	–100	–	μA
I_{IL}	Input Low Current – V_{IL} = 0.4 Vdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	–	–1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = –100 μAdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	2.4	–	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	–	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0–PB7)	 –100 –1.0	 – –	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	–	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	–	10	μA
C_{IN}	Input Capacitance – T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0–D7, PA0–PA7, CA1, CA2, PB0–PB7) (CB1, CB2) ($\phi 2$ Input)	– – –	7.0 10 20	pF pF pF
C_{OUT}	Output Capacitance – T_A = 25°C, f = 1 MHz	–	10	pF
P_D	Power Dissipation (V_{CC} = 5.25V)	–	700	mW

Test Load



C = 130 pF MAX. FOR D0-D7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



OPEN COLLECTOR
OUTPUT TEST LOAD

Figure 2. Test Load (for all Dynamic Parameters)

Read Timing Characteristics (Figure 3.)

Symbol	Parameter	UM6522		UM6522A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

Note: tr, tf = 10 to 30ns.

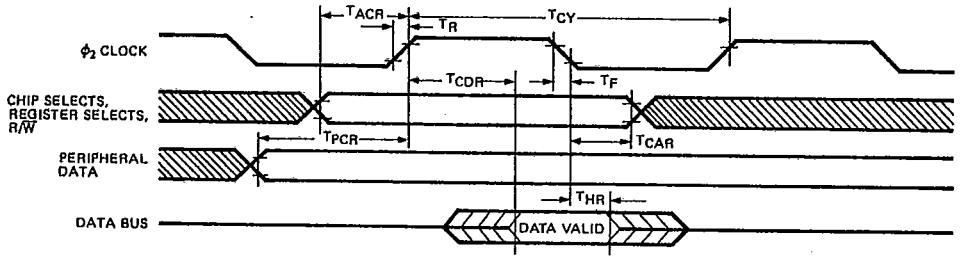


Figure 3. Read Timing Characteristics

Write Timing Characteristics (Figure 4.)

Symbol	Parameter	UM6522		UM6522A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	φ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WGW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

Note: tr, tf = 10 to 30ns.

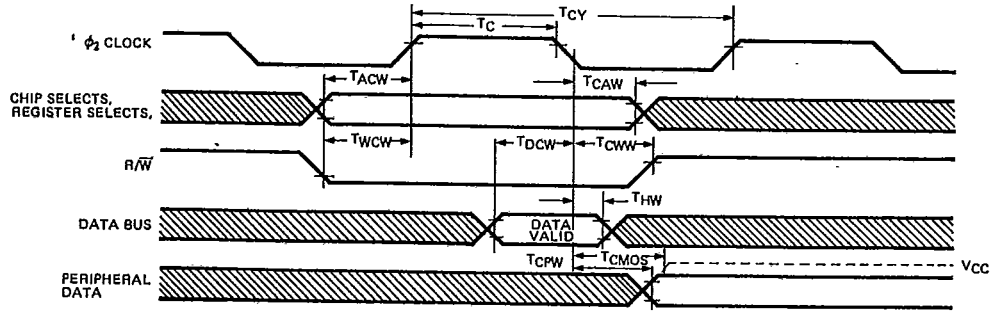


Figure 4. Write Timing Characteristics

Peripheral Interface Characteristics

Symbol	Characteristic	Min.	Max.	Typ.	Units	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	–	1.0		μs	–
T_{CA2}	Delay Time, Clock Negative Transition to CA2, Negative Transition (read handshake or pulse mode)	–	1.0		μs	5a, 5b
T_{RS}	Delay Time, Clock Negative Transition to CA2, Positive Transition (pulse mode)	–	1.0		μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2, Positive Transition (handshake mode)	–	2.0		μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2, Negative Transition (write handshake)	0.05	1.0		μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2, Negative Transition	0.20	1.5		μs	5c, 5d
T_{RS3}	Delay Time, Clock Transition to CA2 or CB2, Positive Transition (pulse mode)	–	1.0		μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2, Positive Transition (handshake mode)	–	2.0		μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1, Active Transition (handshake mode)	400	–		ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1, Active Transition (input latching)	300	–		ns	5e
T_{SR1}	Shift-Out Delay Time – Time from ϕ_2 Falling Edge to CB2, Data Out	–	300		ns	5f
T_{SR2}	Shift-In Setup Time – Time from CB2 Data in to ϕ_2 Rising Edge	300	–		ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}		ns	5g
T_{IPW}	Pulse Width – PB6 Input Pulse	$2 \times T_{CY}$	–			5i
T_{ICW}	Pulse Width – CB1 Input Clock	$2 \times T_{CY}$	–			5h
T_{IPS}	Pulse Spacing – PB6 Input Pulse	$2 \times T_{CY}$	–			5i
T_{ICS}	Pulse Spacing – CB1 Input Pulse	$2 \times T_{CY}$	–			5h
T_{AI}	CA1, CB1 Set-Up Prior to Transition to Arm Latch	$T_C + 50$	–		ns	5h
T_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	–		ns	5e
T_{PWI}	Set-Up Required on CA1, CB1, CA2 or CB2 Prior to Triggering Edge	$T_C + 50$	–		ns	5j
T_{DPR} T_{DPL}	Shift Register Clock – Delay from ϕ_2 to CB1 Rising Edge to CB1 Falling Edge			200 125	ns ns	5k 5k

I/O And Peripherals

Timing Waveforms

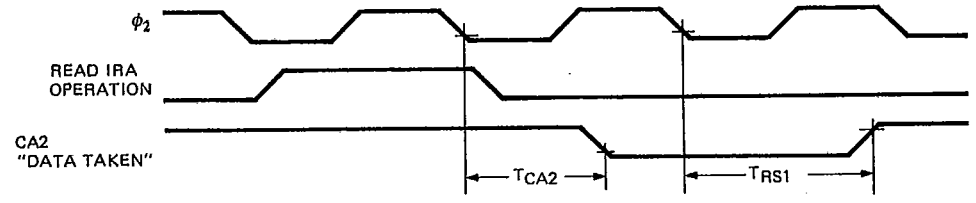


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

Timing Waveforms (Continued)

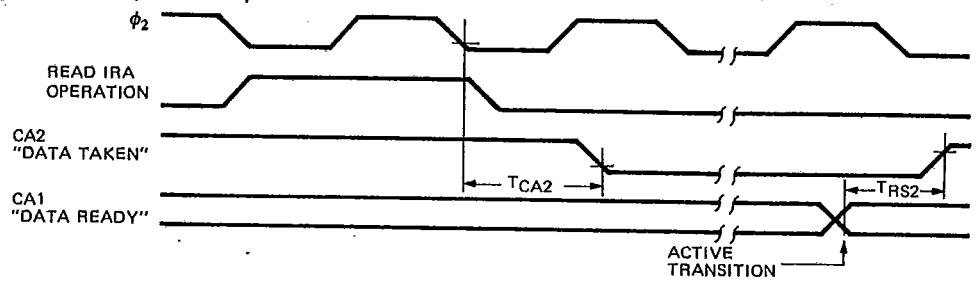


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

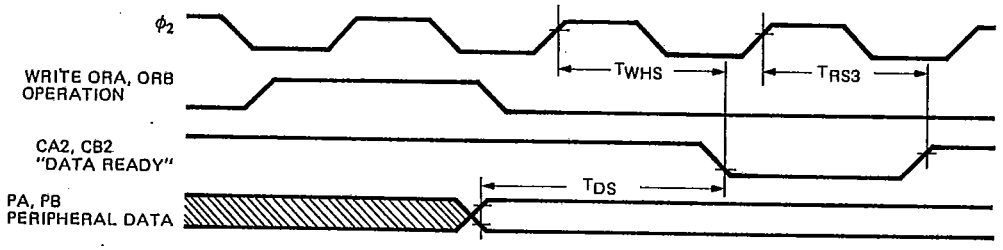


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

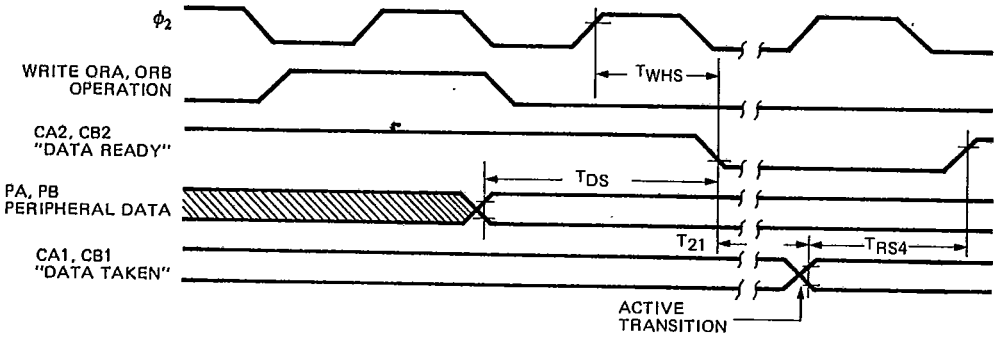


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

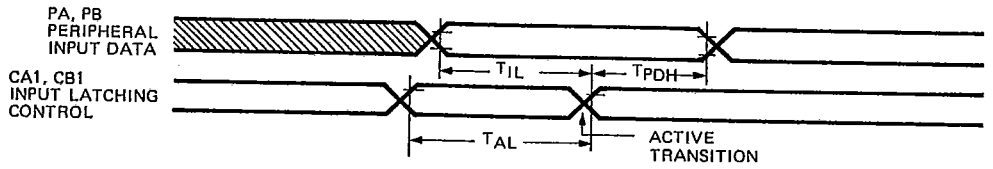


Figure 5e. Peripheral Data Input Latch Timing

Timing Waveforms (Continued)

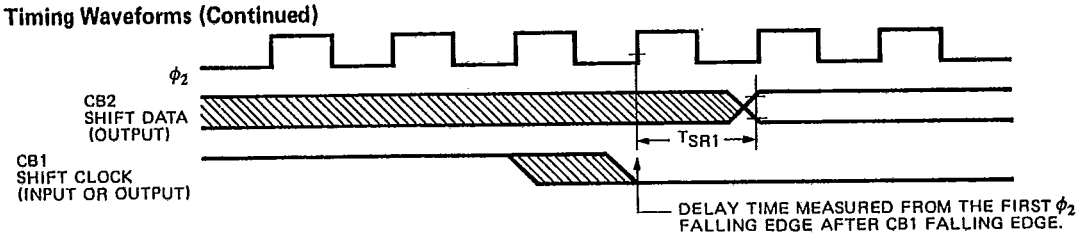


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

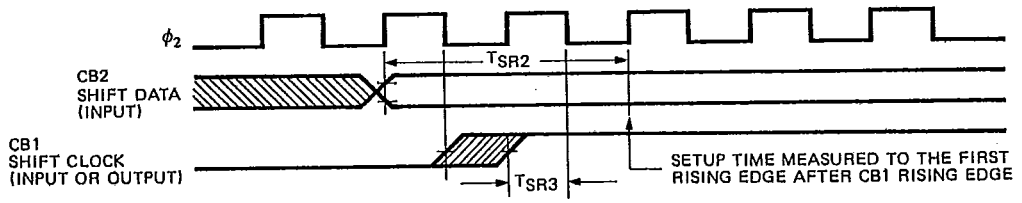


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

Figure 5h. External Shift Clocking

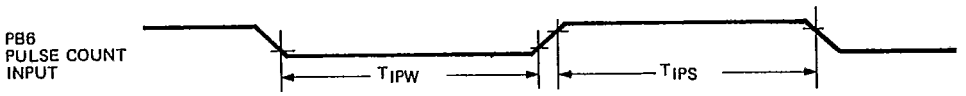


Figure 5i. Pulse Count Input Timing

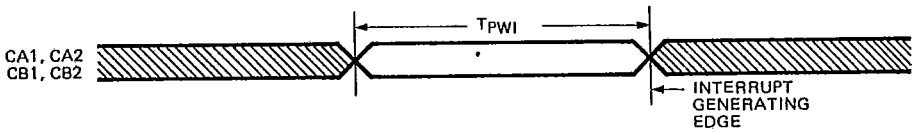


Figure 5j. Setup Time to Trigger Edge

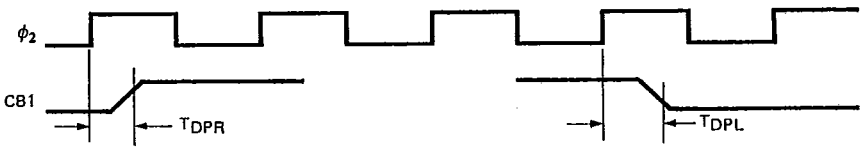


Figure 5k. Shift-in/out with Internal Clock Delay CD2 to CB1 Edge

Pin Description

$\overline{RES}$ (Reset)

The reset input clears all internal registers to logic "0" (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system processor and the UM6522/A.

R/$\overline{W}$ (Read/Write)

The direction of the data transfers between the UM6522/A and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected UM6522/A register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the UM6522/A (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the UM6522/A and the system processor. During read cycles, the contents of the selected UM6522/A register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the UM6522/A is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected UM6522/A register will be accessed when CS1 is high and $\overline{CS2}$ is low.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the UM6522/A, as shown in Figure 6.

$\overline{IRQ}$ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic "1". This output is "open-drain" to allow the interrupt request signal to be wire-ORed with other equivalent signals in the system.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No. "Handshake"	

Figure 6. UM6522/A Internal Register Summary

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high impedance input only; while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

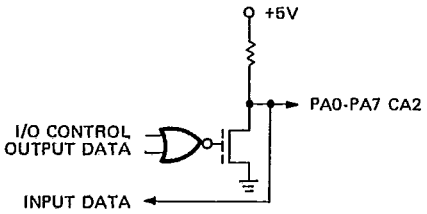


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 andCA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7. CB1 and CB2 cannot drive Darlington transistor circuits.

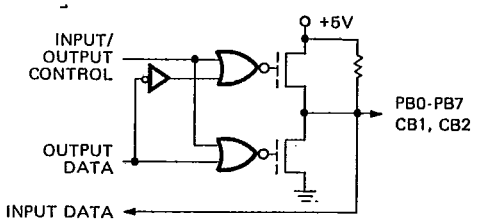


Figure 8. Peripheral B Port Output Circuit

Functional Description

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

When programmed as an output each peripheral pin is also controlled by a corresponding bit in the Output Register (ORA' ORB). A "1" in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled and the selected active transition on CA1 having occurred, IRA will contain the data present on the PA lines at the time of the transition. Once IRA is read, however, it will appear transparent, reflecting the current state of the PA lines until the next "latching" transition.

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10 and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 17.)

Handshake Control of Data Transfer

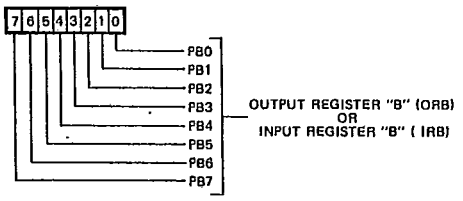
The UM6522/A allows positive control of data transfer between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfer from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the UM6522/A, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" Signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequency.

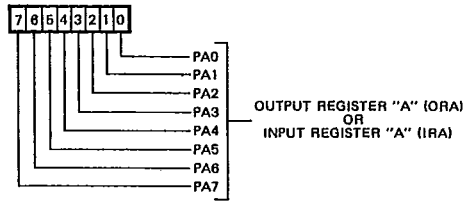
REG 0 – ORB/IRB



Pin Data Direction Selection	Write	Read
DDRB="1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin Level has no affect.
DDRB="0" (INPUT) (Input latching disabled)	MPU writes into ORB but no effect	MPU reads input level on PB Pin.
DDRB="0" (INPUT) (Input Latching enabled)	On Pin Level until DDRB changed	MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB), Input Register B (IRB)

REG 1 – ORA/IRA



Pin Data Direction Selection	Write	Read
DDRA="1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA="1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA="0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA="0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)

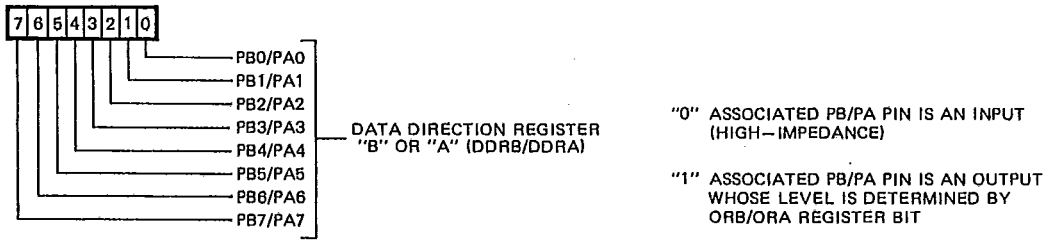


Figure 11. Data Direction Registers (DDRB, DDRA)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the UM6522/A generates the "Data

Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the UM6522/A. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

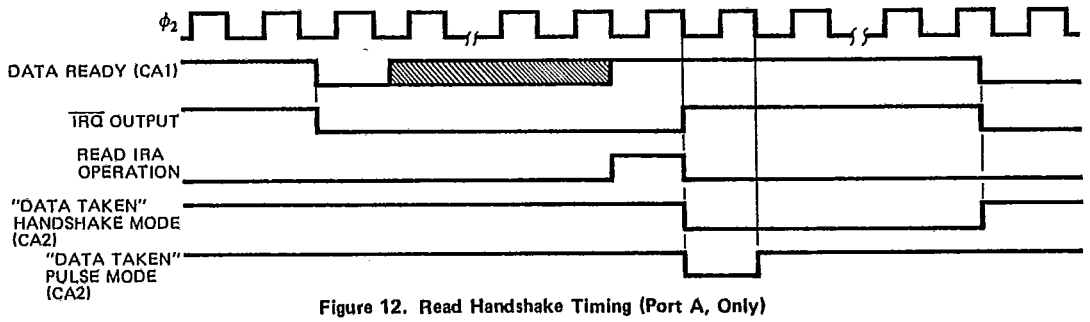


Figure 12. Read Handshake Timing (Port A, Only)

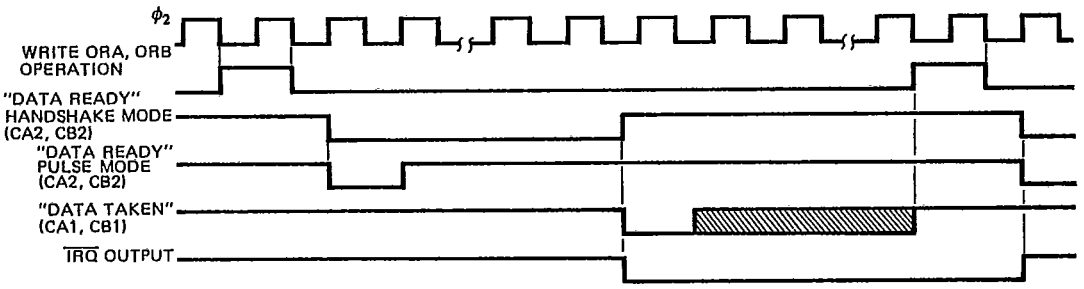
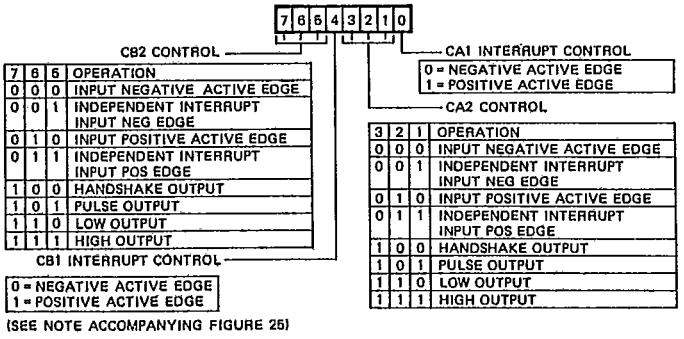


Figure 13. Write Handshake Timing

I/O And Peripherals

REG 12—PERIPHERAL CONTROL REGISTER



7	6	5	OPERATION
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

3	2	1	OPERATION
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

Figure 14. CA1, CA2, CB1, CB2 Control

Timer Operation

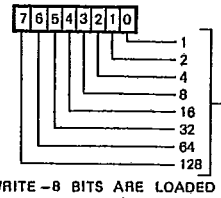
Interval Timer, T1, consists of two 8-Bit latches and a 16-bit decrement at the $\phi 2$ clock rate. Upon reaching "zero", an interrupt flag will be set, and IRQ will go low if the interrupt decrements at the $\phi 2$ clock rate. Upon reaching "zero" an interrupt flag will be set, and IRQ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or (when programmed to) will automatically transfer the contents of the latches into the counter and begin to decrement again. In addition, the timer may be programmed to invert the output signal on a peripheral

pin each time it "times-out." Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

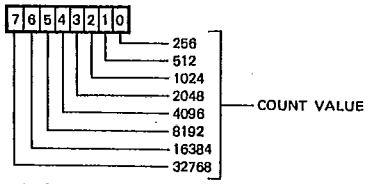
Reg 4 – Timer 1 Low-Order Counter



WRITE – 8 BITS ARE LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW ORDER COUNTER AT THE TIME THE HIGH ORDER COUNTER IS LOADED (REG. 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER ARE TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

Reg 5 – Timer 1 High-Order Counter

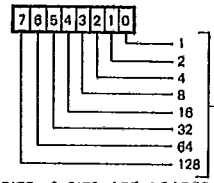


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES ARE TRANSFERRED INTO THE T1 COUNTER, AND INITIATES COUNTDOWN. T1 INTERRUPT FLAG IS ALSO RESET.

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

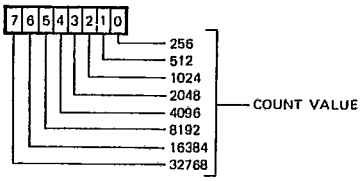
Reg 6 – Timer 1 Low-Order Latches



WRITE – 8 BITS ARE LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT FOLLOWING A WRITE INTO REG 4.

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

Reg 7 – Timer 1 High-Order Latches

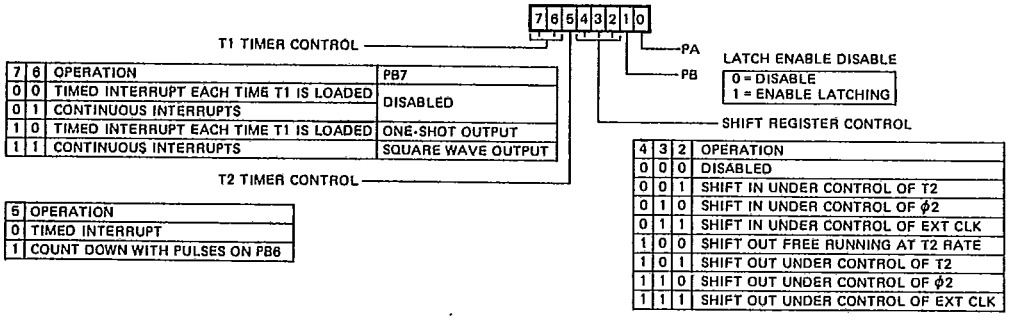


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION, NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES ARE TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

Reg 11 – Auxiliary Control Register



7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE-SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 17. Auxiliary Control Register

Note: The processor does not write directly to the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes to the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

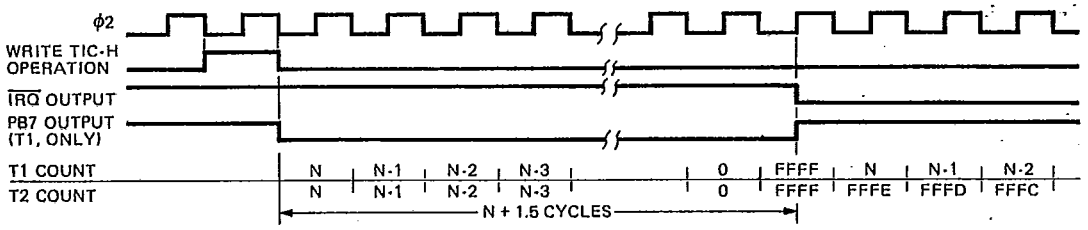


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each Timer load operation. In addition, Timer 1 can be programmed to produce a single negative pulse on PB7.

To generate a single interrupt ACR bits 6 and 7 must be "0", then either TIL-L or TIC-L must be written with the low-order count value. (A write to TIC-L is effectively a Write to TIL-L). Next, the high-order count value is written to TIC-H, (the value is simultaneously written into TIL-H), and TIL-L is transferred to TIC-L. Countdown begins on φ2 following the write TIC-H and decrements at the φ2 rate. T1 interrupt occurs when the counters reach "0". Generation of a negative pulse on PB7 is done in the same manner, except ACR bit 7 must be a one. PB7 will go low after a Write TIC-H and go high again when the counters reach "0".

The T1 interrupt flag is reset by either writing TIC-H (starting a new count) or by reading TIC-L.

Timing for the one-shot mode is illustrated in Figure 18.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. The interrupt flag can be cleared by reading TIC-L, by writing directly into the flag as will be described later, or if a new count value is desired by a write to TIC-H.

All interval timers in the UM6522/A are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.

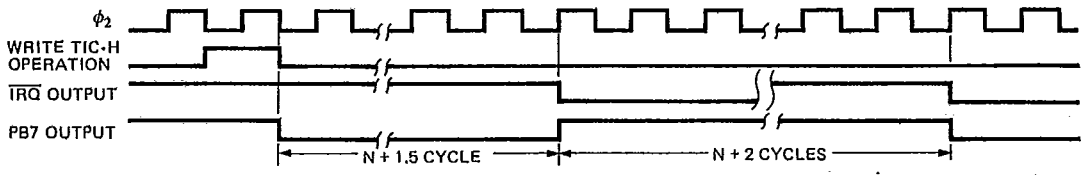


Figure 19. Timer 1 Free-Run Mode Timing

Note: A precaution to take when using PB7 as the timer output concerns the data direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be "1" for PB7 to function as the timer output. If either is a "0", then PB7 functions as a normal output pin, controlled by ORB bit 7.

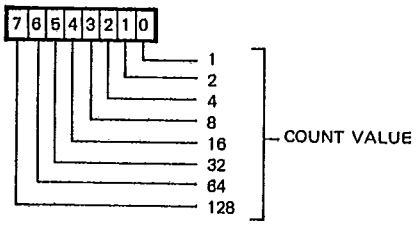
Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at the $\phi 2$ rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, (reading 0) the counters "roll-over" to all 1's ($FFFF_{16}$) and continue decrementing, allowing the user to read them and determine how long T2 interrupt has been set. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

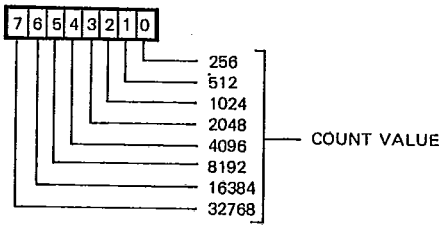
Reg 8 — Timer 2 Low-Order Counter



WRITE — 8 BITS LOADED INTO T2 LOW-ORDER LATCHES.

READ — 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

Reg 9 — Timer 2 High-Order Counter



WRITE — 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER, IN ADDITION, T2 INTERRUPT FLAG IS RESET.

READ — 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time, the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to be set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of $\phi 2$.

Shift Register Operation

The Shift Register (SR) performs serial data transfer into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the UM6522/A involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic "1" by an interrupting condition, and the corresponding interrupt enable bit is set to a "1", the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be wire-ORed to other devices in the system to interrupt the processor.

In the UM6522/A, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic "1" when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

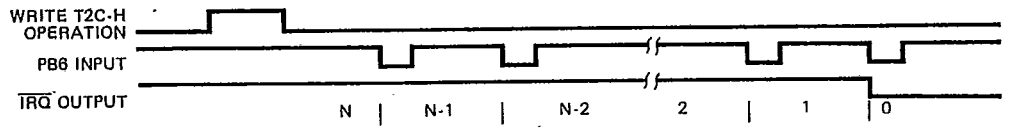
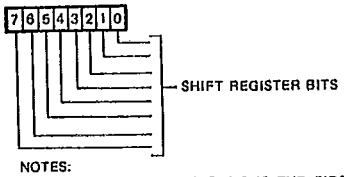


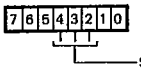
Figure 21. Timer 2 Pulse Counting Mode

Reg 10 — H Reg 10 — Shift Register



NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK BIT 0 AND SHIFTED TOWARDS BIT 7.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

Reg 11 — Auxiliary Control Register



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

I/O And Peripherals

SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operating is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic "0").

Shift In Under Control of T2 (001)

In the 001 mode the shifting rate is controlled by the low order 8 bits of "T2". Shift pulses are generated on the CB1 Pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.

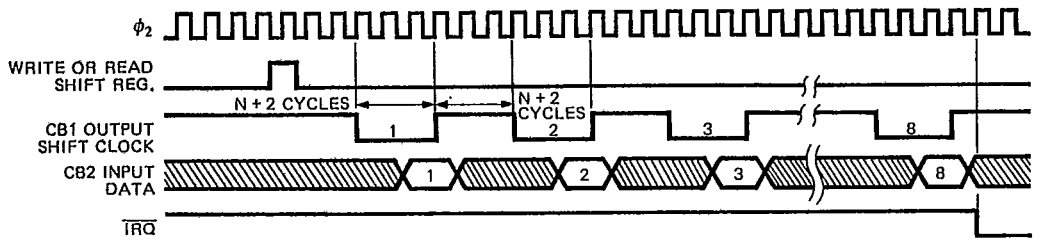


Figure 23-1 Shift Register Input Modes

Shift in Under Control of $\phi 2$ (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each $\phi 2$ clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

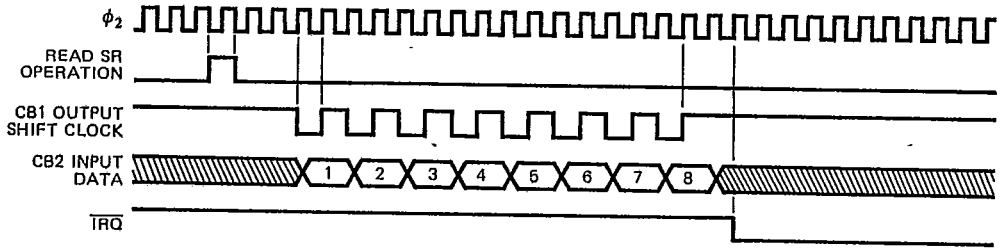


Figure 23-2 Shift Register Input Modes

Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle after CB1 goes high.

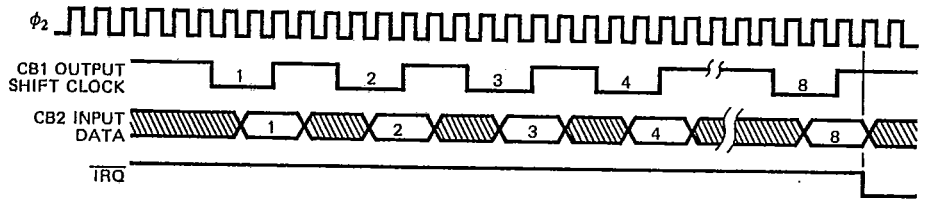


Figure 23-3 Shift Register Input Modes

Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shift rate is set by T2. However, in mode 100 the SR Counter does not stop the shift operation. Since Shift Register bit 7 (SR7) is circulated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CR2 repeatedly. In this mode the shift register counter is disabled, and IRQ is never set.

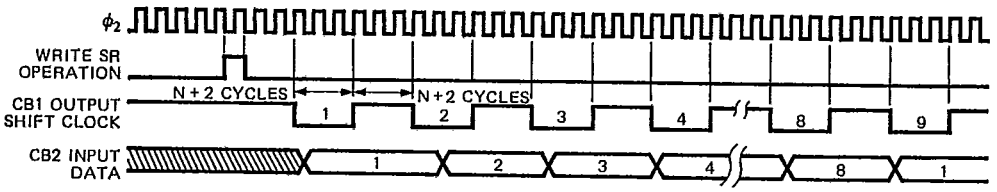


Figure 24-1 Shift Register Output Modes

Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

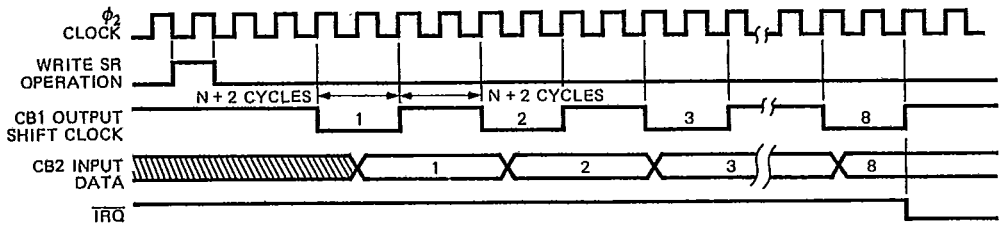


Figure 24-2 Shift Register Output Modes

Shift Out Under Control of $\phi 2$ (110)

In mode 110, the shift rate is controlled by the $\phi 2$ system clock.

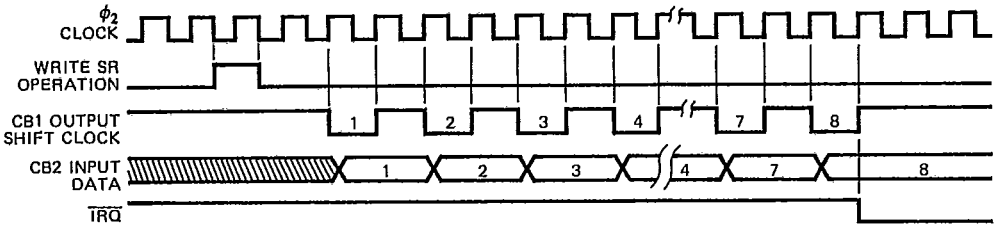


Figure 24-3 Shift Register Output Modes

Shift Out Under Control of External CB1 Clock (111)

In mode 111, shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

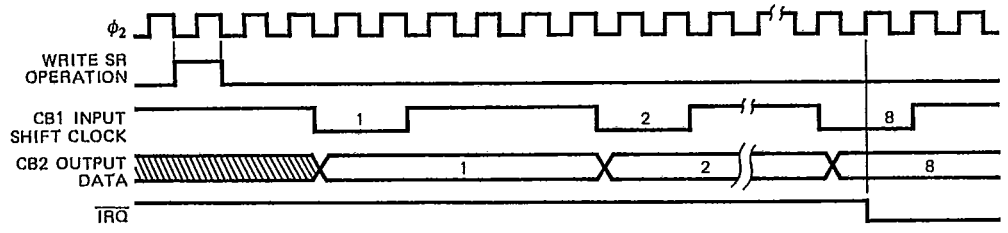


Figure 24-4 Shift Register Output Modes

I/O And Peripherals

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

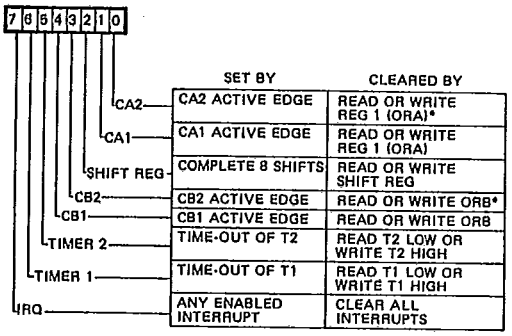
The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic "1" into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a "0", each "1" in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each "zero" in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic "1". In this case, each "1" in bits 6 through 0 will set the corresponding bit. For each "zero", the corresponding bit will be unaffected. The individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a logic "1".

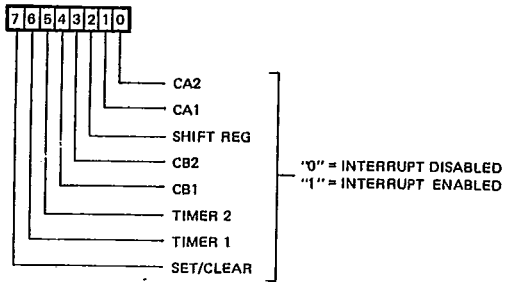
Reg 13 — Interrupt Flag Register



* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

Figure 25. Interrupt Flag Register (IFR)

Reg 14 — Interrupt Enable Register



Notes:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0-6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0-6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

Figure 26. Interrupt Enable Register (IER)

Ordering Information

Part Number	Frequency	Package
UM6522	1 MHz	40L DIP
UM6522A	2 MHz	40L DIP