UMC

UM8326/B

Floppy Disk Data Separator (FDDS)

Features

- Performs complete data separation for floppy disk drives
- Separates FM or MFM-encoded data from any magnetic media
- Eliminates several SSI and MSI devices normally used for data separation
- No critical adjustments required
- Compatible with standard microsystems' FDC 1791, FDC 1793 and other floppy disk controllers
- Small 8-pin dual-in-line package
- +5 Volt only power supply
- TTL-compatible inputs and outputs

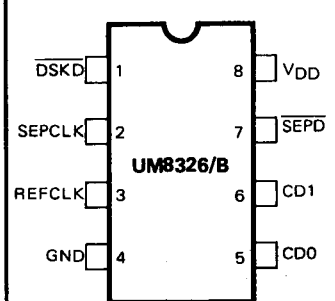
General Description

The Floppy Disk Data Separator provides a low-cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate clock and data inputs for a Floppy Disk Controller.

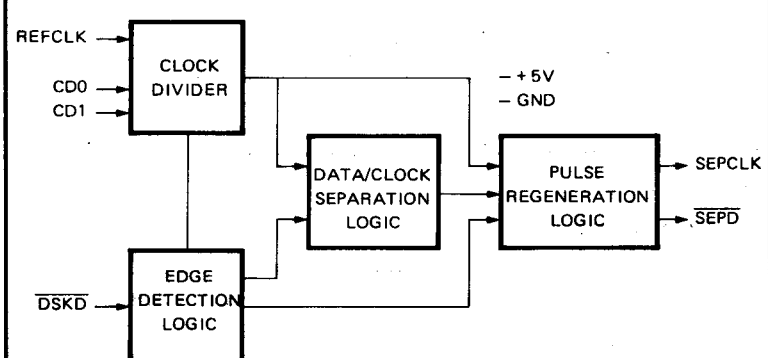
The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and re-clocking circuitry. Supplied in an 8-pin dual-in-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL-compatible on all inputs and outputs.

The UM8326 is available in two versions: The UM8326, which is intended for 5¼" disks, and the UM8326B for both 5¼" and 8" disks.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to + 70°C
Storage Temperature Range . . . . . −55°C to + 150°C
Positive Voltage on any Pin, with respect to ground
. . . . . + 8.0V
Negative Voltage on any Pin, with respect to ground
. . . . . − 0.3V

Note:
When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

*Comments

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{DD} = +5V ± 5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units	Conditions
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level V_{OH}	2.4			V	I_{OH} = −100μA
INPUT CURRENT					
Leakage I_{IL}			10	μA	$0 \leqslant V_{IN} \leqslant V_{DD}$
INPUT CAPACITANCE					
All Inputs			10	pF	
POWER SUPPLY CURRENT					
I_{DD}			60	mA	

A.C. CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	UM8326
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	UM8326B
t_{CKH}	REFCLK High	50		2500	ns	
t_{CKL}	REFCLK Low	50		2500	ns	
t_{SDON}	REFCLK to SEPD "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to SEPD "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	35			ns	
t_{DLL}	DSKD Active Low	0.1		100	μs	
t_{DLH}	DSKD Active High	0.2		100	μs	

Pin Description

Pin No.	Name	Symbol	Function
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5, 6	Clock Divisor	CD0 CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	$\overline{\text{SEPD}}$ is the data output of the FDDS
8	Power Supply	V_{DD}	+5 volt power supply

Operational Description

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long-term timing correctors assure accurate clock separation.

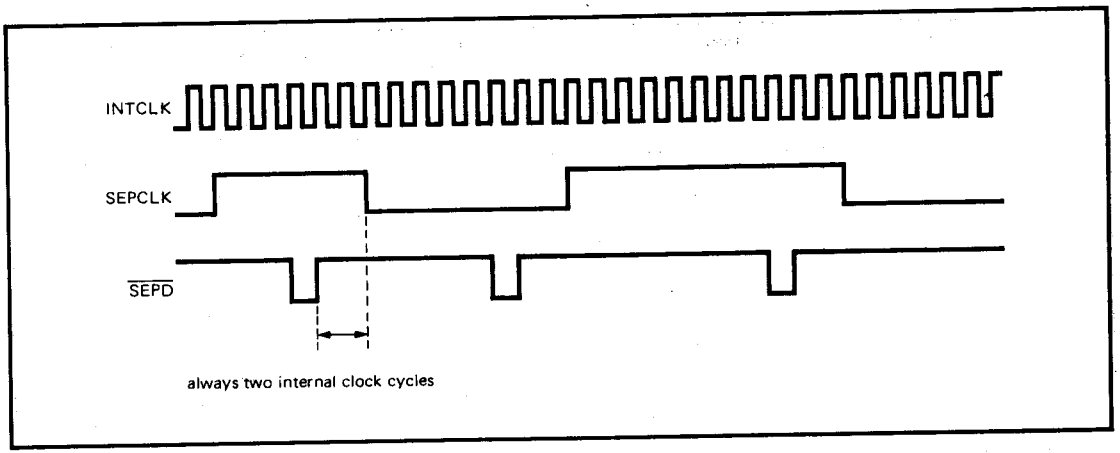
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

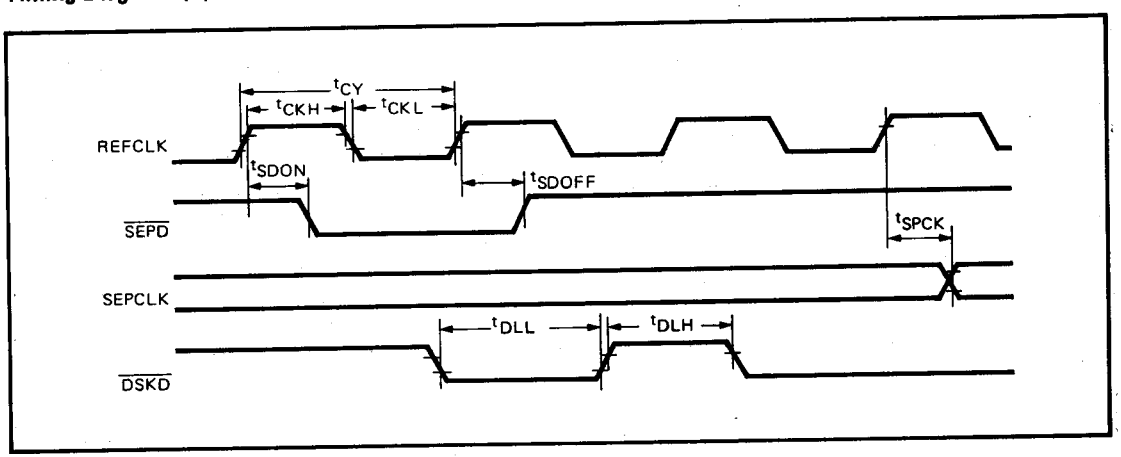
Table 1. Clock Divider Selection Table

Drive (8" or 5¼")	Density (DD or SD)	REFCLK MHz	CD1	CD0	Remarks
8	DD	8	0	0	All selectable
8	SD	8	0	1	
8	SD	4	0	0	
5¼	DD	8	0	1	
5¼	DD	4	0	0	
5¼	SD	8	1	0	
5¼	SD	4	0	1	
5¼	SD	2	0	0	

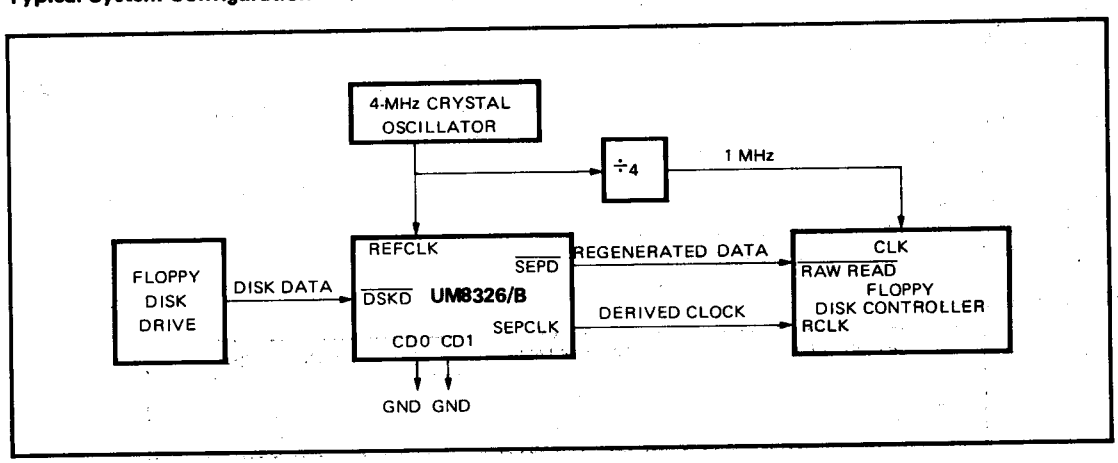
Timing Diagram (1)



Timing Diagram (2)



Typical System Configuration (5¼" Drive, Double Density)



Comparison of Data Separators (UM9228-1, UM8329, UM8326)

PINOUT COMPARISON

Function	UM9228-1	UM8329	UM8326	Remarks
Power Supply:				
V_{CC}	Pin 3 V_{CC}	Pin 20 V_{CC}	Pin 8 V_{DD}	
V_{SS}	13 V_{SS}	10 Ground	4 GND	
Precompensation:				
EARLY	9 EARLY	13 EARLY	-------	See B
LATE	8 LATE	14 LATE	-------	
Amount Control	-------	17 P0	-------	
	-------	18 P1	-------	
	-------	19 P2	-------	
Read Data:				
From FDD	1 RD	1 DSKD	1 DSKD	
To FDC	5 SD	6 SPED	7 SPED	
Data Row	7 DW	5 SEPCLK	2 SEPCLK	
Write Data:				
From FDC	10 WD	12 WDIN	-------	Sec C
To FDD	12 WDOUT	7 WDOUT	-------	
Write Enable	11 WEN	-------	-------	
Write Clock	17 WCLK	9 CLKOUT	-------	
179X/765MODE	-------	2 FDCSEL	5 CD0	See D
Density	-------	3 MINI	6 CD1	
	-------	4 DENS	-------	
MASTER CLK to FDC	18 FCLK	8 HLT/CLK	-------	
External Clock I/P	19 CLKIN	11 XTAL/CLKIN	3 REFCLK	
TEST	-------	16 TEST	-------	
179X/MODE ESP	-------	15 HLD	-------	
DMA	16 DRO	-------	-------	See E
	15 BACK	-------	-------	
	14 DROO/P	-------	-------	
VFO	2 PROR	-------	-------	See F
	4 PFDV	-------	-------	
	6 VCOIN	-------	-------	
VCO SYN	20 VCOSNC	-------	-------	

TIME PRECOMPENSATION

UM9228-1 defines compensation time to be 250ns according to IBM PC design. UM8329's compensation time is programmable, while UM8326 does not have this function.

WRITE DATA

UM9228-1 and UM8329 have write data function in IC, but UM8326 does not; UM9228-1 has a "write enable" pin.

MODE SELECTION

UM8329 and UM8326 allow user to select different FDCs and to interface with different FDCs; UM9228-1 is typically used in 5½ FDD (MFM coding) interface.

DMA MODE

UM9228-1 can accept DMA requests and define delay time between two different DMA requests to be 5 μs.

VFO CIRCUIT

Because UM9228-1 does not have VFO or PLL circuit, user must combine MC4024 and MC4044 to have a complete data separator. Please see UM9228-1 application circuit.

Ordering Information

Part Number	Frequency Option	Package Type
UM8326	4MHz	Plastic
UM8326B	8MHz	Plastic