STANDARD MICROSYSTEMS CORPORATION

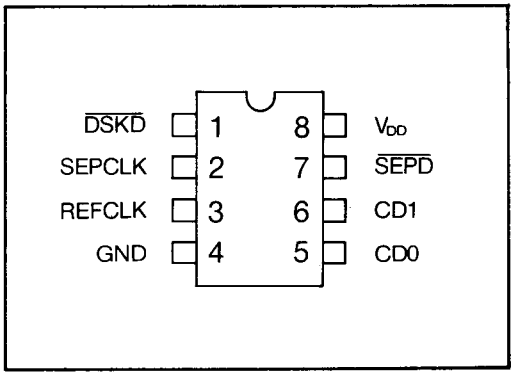
FDC 9216
FDC 9216B
μPC FAMILY

Floppy Disk Data Separator
FDDS

FEATURES

- ☐ PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- ☐ SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ☐ ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- ☐ NO CRITICAL ADJUSTMENTS REQUIRED
- ☐ COMPATIBLE WITH STANDARD MICROSYSTEMS' FDC 1791, FDC 1793 AND OTHER FLOPPY DISK CONTROLLERS
- ☐ SMALL 8-PIN DUAL-IN-LINE PACKAGE
- ☐ +5 VOLT ONLY POWER SUPPLY
- ☐ TTL COMPATIBLE INPUTS AND OUTPUTS

PIN CONFIGURATION



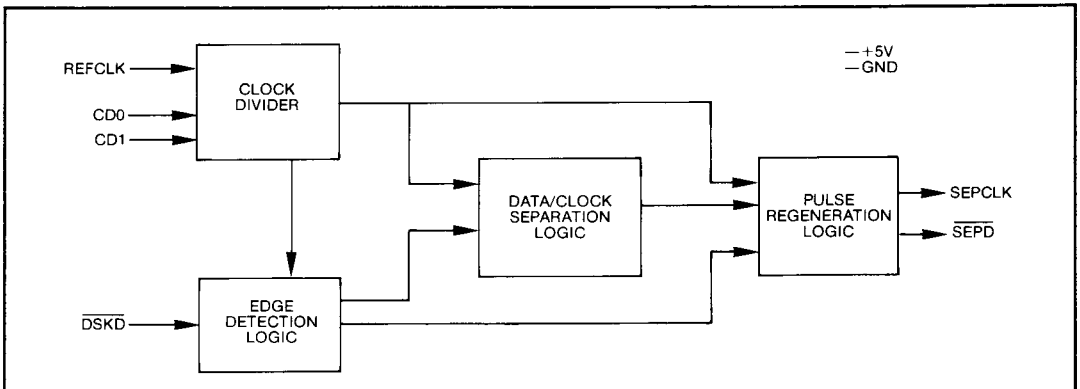
SECTION VI

GENERAL DESCRIPTION

The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The FDC 9216 is available in two versions; the FDC 9216, which is intended for 5¼" disks and the FDC 9216B for 5¼" and 8" disks.

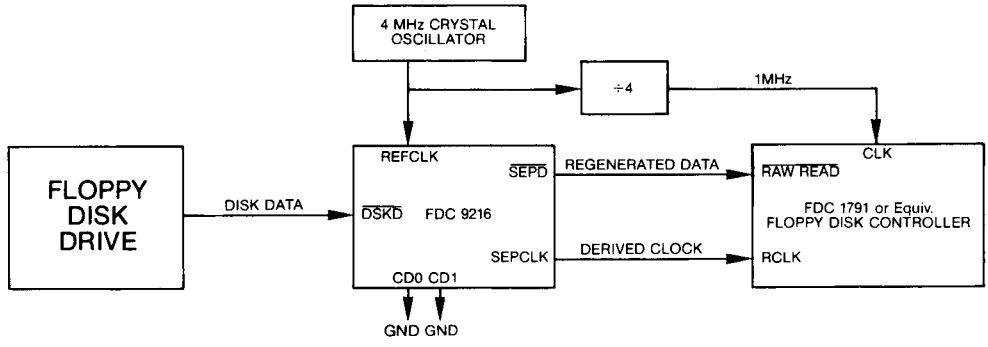


FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5, 6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS
8	Power Supply	V_{DD}	+5 volt power supply

FIGURE 1
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)



OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

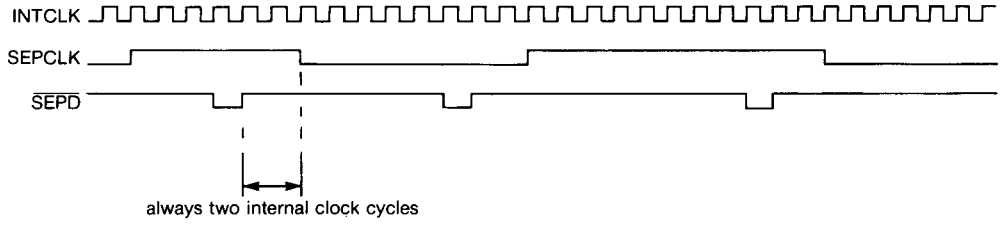
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8" or 5¼")	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	
8	SD	8	0	1	Select either one
8	SD	4	0	0	
5¼	DD	8	0	1	
5¼	DD	4	0	0	Select either one
5¼	SD	8	1	0	
5¼	SD	4	0	1	Select any one
5¼	SD	2	0	0	

FIGURE 2



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C, V_{DD}=+5V±5%, unless otherwise noted)

Parameter		Min.	Typ.	Max.	Units	Comments
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL}=1.6mA
High Level V_{OH}		2.4			V	I_{OH}=−100 μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$O \leq V_{IN} \leq V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				60	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{cy}	REFCLK Frequency	0.2		4.3	MHz	FDC 9216
f_{cy}	REFCLK Frequency	0.2		8.3	MHz	FDC 9216B
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay	25	100	250	ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay	25	100	250	ns	
t_{SPCK}	REFCLK to SEPCLK Delay	35			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

FIGURE 3: AC CHARACTERISTICS