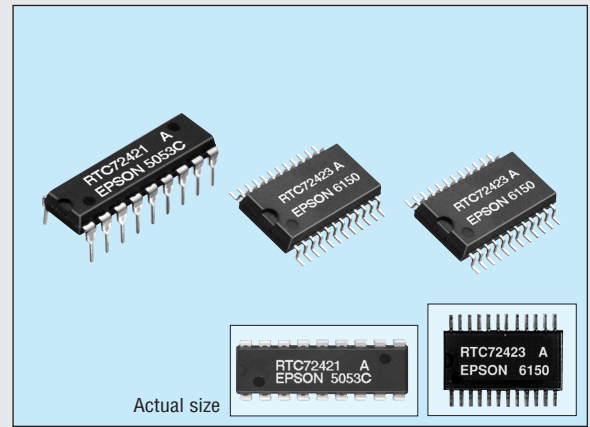


4-bit REAL TIME CLOCK MODULE

RTC-72421/72423

- Built-in crystal unit allows adjustment-free efficient operation.
- ALE input terminal available for 8048, 8051, and 8085 series.
- 12/24 h clock switchover function and automatic leap year setting.
- Interrupt masking.
- 30 second adjustment function.
- Low current consumption and features a backup function.



Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Specifications	Unit
Power source voltage	V _{DD}	T _a =+25 °C	-0.3 to 7.0	
Input and output voltage	V _{I/O}	T _a =+25 °C	GND -0.3 to V _{DD} +0.3	V
Storage temperature	T _{STG}	RTC-72421	-55 to +85	°C
		RTC-72423	-55 to +125	
Soldering condition	T _{SOL}	RTC-72421	Under +260 °C within 10 s (lead part) (package should be less than +150 °C)	
		RTC-72423	Twice at under +260 °C within 10 s or under +230 °C within 3 min.	

Operating range

Item	Symbol	Condition	Specifications	Unit
Operating voltage	V _{DD}		4.5 to 5.5	V
Operating temperature	T _{OPR}	RTC-72421	-10 to 70	°C
		RTC-72423	-40 to 85	
Data holding voltage	V _{DH}		2.0 to 5.5	V
CSI data holding time	t _{CDR}	Refer to the data holding timing	2.0 Min.	μs
Operation restoring time	t _r			

Frequency characteristics and current consumption characteristics

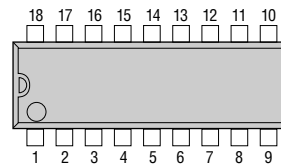
Item	Symbol	Condition	Specifications	Unit	
Frequency tolerance	Δf/fo	T _a =+25 °C	72421 A	±10	x 10 ⁻⁶
			72421 B	±50	
		V _{DD} =5 V	72423 A	±20	
			72423	±50	
Frequency temperature characteristics		-10 °C to +70 °C (+25 °C reference temperature)	+10/-120		
Aging	f _a	V _{DD} =5 V, T _a =+25 °C, first year	±5 Max.	x 10 ⁴ /year	
Shock resistance	S.R.	Three drops on a hard board from 750 mm or 29400 m/s ² x 0.3 ms x 1/2 sine wave x 3 directions	±10 Max.	x 10 ⁻⁶	
Current consumption	I _{DD1}	CS ₁ =0 V	V _{DD} =5 V	10 Max.	μA
	I _{DD2}	Exclude input/output current	V _{DD} =2 V	5 Max.	

DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable terminal
"H" input voltage (1)	V _{IH1}	—	2.2	—	—	V	All inputs other than CS ₁
"L" input voltage (1)	V _{IL1}						
Input leak current (1)	I _{LK1}	V ₁ =V _{DD} /0 V	—	—	±1	μA	Input other than Do to D ₃
Input leak current (2)	I _{LK2}				±10		
"L" output voltage (1)	V _{OL1}	I _{OL} =2.5 mA	2.4	—	0.4	V	Do to D ₃
"H" output voltage	V _{OH}				I _{OH} =-400 μA		
"L" output voltage (2)	V _{OL2}	I _{OL} =2.5 mA	—	—	0.4	V	STD.P
Off leak current	I _{OFFLK}	V ₁ =V _{DD} /0 V			10		
Input capacity	C ₁	Input frequency 1 MHz	10	—	—	pF	Input other than Do to D ₃
			20	—	—		
"H" input voltage (2)	V _{IH2}	V _{DD} =2 to 5.5 V	4/5 V _{DD}	—	—	V	CS ₁
"L" input voltage (2)	V _{IL2}		—	—	1/5 V _{DD}		

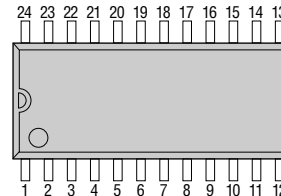
Terminal connection

RTC-72421



No.	72421	No.	72423
1	STD. P	1	STD. P
2	CS ₁	2	CS ₁
3	ALE	3	NC
4	A ₀	4	ALE
5	A ₁	5	A ₀
6	A ₂	6	NC
7	A ₃	7	A ₁
8	RD	8	NC
9	GND	9	A ₂
10	WR	10	A ₃
11	D ₁	11	RD
12	D ₂	12	GND
13	D ₁	13	WR
14	D ₂	14	D ₂
15	CS ₁	15	D ₂
16	(V _{DD})	16	D ₁
17	(V _{DD})	17	NC
18	V _{DD}	18	NC
		19	D ₁
		20	CS ₁
		21	NC
		22	(V _{DD})
		23	(V _{DD})
		24	V _{DD}

RTC-72423

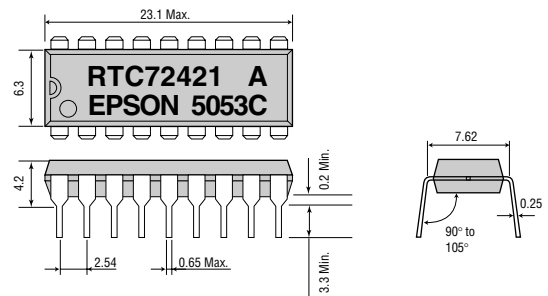


- (V_{DD}) and V_{DD} are to have the same level of voltage. Do not connect it to any external terminals.
- NC is not connected internally.

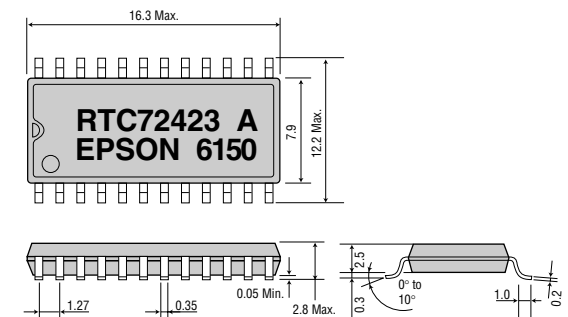
External dimensions

(Unit: mm)

RTC-72421



RTC-72423



Register table

Address	A ₃	A ₂	A ₁	A ₀	Register	Data				Count Value	Remarks
						D ₃	D ₂	D ₁	D ₀		
0	0	0	0	0	S ₁	s ₈	s ₄	s ₂	s ₁	0 to 9	1- second digit register
1	0	0	0	1	S ₁₀	*	s ₄₀	s ₂₀	s ₁₀	0 to 5	10- second digit register
2	0	0	1	0	MI ₁	mi ₈	mi ₄	mi ₂	mi ₁	0 to 9	1- minute digit register
3	0	0	1	1	MI ₁₀	*	mi ₄₀	mi ₂₀	mi ₁₀	0 to 5	10- minute digit register
4	0	1	0	0	H ₁	h ₈	h ₄	h ₂	h ₁	0 to 9	1- hour digit register
5	0	1	0	1	H ₁₀	*	PM/AM	h ₂₀	h ₁₀	0 to 2 or 0 to 1	PM/AM, 10- hours digit register
6	0	1	1	0	D ₁	d ₈	d ₄	d ₂	d ₁	0 to 9	1- day digit register
7	0	1	1	1	D ₁₀	*	*	d ₂₀	d ₁₀	0 to 3	10- day digit register
8	1	0	0	0	MO ₁	m ₀₈	m ₀₄	m ₀₂	m ₀₁	0 to 9	1- month digit register
9	1	0	0	1	MO ₁₀	*	*	*	m ₀₁₀	0 to 1	10- month digit register
A	1	0	1	0	Y ₁	y ₈	y ₄	y ₂	y ₁	0 to 9	1- year digit register
B	1	0	1	1	Y ₁₀	y ₈₀	y ₄₀	y ₂₀	y ₁₀		10- year digit register
C	1	1	0	0	W	*	w ₄	w ₂	w ₁	0 to 6	Week register
D	1	1	0	1	RegD	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	—	Control Register D
E	1	1	1	0	RegE	t ₁	t ₀	ITRPT/ STND	MASK		Control Register E
F	1	1	1	1	RegF	TEST	24/12	STOP	REST		Control Register F

0="L" level, 1="H" level, REST = RESET ITRPT/ STND=INTERRUPT/STANDARD

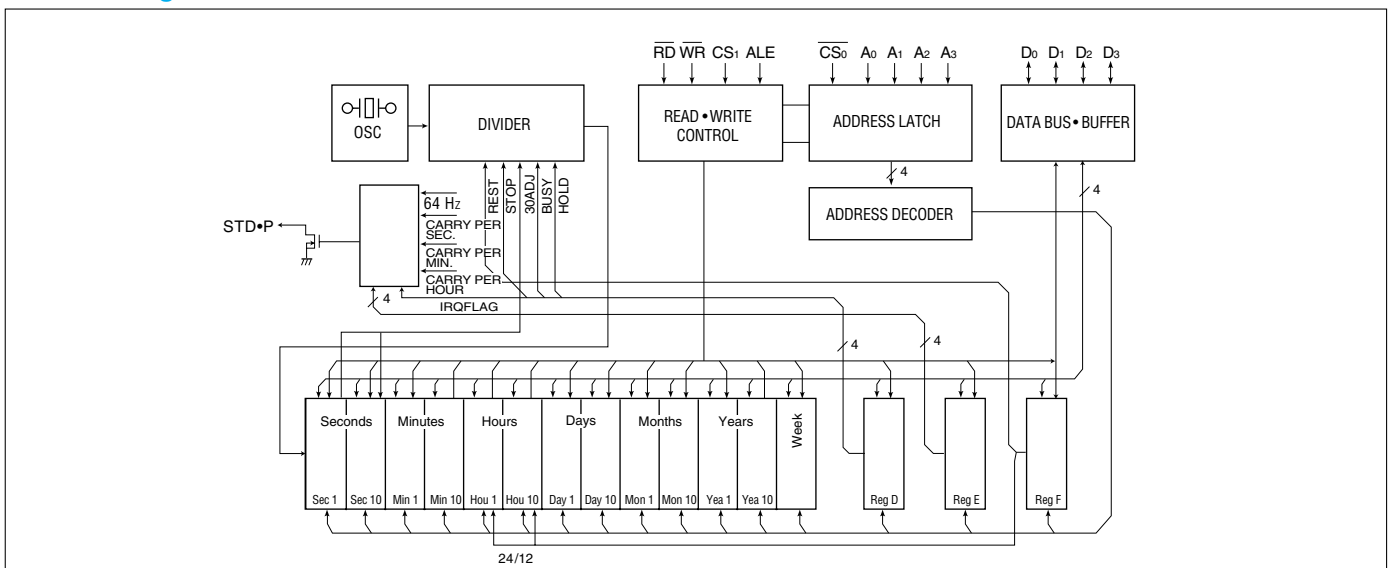
- Bit * does not exist.
- Please mask AM/PM bit with 10's of hours operations.
- Busy is read only. IRQ can only. IRQ can only be set low ("0").
- | Data Bit | PM/AM | ITRPT/STND | 24/12 |
|----------|-------|------------|-------|
| 1 | PM | ITRPT | 24 |
| 0 | AM | STND | 12 |
- TEST bit should be "0".

Switching characteristics (with ALE)

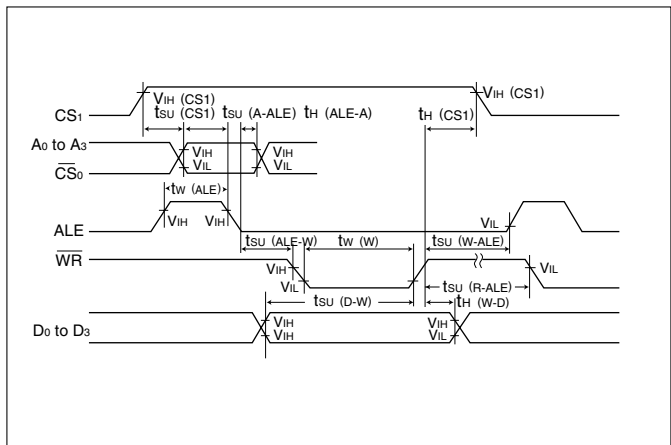
(Please connect ALE to V_{DD} if the microprocessor does not have an ALE output.)
(V_{DD} = 5 V ± 0.5 V)

Item	Symbol	Condition	Min.	Max.	Unit
CS ₁ setup time	t _{SU} (CS1)		1000		ns
Address setup time before ALE	t _{SU} (A-ALE)		50		
Address hold time after ALE	t _H (ALE-A)		50		
ALE pulse width	t _W (ALE)		80		
ALE setup time before WRITE	t _{SU} (ALE-W)		0		
ALE setup time before READ	t _{SU} (ALE-R)		0		
ALE setup time after WRITE	t _{SU} (W-ALE)		50		
ALE setup time after READ	t _{SU} (R-ALE)		50		
WRITE pulse width	t _W (W)		120		
DATA delay time after READ	t _{PZV} (R-Q)	C _L =150 pF	—	120	
DATA Hold time after READ	t _{PVZ} (R-Q)		0	70	
DATA setup time before WRITE	t _{SU} (D-W)		80		
DATA hold time after WRITE	t _H (W-D)		10		
CS ₁ hold time	t _H (CS1)		1000		
READ/WRITE recovery time	t _{REC} (R/W)		200		

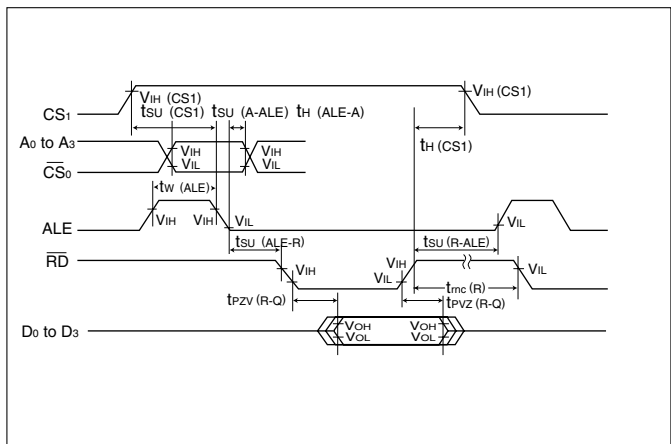
Block diagram



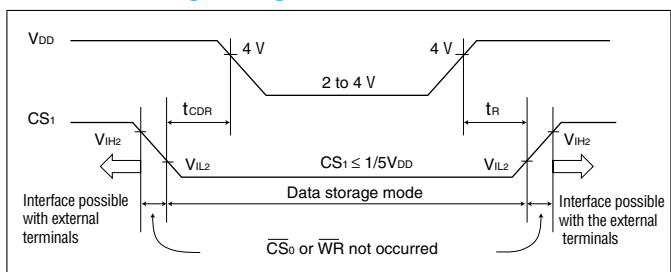
Write mode (with ALE)



Read mode (with ALE)



Data holding timing



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