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# 1-MBIT (128K x 8)
# BOOT BLOCK FLASH MEMORY
## 28F001BX-T/28F001BX-B/28F001BN-T/28F001BN-B

- **High-Integration Blocked Architecture**
  - **One 8 KB Boot Block w/Lock Out**
  - **Two 4 KB Parameter Blocks**
  - **One 112 KB Main Block**

- **100,000 Erase/Program Cycles Per Block**

- **Simplified Program and Erase**
  - **Automated Algorithms via On-Chip Write State Machine (WSM)**

- **SRAM-Compatible Write Interface**

- **Deep Power-Down Mode**
  - **0.05 $\mu$A $I_{CC}$ Typical**
  - **0.8 $\mu$A $I_{PP}$ Typical**

- **12.0V $\pm$5% $V_{PP}$**

- **High-Performance Read**
  - **70/75 ns, 90 ns, 120 ns, 150 ns Maximum Access Time**
  - **5.0V $\pm$10% $V_{CC}$**

- **Hardware Data Protection Feature**
  - **Erase/Write Lockout during Power Transitions**

- **Advanced Packaging, JEDEC Pinouts**
  - **32-Pin PDIP**
  - **32-Lead PLCC, TSOP**

- **ETOX™ II Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**

- **Extended Temperature Options**

Intel's 28F001BX-B and 28F001BX-T combine the cost-effectiveness of Intel standard flash memory with features that simplify write and allow block erase. These devices aid the system designer by combining the functions of several components into one, making boot block flash an innovative alternative to EPROM and EEPROM or battery-backed static RAM. Many new and existing designs can take advantage of the 28F001BX's integration of blocked architecture, automated electrical reprogramming, and standard processor interface.

The 28F001BX-B and 28F001BX-T are 1,048,576 bit nonvolatile memories organized as 131,072 bytes of 8 bits. They are offered in 32-pin plastic DIP, 32-lead PLCC and 32-lead TSOP packages. Pin assignment conform to JEDEC standards for byte-wide EPROMs. These devices use an integrated command port and state machine for simplified block erasure and byte reprogramming. The 28F001BX-T's block locations provide compatibility with microprocessors and microcontrollers that boot from high memory, such as Intel's MCS®-186 family, 80286, i386™, i486™, i860™ and 80960CA. With exactly the same memory segmentation, the 28F001BX-B memory map is tailored for microprocessors and microcontrollers that boot from low memory, such as Intel's MCS-51, MCS-196, 80960KX and 80960SX families. All other features are identical, and unless otherwise noted, the term 28F001BX can refer to either device throughout the remainder of this document.

The boot block section includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to the other locations of the 28F001BX. Intel's 28F001BX employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. A deep-powerdown mode lowers power consumption to 0.25 $\mu$W typical through $V_{CC}$, crucial in laptop computer, handheld instrumentation and other low-power applications. The RP# power control input also provides absolute data protection during system powerup or power loss.

Manufactured on Intel's ETOX process base, the 28F001BX builds on years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

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# NOTE: The 28F001BN is equivalent to the 28F001BX.
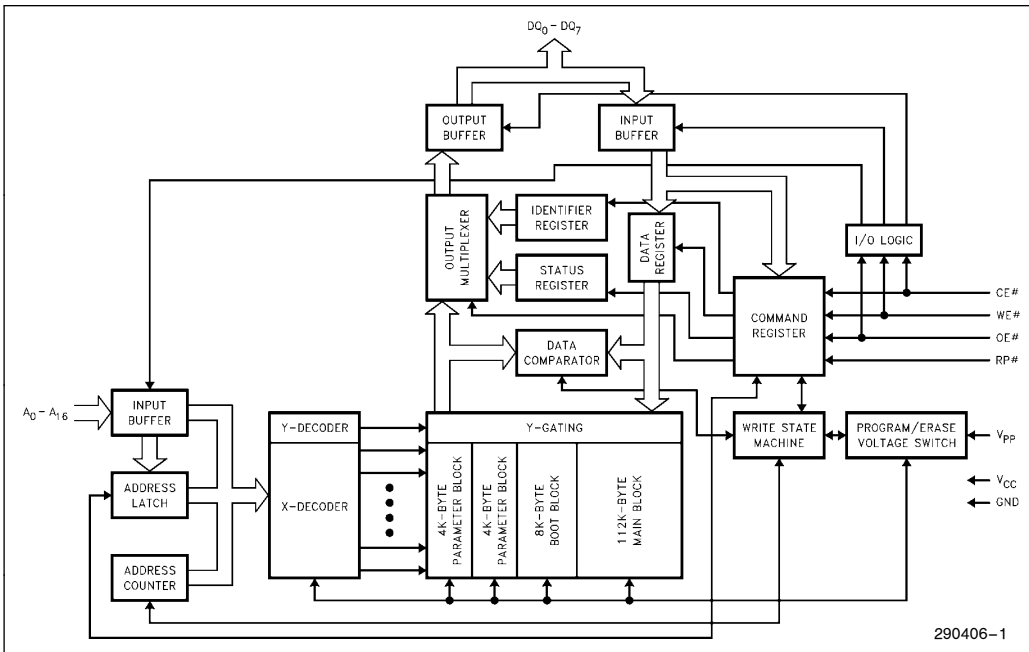
**Figure 1. 28F001BX Block Diagram**

**Table 1. Pin Description**

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0-A_{16}$ | INPUT | **ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. |
| $DQ_0-DQ_7$ | INPUT/ OUTPUT | **DATA INPUTS/OUTPUTS:** Inputs data and commands during memory write cycles; outputs data during memory, Status Register and Identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle. |
| CE# | INPUT | **CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low; CE# high deselects the memory device and reduces power consumption to standby levels. |
| RP# | INPUT | **POWERDOWN:** Puts the device in deep powerdown mode. RP# is active low; RP# high gates normal operation. RP# = $V_{HH}$ allows programming of the boot block. RP# also locks out erase or write operations when active low, providing data protection during power transitions. RP# active resets internal automation. Exit from deep powerdown sets device to Read Array mode. |
| OE# | INPUT | **OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. OE# is active low. OE# = $V_{HH}$ (pulsed) allows programming of the boot block. |
| WE# | INPUT | **WRITE ENABLE:** Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse. |
| $V_{PP}$ | | **ERASE/PROGRAM POWER SUPPLY** for erasing blocks of the array or programming bytes of each block. Note: With $V_{PP} < V_{PPL}$ max, memory contents cannot be altered. |
| $V_{CC}$ | | **DEVICE POWER SUPPLY:** (5V ±10%) |
| GND | | **GROUND** |

**Figure 2. DIP Pin Configuration**

**Figure 3. TSOP Lead Configuration**

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| 28F010 | | | | | | | NC |
|---|---|---|---|---|---|---|---|
| 28F001BX(128K×8) | $A_{12}$ | $A_{15}$ | $A_{16}$ | $V_{PP}$ | $V_{CC}$ | WE# | RP# |



N28F001BX
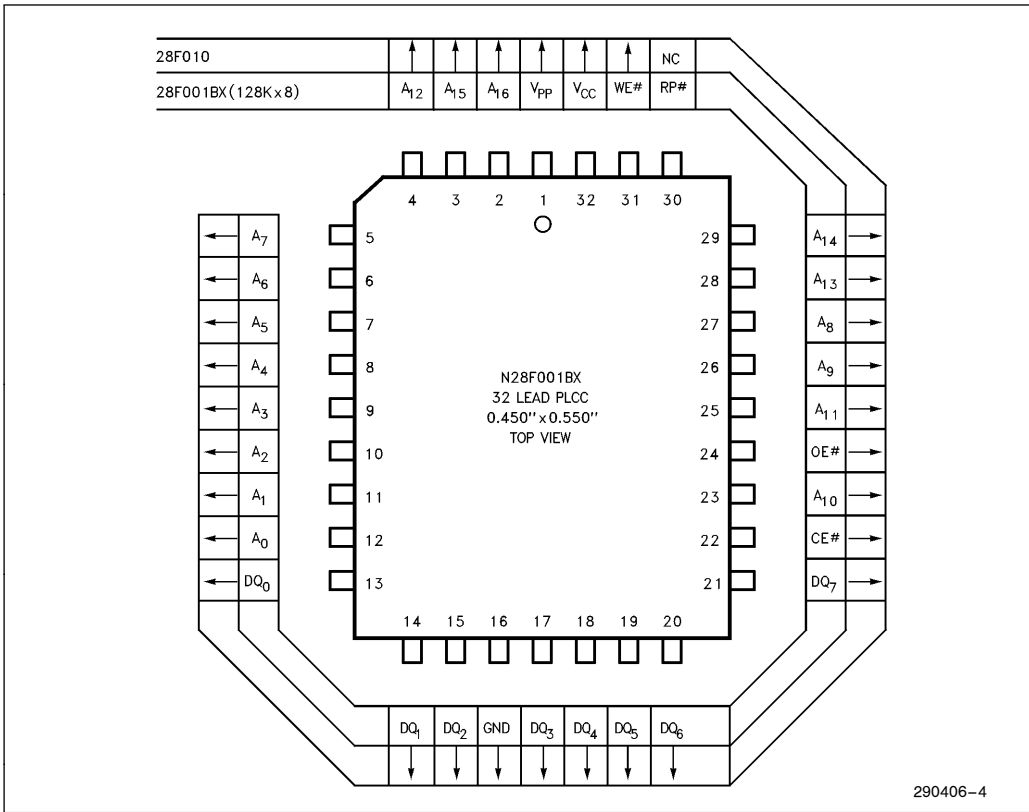32 LEAD PLCC
0.450″×0.550″
TOP VIEW

290406−4

**Figure 4. PLCC Lead Configuration**

## APPLICATIONS

The 28F001BX flash 'boot block' memory augments the non-volatility, in-system electrical erasure and reprogrammability of Intel's standard flash memory by offering four separately erasable blocks and integrating a state machine to control erase and program functions. The specialized blocking architecture and automated programming of the 28F001BX provide a full-function, non-volatile flash memory ideal for a wide range of applications, including PC boot/BIOS memory, minimum-chip embedded program memory and parametric data storage. The 28F001BX combines the safety of a hardware-protected 8-KByte boot block with the flexibility of three separately reprogrammable blocks (two 4-KByte parameter blocks and one 112-KByte code block) into one versatile, cost-effective flash memory. Additionally, reprogramming one block does not affect code stored in another block, ensuring data integrity.

The flexibility of flash memory reduces costs throughout the life cycle of a design. During the early stages of a system's life, flash memory reduces prototype development and testing time, allowing the system designer to modify in-system software electrically versus manual removal of components. During production, flash memory provides flexible firmware for just-in-time configuration, reducing system inventory and eliminating unnecessary handling and less reliable socketed connections. Late in the life cycle, when software updates or code "bugs" are often unpredictable and costly, flash memory reduces update costs by allowing the manufacturers to send floppy updates versus a technician. Alternatively, remote updates over a communication link are possible at speeds up to 9600 baud due to flash memory's fast programming time.

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Reprogrammable environments, such as the personal computer, are ideal applications for the 28F001BX. The internal state machine provides SRAM-like timings for program and erasure, using the Command and Status Registers. The blocking scheme allows BIOS update in the main and parameter blocks, while still providing recovery code in the boot block in the unlikely event a power failure occurs during an update, or where BIOS code is corrupted. Parameter blocks also provide convenient configuration storage, backing up SRAM and battery configurations. EISA systems, for example, can store hardware configurations in a flash parameter block, reducing system SRAM.

Laptop BIOSs are becoming increasingly complex with the addition of power management software and extended system setup screens. BIOS code complexity increases the potential for code updates after the sale, but the compactness of laptop designs makes hardware updates very costly. Boot block flash memory provides an inexpensive update solution for laptops, while reducing laptop obsolescence. For portable PCs and hand-held equipment, the deep powerdown mode dramatically lowers system power requirements during periods of slow operation or sleep modes.

The 28F001BX gives the embedded system designer several desired features. The internal state machine reduces the size of external code dedicated to the erase and program algorithms, as well as freeing the microcontroller or microprocessor to respond to other system requests during program and erasure. The four blocks allow logical segmentation of the entire embedded software: the 8-KByte block for the boot code, the 112-KByte block for the main program code and the two 4-KByte blocks for updatable parametric data storage, diagnostic messages and data, or extensions of either the boot code or program code. The boot block is hardware protected against unauthorized write or erase of its vital code in the field. Further, the powerdown mode also locks out erase or write operations, providing absolute data protection during system powerup or power loss. This hardware protection provides obvious advantages for safety related applications such as transportation, military, and medical. The 28F001BX is well suited for minimum-chip embedded applications ranging from communications to automotive.
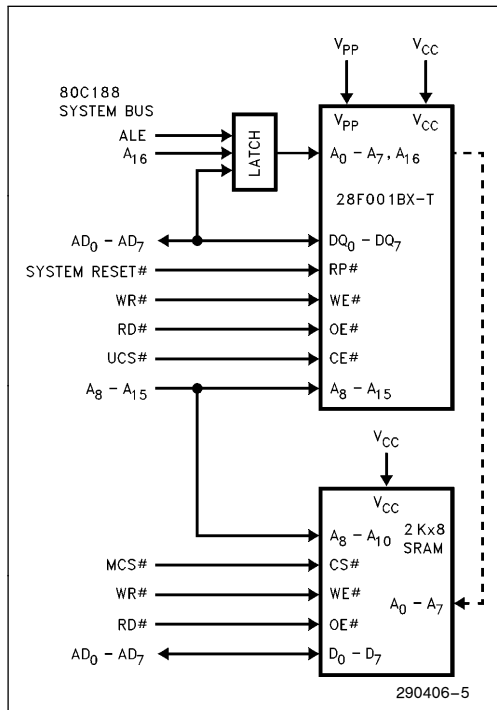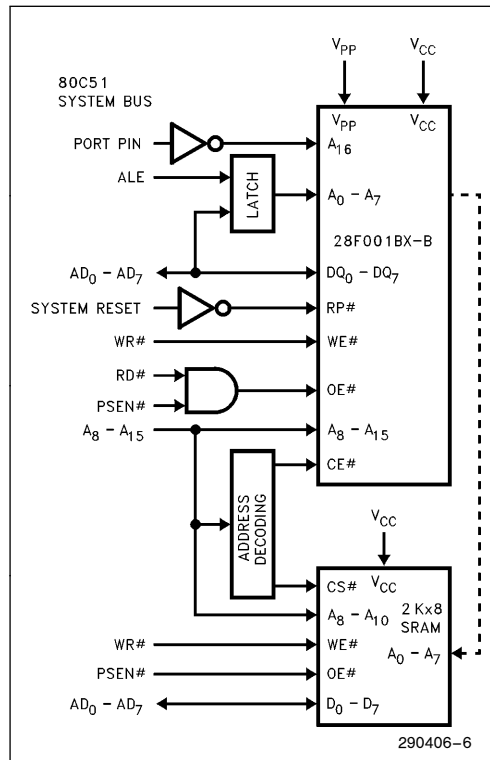


**Figure 5. 28F001BX-T in a 80C188 System**



**Figure 6. 28F001BX-B in a 80C51 System**

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## PRINCIPLES OF OPERATION

The 28F001BX introduces on-chip write automation to manage write and erase functions. The write state machine allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, minimal processor overhead with RAM-like write timings, and maximum EPROM compatiblity.

After initial device powerup, or after return from deep powerdown mode (see Bus Operations), the 28F001BX functions as a read-only memory. Manipulation of external memory-control pins yield standard EPROM read, standby, output disable or Intelligent Identifier operations. Both Status Register and Intelligent Identifiers can be accessed through the Command Register when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the $V_{PP}$ pin. In addition, high voltage on $V_{PP}$ enables successful erasure and programming of the device. All functions associated with altering memory contents—program, erase, status, and int$_e$ligent Identifier—are accessed via the Command Register and verified through the Status Register.

Commands are written using standard microprocessor write timings. Register contents serve as input to the WSM, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output program and erase status for verification.

Interface software to initiate and poll progress of internal program and erase can be stored in any of the 28F001BX blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of program and/or erase, code execution out of the 28F001BX is again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase and read data/execute code from any other block.

## Command Register and Write Automation

An on-chip state machine controls block erase and byte program, freeing the system processor for other tasks. After receiving the erase setup and erase confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the Status Register. Programming is similarly controlled, after destination address and expected data are supplied. The program algorithm of past Intel Flash Memories is now regulated by the state machine, including program pulse repetition where required and internal verification and margining of data.

## Data Protection

Depending on the application, the system designer may choose to make the $V_{PP}$ power supply switchable (available only when memory updates are required) or hardwired to $V_{PPH}$. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. The 28F001BX Command Register architecture provides protection from unwanted program or erase operations even when high voltage is applied to $V_{PP}$. Additionally, all functions are disabled whenever $V_{CC}$ is below the write lockout voltage $V_{LKO}$, or when RP# is at $V_{IL}$. The 28F001BX accommodates either design practice and encourages optimization of the processor-memory interface.

The two-step program/erase write sequence to the Command Register provides additional software write protection.
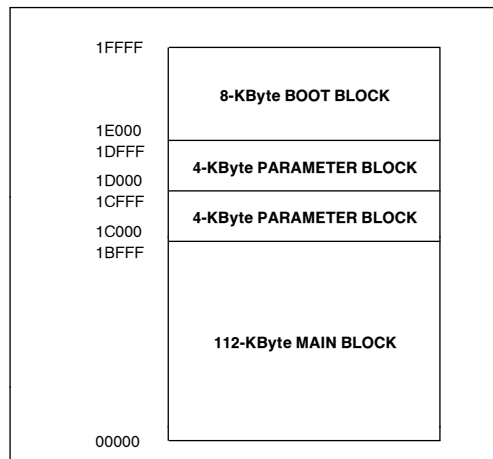


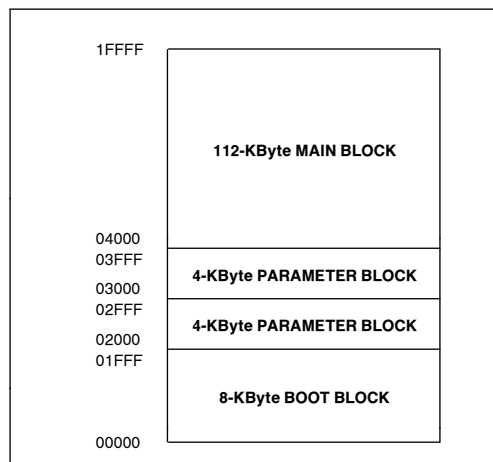**Figure 7. 28F001BX-T Memory Map**



**Figure 8. 28F001BX-B Memory Map**

## BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

## Read

The 28F001BX has three read modes. The memory can be read from any of its blocks, and information can be read from the Intelligent Identifier or the Status Register. $V_{PP}$ can be at either $V_{PPL}$ or $V_{PPH}$.

The first task is to write the appropriate read mode command to the Command Register (array, Intelligent Identifier, or Status Register). The 28F001BX automatically resets to Read Array mode upon initial device powerup or after exit from deep powerdown. The 28F001BX has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable (CE#) is the device selection control, and when active enables the selected memory device. Output Enable (OE#) is the data input/output ($DQ_0$–$DQ_7$) direction control, and when active drives data from the selected memory onto the I/O bus. RP# and WE# must also be at $V_{IH}$. Figure 12 illustrates read bus cycle waveforms.

## Output Disable

With OE# at a logic-high level ($V_{IH}$), the device outputs are disabled. Output pins ($DQ_0$–$DQ_7$) are placed in a high-impedance state.

## Standby

CE# at a logic-high level ($V_{IH}$) places the 28F001BX in standby mode. Standby operation disables much of the 28F001BX's circuitry and substantially reduces device power consumption. The outputs ($DQ_0$–$DQ_7$) are placed in a high-impedance state independent of the status of OE#. If the 28F001BX is deselected during erase or program, the device will continue functioning and consuming normal active power until the operation is completed.

## Deep Power-Down

The 28F001BX offers a 0.25 $\mu$W $V_{CC}$ power-down feature, entered when RP# is at $V_{IL}$. During read modes, RP# low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The 28F001BX requires time $t_{PHQV}$ (see AC Characteristics-Read Only Operations) after return from power-down until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command Register is reset to Read Array, and the Status Register is cleared to value 80H, upon return to normal operation.

During erase or program modes, RP# low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially programmed or erased. Time $t_{PHWL}$ after RP# goes to logic-high ($V_{IH}$) is required before another command can be written.

### Table 2. 28F001BX Bus Operations

| Mode | Notes | RP# | CE# | OE# | WE# | $A_9$ | $A_0$ | $V_{PP}$ | $DQ_{0-7}$ |
|---|---|---|---|---|---|---|---|---|---|
| Read | 1, 2, 3 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | X | $D_{OUT}$ |
| Output Disable | 2 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | X | High Z |
| Standby | 2 | $V_{IH}$ | $V_{IH}$ | X | X | X | X | X | High Z |
| Deep Power Down | 2 | $V_{IL}$ | X | X | X | X | X | X | High Z |
| Intelligent Identifier (Mfr) | 2, 3, 4 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{IL}$ | X | 89H |
| Intelligent Identifier (Device) | 2, 3, 4, 5 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{IH}$ | X | 94H, 95H |
| Write | 2, 6, 7, 8 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | X | $D_{IN}$ |

**NOTES:**
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not programmed or erased.
2. X can be $V_{IL}$ or $V_{IH}$ for control pins and addresses, and $V_{PPL}$ or $V_{PPH}$ for $V_{PP}$.
3. See DC Characteristics for $V_{PPL}$, $V_{PPH}$, $V_{HH}$ and $V_{ID}$ voltages.
4. Manufacturer and device codes may also be accessed via a Command Register write sequence. Refer to Table 3. $A_1$–$A_8$, $A_{10}$–$A_{16} = V_{IL}$.
5. Device ID = 94H for the 28F001BX-T and 95H for the 28F001BX-B.
6. Command writes involving block erase or byte program are successfully executed only when $V_{PP} = V_{PPH}$.
7. Refer to Table 3 for valid $D_{IN}$ during a write operation.
8. Program or erase the boot block by holding RP# at $V_{HH}$ or toggling OE# to $V_{HH}$. See AC Waveforms for program/erase operations.

The use of RP# during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during write/ erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur because the flash memory would be providing the status information instead of array data. Intel's Flash Memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application RP# is controlled by the same RESET# signal that resets the system CPU.

## Intelligent Identifier Operation

The Intelligent Identifier operation outputs the manufacturer code, 89H; and the device code, 94H for the 28F001BX-T and 95H for the 28F001BX-B. Programming equipment or the system CPU can then automatically match the device with its proper erase and programming algorithms.

### PROGRAMMING EQUIPMENT

CE# and OE# at a logic low level ($V_{IL}$), with $A_9$ at high voltage $V_{ID}$ (see DC Characteristics) activates this operation. Data read from locations 00000H and 00001H represent the manufacturer's code and the device code respectively.

### IN-SYSTEM PROGRAMMING

The manufacturer- and device-codes can also be read via the Command Register. Following a write of 90H to the Command Register, a read from address location 00000H outputs the manufacturer code (89H). A read from address 00001H outputs the device code (94H for the 28F001BX-T and 95H for the 28F001BX-B). It is not necessary to have high voltage applied to $V_{PP}$ to read the Intelligent Identifiers from the Command Register.

## Write

Writes to the Command Register allow read of device data and Intelligent Identifiers. They also control inspection and clearing of the Status Register. Additionally, when $V_{PP} = V_{PPH}$, the Command Register controls device erasure and programming. The contents of the register serve as input to the internal state machine.

The Command Register itself does not occupy an addressable memory location. The register is a latch used to store the command and address and data information needed to execute the command. Erase

Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Program Setup Command requires both appropriate command data and the address of the location to be programmed, while the Program command consists of the data to be written and the address of the location to be programmed.

The Command Register is written by bringing WE# to a logic-low level ($V_{IL}$) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveform for Write Operations, Figure 13, for specific timing parameters.

## COMMAND DEFINITIONS

When $V_{PPL}$ is applied to the $V_{PP}$ pin, read operations from the Status Register, intelligent identifiers, or array blocks are enabled. Placing $V_{PPH}$ on $V_{PP}$ enables successful program and erase operations as well.

Device operations are selected by writing specific commands into the Command Register. Table 3 defines these 28F001BX commands.

## Read Array Command

Upon initial device powerup and after exit from deep-powerdown mode, the 28F001BX defaults to Read Array mode. This operation is also initiated by writing FFH into the Command Register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the Command Register contents are altered. Once the internal write state machine has started an erase or program operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or $V_{PPH}$.

## Intelligent Identifier Command for In-System Programming

The 28F001BX contains an Intelligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the Command Register. Following the command write, a read cycle from address 00000H retrieves the manufacturer code of 89H. A read cycle from address 00001H returns the device code of 94 (28F001BX-T) or 95H (28F001BX-B). To terminate the operation, it is necessary to write another valid command into the register. Like the Read Array command, the Intelligent Identifier command is functional when $V_{PP} = V_{PPL}$ or $V_{PPH}$.

**Table 3. 28F001BX Command Definitions**

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|
| | | | Operation | Address | Data | Operation | Address | Data |
| Read Array/Reset | 1 | 1 | Write | X | FFH | | | |
| Intelligent Identifier | 3 | 2, 3, 4 | Write | X | 90H | Read | IA | IID |
| Read Status Register | 2 | 3 | Write | X | 70H | Read | X | SRD |
| Clear Status Register | 1 | | Write | X | 50H | | | |
| Erase Setup/Erase Confirm | 2 | 2 | Write | BA | 20H | Write | BA | D0H |
| Erase Suspend/Erase Resume | 2 | | Write | X | B0H | Write | X | D0H |
| Program Setup/Program | 2 | 2, 3 | Write | PA | 40H | Write | PA | PD |

**NOTES:**
1. Bus operations are defined in Table 2.
2. IA = Identifier Address: 00H for manufacturer code, 01H for device code.
   BA = Address within the block being erased.
   PA = Address of memory location to be programmed.
3. SRD = Data read from Status Register. See Table 4 for a description of the Status Register bits.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of WE#.
   IID = Data read from Intelligent Identifiers.
4. Following the Intelligent Identifier command, two read operations access manufacture and device codes.
5. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

## Read Status Register Command

The 28F001BX contains a Status Register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status Register command (70H) to the Command Register. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command Register. The contents of the Status Register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle. OE# or CE# must be toggled to $V_{IH}$ before further reads to update the Status Register latch. The Read Status Register command functions when $V_{PP} = V_{PPL}$ or $V_{PPH}$.

## Clear Status Register Command

The Erase Status and Program Status bits are set to "1" by the Write State Machine and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 4). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that series. This adds flexibility to the way the device may be used.

Additionally, the $V_{PP}$ Status bit (SR.3), when set to "1", MUST be reset by system software before further byte programs or block erases are attempted. To clear the Status Register, the Clear Status Register command (50H) is written to the Command Register. The Clear Status Register command is functional when $V_{PP} = V_{PPL}$ or $V_{PPH}$.

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**Table 4. 28F001BX Status Register Definitions**

| WSMS | ESS | ES | PS | VPPS | R | R | R |
|------|-----|----|----|------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

SR.7 = WRITE STATE MACHINE STATUS
   1 = Ready
   0 = Busy

SR.6 = ERASE SUSPEND STATUS
   1 = Erase Suspended
   0 = Erase In Progress/Completed

SR.5 = ERASE STATUS
   1 = Error in Block Erasure
   0 = Successful Block Erase

SR.4 = PROGRAM STATUS
   1 = Error in Byte Program
   0 = Successful Byte Program

SR.3 = $V_{PP}$ STATUS
   1 = $V_{PP}$ Low Detect; Operation Abort
   0 = $V_{PP}$ OK

SR.2–SR.0 = RESERVED FOR FUTURE ENHANCE-MENTS
These bits are reserved for future use and should be masked out when polling the Status Register.

**NOTES:**
The Write State Machine Status Bit must first be checked to determine program or erase completion, before the Program or Erase Status bits are checked for success.

If the Program AND Erase Status bits are set to "1s" during an erase attempt, an improper command sequence was entered. Attempt the operation again.

If $V_{PP}$ low status is detected, the Status Register must be cleared before another program or erase operation is attempted.

The $V_{PP}$ Status bit, unlike an A/D converter, does not provide continuous indication of $V_{PP}$ level. The WSM interrogates the $V_{PP}$ level only after the program or erase command sequences have been entered and informs the system if $V_{PP}$ has not been switched on. The $V_{PP}$ Status bit is not guaranteed to report accurate feedback between $V_{PPL}$ and $V_{PPH}$.

## Erase Setup/Erase Confirm Commands

Erase is executed one block at a time, initiated by a two-cycle command sequence. An Erase Setup command (20H) is first written to the Command Register, followed by the Erase Confirm command (D0H). These commands require both appropriate command data and an address within the block to be erased. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After receiving the two-command erase sequence, the 28F001BX automatically outputs Status Register data when read (see Figure 10; Block Erase Flowchart). The CPU can detect the completion of the erase event by checking the WSM Status bit of the Status Register (SR.7).

When the Status Register indicates that erase is complete, the Erase Status bit should be checked. If erase error is detected, the Status Register should be cleared. The Command Register remains in Read Status Register Mode until further commands are issued to it.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, block erasure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$,

the $V_{PP}$ Status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

## Erase Suspend/Erase Resume Commands

The Erase Suspend Command allows erase sequence interruption in order to read data from another block of memory. Once the erase sequence is started, writing the Erase Suspend command (B0H) to the Command Register requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The 28F001BX continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended (both will be set to "1s").

At this point, a Read Array command can be written to the Command Register to read data from blocks **other than that which is suspended**. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H), at which time the WSM will continue with the erase sequence. The Erase Suspend Status and WSM Status bits of the Status Register will be cleared. After the Erase Resume command is written to it, the 28F001BX automatically outputs Status Register data when read (see Figure 11; Erase Suspend/Resume Flowchart).

### Program Setup/Program Commands

Programming is executed by a two-write sequence. The program Setup command (40H) is written to the Command Register, followed by a second write specifying the address and data (latched on the rising edge of WE#) to be programmed. The WSM then takes over, controlling the program and verify algorithms internally. After the two-command program sequence is written to it, the 28F001BX automatically outputs Status Register data when read (see Figure 9; Byte Program Flowchart). The CPU can detect the completion of the program event by analyzing the WSM Status bit of the Status Register. Only the Read Status Register command is valid while programming is active.

When the Status Register indicates that programming is complete, the Program Status bit should be checked. If program error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for "1s" that do not successfully program to "0s". The Command Register remains in Read Status Register mode until further commands are issued to it. If byte program is attempted while $V_{PP} = V_{PPL}$, the $V_{PP}$ Status bit will be set to "1". Program attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

### EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled; an expensive solution.

Intel has designed extended cycling capability into its ETOX flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electrical field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 Mv/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure.

The 28F001BX-B and 28F001BX-T are capable of 100,000 program/erase cycles on each parameter block, main block and boot block.

### ON-CHIP PROGRAMMING ALGORITHM

The 28F001BX integrates the Quick Pulse programming algorithm of prior Intel Flash Memory devices on-chip, using the Command Register, Status Register and Write State Machine (WSM). On-chip integration dramatically simplifies system software and provides processor-like interface timings to the Command and Status Registers. WSM operation, internal program verify and $V_{PP}$ high voltage presence are monitored and reported via appropriate Status Register bits. Figure 9 shows a system software flowchart for device programming. The entire sequence is performed with $V_{PP}$ at $V_{PPH}$. Program abort occurs when RP# transitions to $V_{IL}$, or $V_{PP}$ drops to $V_{PPL}$. Although the WSM is halted, byte data is partially programmed at the location where programming was aborted. Block erasure or a repeat of byte programming will initialize this data to a known value.

### ON-CHIP ERASE ALGORITHM

As above, the Quick Erase algorithm of prior Intel Flash Memory devices is now implemented internally, including all preconditioning of block data. WSM operation, erase success and $V_{PP}$ high voltage presence are monitored and reported through the Status Register. Additionally, if a command other than Erase Confirm is written to the device after Erase Setup has been written, both the Erase Status and Program Status bits will be set to "1". When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 10 shows a system software flowchart for block erase.

Erase typically takes 1–4 seconds per block. The Erase Suspend/Erase Resume command sequence allows interrupt of this erase operation to read data **from a block other than that in which erase is being performed**. A system software flowchart is shown in Figure 11.

The entire sequence is performed with $V_{PP}$ at $V_{PPH}$. Abort occurs when RP# transitions to $V_{IL}$ or $V_{PP}$ falls to $V_{PPL}$, while erase is in progress. Block data is partially erased by this operation, and a repeat of erase is required to obtain a fully erased block.

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## BOOT BLOCK PROGRAM AND ERASE

The boot block is intended to contain secure code which will minimally bring up a system and control programming and erase of other blocks of the device, if needed. Therefore, additional "lockout" protection is provided to guarantee data integrity. Boot block program and erase operations are enabled through high voltage $V_{HH}$ on either RP# or OE#, and the normal program and erase command sequences are used. Reference the AC Waveforms for Program/Erase.

If boot block program or erase is attempted while RP# is at $V_{IH}$, either the Program Status or Erase Status bit will be set to "1", reflective of the opera-tion being attempted and indicating boot block lock. Program/erase attempts while $V_{IH} < RP# < V_{HH}$ produce spurious results and should not be attempted.

### In-System Operation

For on-board programming, the RP# pin is the most convenient means of altering the boot block. Before issuing Program or Erase confirms commands, RP# must transition to $V_{HH}$. Hold RP# at this high voltage throughout the program or erase interval (until after Status Register confirm of successful completion). At this time, it can return to $V_{IH}$ or $V_{IL}$.



| Bus Operation | Command | Comments |
|---|---|---|
| Write | Program Setup | Data = 40H<br>Address = Byte to be Programmed |
| Write | Program | Data to be programmed<br>Address = Byte to be Programmed |
| Read | | Status Register Data.<br>Toggle OE# or CE# to update Status Register |
| Standby | | Check SR.7<br>1 = Ready, 0 = Busy |

Repeat for subsequent bytes.

Full status check can be done after each byte or after a sequence of bytes.

Write FFH after the last byte programming operation to reset the device to Read Array Mode.

| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1 = $V_{PP}$ Low Detect |
| Standby | | Check SR.4<br>1 = Byte Program Error |

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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**Figure 9. 28F001BX Byte Programming Flowchart**

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| Bus Operation | Command | Comments |
|---|---|---|
| Write | Erase Setup | Data = 20H<br>Address = Within Block to be erased |
| Write | Erase | Data = D0H<br>Address = Within Block to be erased |
| Read | | Status Register Data.<br>Toggle OE # or CE # to update Status Register |
| Standby | | Check SR.7<br>1 = Ready, 0 = Busy |

Repeat for subsequent blocks.

Full status check can be done after each block or after a sequence of blocks.

Write FFH after the last block erase operation to reset the device to Read Array Mode.

**FULL STATUS CHECK PROCEDURE**

| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1 = $V_{PP}$ Low Detect |
| Standby | | Check SR.4, 5<br>Both 1 = Command Sequence Error |
| Standby | | Check SR.5<br>1 = Block Erase Error |

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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**Figure 10. 28F001BX Block Erase Flowchart**

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**intel**



| Bus Operation | Command | Comments |
|---|---|---|
| Write | Erase Suspend | Data = B0H |
| Write | Erase Status Register | Data = 70H |
| Standby/Read | | Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE# or CE# to Update Status Register |
| Standby | | Check SR.6 1 = Suspended |
| Write | Read Array | Data = FFH |
| Read | | Read array data from block other than that being erased. |
| Write | Erase Resume | Data = D0H |

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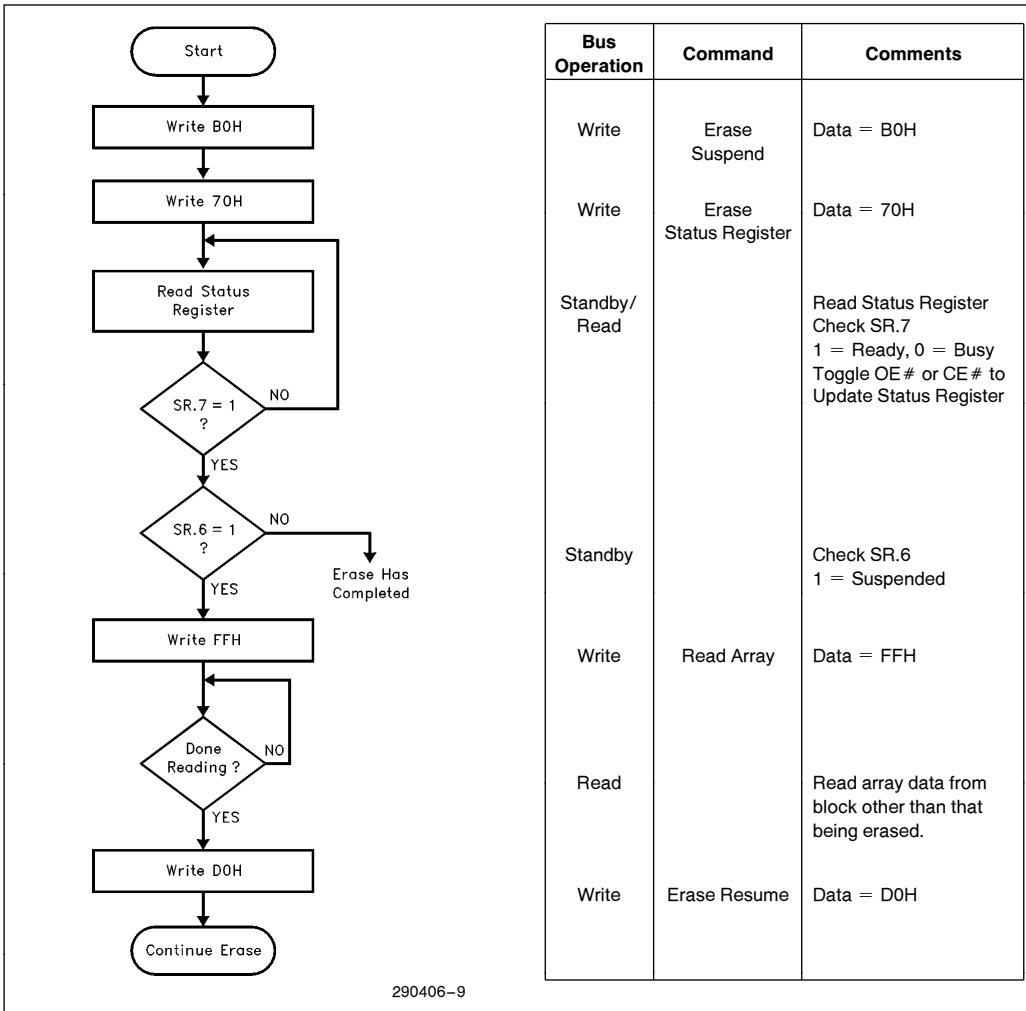**Figure 11. 28F001BX Erase Suspend/Resume Flowchart**

**Programming Equipment**

For PROM programming equipment that cannot bring RP# to high voltage, OE# provides an alternate boot block access mechanism. OE# must transition to $V_{HH}$ a minimum of 480 ns before the initial program/erase setup command and held at $V_{HH}$ at least 480 ns after program or erase confirm commands are issued to the device. After this interval, OE# can return to normal TTL levels.

## DESIGN CONSIDERATIONS

### Three-Line Output Control

Flash memories are often used in larger memory arrays. Intel provides three control inputs to accommo-date multiple memory connections. Three-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these control inputs, an address decoder should enable CE#, while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

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## Power Supply Decoupling

Flash memory power switching characteristics require careful device coupling. System designers are interested in 3 supply current issues; standby current levels ($I_{SB}$), active current levels ($I_{CC}$) and transient peaks producted by falling and rising edges of CE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 $\mu$F ceramic capacitor connected between its $V_{CC}$ and GND, and between its $V_{PP}$ and GND. These high frequency, low inherent-inductance capacitors should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 $\mu$F electrolytic capacitor should be placed at the array's power supply connection between $V_{CC}$ and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

## $V_{PP}$ Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the $V_{PP}$ power supply trace. The $V_{PP}$ pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given to the $V_{CC}$ power bus. Adequate $V_{PP}$ supply traces and decoupling will decrease $V_{PP}$ voltage spikes and overshoots.

## $V_{CC}$, $V_{PP}$, RP# Transitions and the Command/Status Registers

Programming and erase completion are not guaranteed if $V_{PP}$ drops below $V_{PPH}$. If the $V_{PP}$ Status bit of the Status Register (SR.3) is set to "1", a Clear Status Register command MUST be issued before further program/erase attempts are allowed by the WSM. Otherwise, the Program (SR.4) or Erase (SR.5) Status bits of the Status Register will be set to "1" if error is detected. RP# transitions to $V_{IL}$ during program and erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device poweroff, or RP# transitions to $V_{IL}$, clear the Status Register to initial value 80H.

The Command Register latches commands as issued by system software and is not altered by $V_{PP}$ or CE# transitions or WSM actions. Its state upon powerup, after exit from Deep-Powerdown or after $V_{CC}$ transitions below $V_{LKO}$, is FFH, or Read Array Mode.

After program or erase is complete, even after $V_{PP}$ transitions down to $V_{PPL}$, the Command Register must be reset to read array mode via the Read Array command if access to the memory array is desired.

## Power Up/Down Protection

The 28F001BX is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F001BX is indifferent as to which power supply, $V_{PP}$ or $V_{CC}$, powers up first. Power supply sequencing is not required. Internal circuitry in the 28F001BX ensures that the Command Register is reset to Read Array mode on power up.

A system designer must guard against spurious writes for $V_{CC}$ voltages above $V_{LKO}$ when $V_{PP}$ is active. Since both WE# and CE# must be low for a command write, driving either to $V_{IH}$ will inhibit writes. The Command Register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

Finally, the device is disabled, until RP# is brought to $V_{IH}$, regardless of the state of its control inputs. This provides an additional level of protection.

## 28F001BX Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases usable battery life because the 28F001BX does not consume any power to retain code or data when the system is off.

In addition, the 28F001BX's Deep-Powerdown mode ensures extremely low power dissipation even when system power is applied. For example, laptop and other PC applications, after copying BIOS to DRAM, can lower RP# to $V_{IL}$, producing negligible power consumption. If access to the boot code is again needed, as in case of a system RESET#, the part can again be accessed, following the $t_{PHAV}$ wakeup cycle required after RP# is first raised back to $V_{IH}$. The first address presented to the device while in powerdown requires time $t_{PHAV}$, after RP# transitions high, before outputs are valid. Further accesses follow normal timing. See AC Characteristics—Read-Only Operations and Figure 12 for more information.

## ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ...................0°C to 70°C[1]
During Erase/Program ...........0°C to 70°C[1]

Operating Temperature
During Read ...............−40°C to +85°C[2]
During Erase/Program ......−40°C to +85°C[2]

Temperature under Bias .........−10°C to 80°C[1]

Temperature under Bias .......−20°C to +90°C[2]

Storage Temperature.............−65°C to 125°C

Voltage on Any Pin
(except $A_9$, RP#, OE#, $V_{CC}$ and $V_{PP}$)
with Respect to GND ..........−2.0V to 7.0V[3]

Voltage on $A_9$, RP#, and OE#
with Respect to GND .......−2.0V to 13.5V[3, 4]

$V_{PP}$ Program Voltage
with Respect to GND
During Erase/Program ......−2.0V to 14.0V[3, 4]

$V_{CC}$ Supply Voltage
with Respect to GND ..........−2.0V to 7.0V[3]

Output Short Circuit Current.............100 mA[5]

> NOTICE: This is a production data sheet. The specifications are subject to change without notice.

> *WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| $T_A$ | Operating Temperature[1] | 0 | 70 | °C |
| $T_A$ | Operating Temperature[2] | −40 | 85 | °C |
| $V_{CC}$ | Supply Voltage | 4.50 | 5.50 | V |

**NOTES:**
1. Operating temperature is for commercial product defined by this specification.
2. Operating temperature is for extended temperature product defined by this specification.
3. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is $V_{CC}$ +0.5V which, during transitions, may overshoot to $V_{CC}$ + 2.0V for periods <20 ns.
4. Maximum DC voltage on $A_9$ or $V_{PP}$ may overshoot to +14.0V for periods <20 ns.
5. Output shorted for no more than one second. No more than one output shorted at a time.

## DC CHARACTERISTICS

$V_{CC}$ = 5.0V ±10%, $T_A$ = 0°C to +70°C

| Symbol | Parameter | Notes | Min | Typ | Max | Unit | Test Conditions |
|--------|-----------|-------|-----|-----|-----|------|-----------------|
| $I_{IL}$ | Input Load Current | 1 | | | ±1.0 | μA | $V_{CC}$ = $V_{CC}$ Max<br>$V_{IN}$ = $V_{CC}$ or GND |
| $I_{LO}$ | Output Leakage Current | 1 | | | ±10 | μA | $V_{CC}$ = $V_{CC}$ Max<br>$V_{OUT}$ = $V_{CC}$ or GND |
| $I_{CCS}$ | $V_{CC}$ Standby Current | | | 1.2 | 2.0 | mA | $V_{CC}$ = $V_{CC}$ Max<br>CE# = RP# = $V_{IH}$ |
| | | | | 30 | 100 | μA | $V_{CC}$ = $V_{CC}$ Max<br>CE# = RP# = $V_{CC}$ ±0.2V |
| $I_{CCD}$ | $V_{CC}$ Deep Power-Down Current | 1 | | 0.05 | 1.0 | μA | RP# = GND ±0.2V |

## DC CHARACTERISTICS (Continued)

$V_{CC} = 5.0V \pm 10\%$, $T_A = 0°C$ to $+70°C$

| Symbol | Parameter | Notes | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_{CCR}$ | $V_{CC}$ Read Current | 1 | | 13 | 30 | mA | $V_{CC} = V_{CC}$ Max, $CE\# = V_{IL}$ f = 8 MHz, $I_{OUT} = 0$ mA |
| $I_{CCP}$ | $V_{CC}$ Programming Current | 1 | | 5 | 20 | mA | Programming in Progress |
| $I_{CCE}$ | $V_{CC}$ Erase Current | 1 | | 6 | 20 | mA | Erase in Progress |
| $I_{CCES}$ | $V_{CC}$ Erase Suspend Current | 1, 2 | | 5 | 10 | mA | Erase Suspended $CE\# = V_{IH}$ |
| $I_{PPS}$ | $V_{PP}$ Standby Current | 1 | | $\pm 1$ | $\pm 10$ | $\mu A$ | $V_{PP} \leq V_{CC}$ |
| | | | | 90 | 200 | $\mu A$ | $V_{PP} > V_{CC}$ |
| $I_{PPD}$ | $V_{PP}$ Deep Power-Down Current | 1 | | 0.80 | 1.0 | $\mu A$ | $RP\# = GND \pm 0.2V$ |
| $I_{PPP}$ | $V_{PP}$ Programming Current | 1 | | 6 | 30 | mA | $V_{PP} = V_{PPH}$ Programming in Progress |
| $I_{PPE}$ | $V_{PP}$ Erase Current | 1 | | 6 | 30 | mA | $V_{PP} = V_{PPH}$ Erase in Progress |
| $I_{PPES}$ | $V_{PP}$ Erase Suspend Current | 1 | | 90 | 300 | $\mu A$ | $V_{PP} = V_{PPH}$ Erase Suspended |
| $I_{ID}$ | $A_9$ Intelligent Identifier Current | 1 | | 90 | 500 | $\mu A$ | $A_9 = V_{ID}$ |
| $V_{IL}$ | Input Low Voltage | | $-0.5$ | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC} + 0.5$ | V | |
| $V_{OL}$ | Output Low Voltage | | | | 0.45 | V | $V_{CC} = V_{CC}$ Min $I_{OL} = 5.8$ mA |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $V_{CC} = V_{CC}$ Min $I_{OH} = 2.5$ mA |
| $V_{ID}$ | $A_9$ Intelligent Identifier Voltage | | 11.5 | | 13.0 | V | |
| $V_{PPL}$ | $V_{PP}$ during Normal Operations | 3 | 0.0 | | 6.5 | V | |
| $V_{PPH}$ | $V_{PP}$ during Prog/Erase Operations | | 11.4 | 12.0 | 12.6 | V | |
| $V_{LKO}$ | $V_{CC}$ Erase/Write Lock Voltage | | 2.5 | | | V | |
| $V_{HH}$ | $RP\#$, $OE\#$ Unlock Voltage | | 11.4 | | 12.6 | V | Boot Block Prog/Erase |

**NOTES:**
1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0V$, $V_{PP} = 12.0V$, $T_A = 25°C$. These currents are valid for all product versions (packages and speeds).
2. $I_{CCES}$ is specified with the device deselected. If the 28F001BX is read while in Erase Suspend mode, current draw is the sum of $I_{CCES}$ and $I_{CCR}$.
3. Erase/Programs are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between $V_{PPH}$ and $V_{PPL}$.

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## DC CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$, $T_A = -40°C$ to $+85°C$

| Symbol | Parameter | Notes | Min | Typ | Max | Unit | Test Conditions |
|--------|-----------|-------|-----|-----|-----|------|-----------------|
| $I_{IL}$ | Input Load Current | 1 | | | ±1.0 | μA | $V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND |
| $I_{LO}$ | Output Leakage Current | 1 | | | ±10 | μA | $V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND |
| $I_{CCS}$ | $V_{CC}$ Standby Current | | | 1.2 | 2.0 | mA | $V_{CC} = V_{CC}$ Max CE# = RP# = $V_{IH}$ |
| | | | | 30 | 150 | μA | $V_{CC} = V_{CC}$ Max CE# = RP# = $V_{CC}$ ±0.2V |
| $I_{CCD}$ | $V_{CC}$ Deep Power-Down Current | 1 | | 0.05 | 2.0 | μA | RP# = GND ±0.2V |
| $I_{CCR}$ | $V_{CC}$ Read Current | 1 | | 13 | 35 | mA | $V_{CC} = V_{CC}$ Max, CE# = $V_{IL}$ f = 8 MHz, $I_{OUT} = 0$ mA |
| $I_{CCP}$ | $V_{CC}$ Programming Current | 1 | | 5 | 20 | mA | Programming in Progress |
| $I_{CCE}$ | $V_{CC}$ Erase Current | 1 | | 6 | 20 | mA | Erase in Progress |
| $I_{CCES}$ | $V_{CC}$ Erase Suspend Current | 1, 2 | | 5 | 10 | mA | Erase Suspended CE# = $V_{IH}$ |
| $I_{PPS}$ | $V_{PP}$ Standby Current | 1 | | ±1 | ±15 | μA | $V_{PP} \le V_{CC}$ |
| | | | | 90 | 400 | μA | $V_{PP} > V_{CC}$ |
| $I_{PPD}$ | $V_{PP}$ Deep Power-Down Current | 1 | | 0.80 | 1.0 | μA | RP# = GND ±0.2V |
| $I_{PPP}$ | $V_{PP}$ Programming Current | 1 | | 6 | 30 | μA | $V_{PP} = V_{PPH}$ Programming in Progress |
| $I_{PPE}$ | $V_{PP}$ Erase Current | 1 | | 6 | 30 | mA | $V_{PP} = V_{PPH}$ Erase in Progress |
| $I_{PPES}$ | $V_{PP}$ Erase Suspend Current | 1 | | 90 | 400 | μA | $V_{PP} = V_{PPH}$ Erase Suspended |
| $I_{ID}$ | $A_9$ Intelligent Identifier Current | 1 | | 90 | 500 | μA | $A_9 = V_{ID}$ |
| $V_{IL}$ | Input Low Voltage | | −0.5 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC} + 0.5$ | V | |
| $V_{OL}$ | Output Low Voltage | | | | 0.45 | V | $V_{CC} = V_{CC}$ Min $I_{OL} = 5.8$ mA |
| $V_{OH1}$ | Output High Voltage (TTL) | | 2.4 | | | V | $V_{CC} = V_{CC}$ Min $I_{OH} = 2.5$ mA |
| $V_{OH2}$ | Output High Voltage (CMOS) | | $0.85\,V_{CC}$ | | | V | $V_{CC} = V_{CC}$ Min $I_{OH} = -2.5$ μA |
| | | | $V_{CC} - 0.4$ | | | | $V_{CC} = V_{CC}$ Min $I_{OH} = -100$ μA |
| $V_{ID}$ | $A_9$ Intelligent Identifier Voltage | | 11.5 | | 13.0 | V | |
| $V_{PPL}$ | $V_{PP}$ during Normal Operations | 3 | 0.0 | | 6.5 | V | |
| $V_{PPH}$ | $V_{PP}$ during Prog/Erase Operations | | 11.4 | 12.0 | 12.6 | V | |
| $V_{LKO}$ | $V_{CC}$ Erase/Write Lock Voltage | | 2.5 | | | V | |
| $V_{HH}$ | RP#, OE# Unlock Voltage | | 11.4 | | 12.6 | V | Boot Block Prog/Erase |

**NOTES:**
1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0V$, $V_{PP} = 12.0V$, $T_A = 25°C$. These currents are valid for all product versions (packages and speeds).
2. $I_{CCES}$ is specified with the device deselected. If the 28F001BX is read while in Erase Suspend mode, current draw is the sum of $I_{CCES}$ and $I_{CCR}$.
3. Erase/Programs are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between $V_{PPH}$ and $V_{PPL}$.
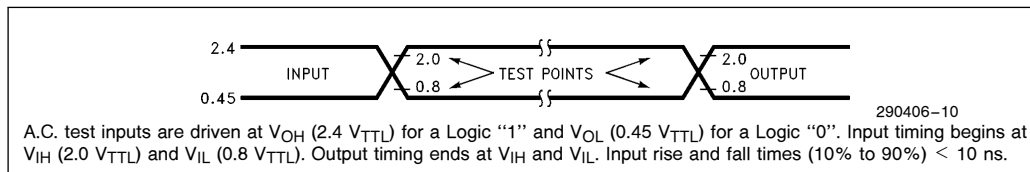
## CAPACITANCE[1] $T_A = 25°C$, $f = 1$ MHz

| Symbol | Parameter | Max | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 8 | pF | $V_{IN} = 0V$ |
| $C_{OUT}$ | Output Capacitance | 12 | pF | $V_{OUT} = 0V$ |

**NOTE:**
1. Sampled, not 100% tested.
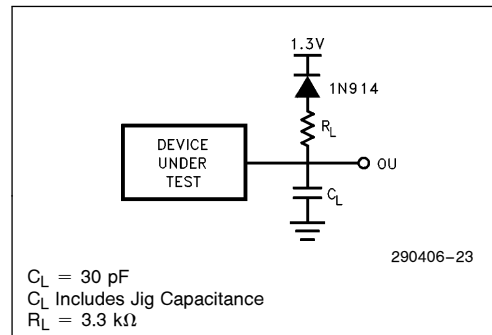
## AC INPUT/OUTPUT REFERENCE WAVEFORM
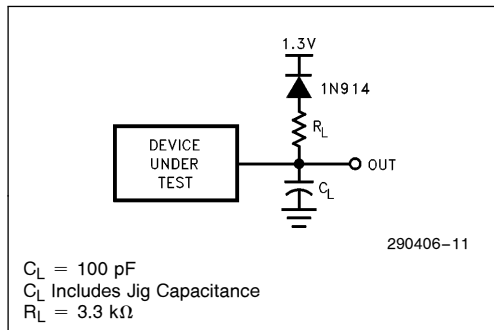


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A.C. test inputs are driven at $V_{OH}$ (2.4 $V_{TTL}$) for a Logic "1" and $V_{OL}$ (0.45 $V_{TTL}$) for a Logic "0". Input timing begins at $V_{IH}$ (2.0 $V_{TTL}$) and $V_{IL}$ (0.8 $V_{TTL}$). Output timing ends at $V_{IH}$ and $V_{IL}$. Input rise and fall times (10% to 90%) < 10 ns.

## STANDARD TEST CONFIGURATION AC TESTING LOAD CIRCUIT



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$C_L = 100$ pF
$C_L$ Includes Jig Capacitance
$R_L = 3.3$ k$\Omega$

## HIGH SPEED TEST CONFIGURATION AC TESTING LOAD CIRCUIT



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$C_L = 30$ pF
$C_L$ Includes Jig Capacitance
$R_L = 3.3$ k$\Omega$

## AC CHARACTERISTICS—Read-Only Operations[1]

| Symbol | | Parameter | Notes | 28F001BX-70 | | | | 28F001BX-90 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC} = 5V$ $\pm 5\%$ 30 pF | | $V_{CC} = 5V$ $\pm 10\%$ 100 pF | | $V_{CC} = 5V$ $\pm 10\%$ 100 pF | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | 70 | | 75 | | 90 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | | | 70 | | 75 | | 90 | ns |
| $t_{ELQV}$ | $t_{CE}$ | CE# to Output Delay | 2 | | 70 | | 75 | | 90 | ns |
| $t_{PHQV}$ | $t_{PWH}$ | RP# to Output Delay | | | 600 | | 600 | | 600 | ns |
| $t_{GLQV}$ | $t_{OE}$ | OE# to Output Delay | 2 | | 27 | | 30 | | 35 | ns |
| $t_{ELQX}$ | $t_{LZ}$ | CE# to Output in Low Z | 3 | 0 | | 0 | | 0 | | ns |
| $t_{EHQZ}$ | $t_{HZ}$ | CE# to Output in High Z | 3 | | 55 | | 55 | | 35 | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | OE# to Output in Low Z | 3 | 0 | | 0 | | 0 | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | OE# to Output in High Z | 3 | | 30 | | 30 | | 30 | ns |
| | $t_{OH}$ | Output Hold from Address CE#, or OE# Change, Whichever Occurs First | 3 | 0 | | 0 | | 0 | | ns |

**NOTES:**
1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of CE# without impact on $t_{CE}$.
3. Sampled, but not 100% tested.
4. See High Speed Test Configuration.
5. See Standard Test Configuration.

## AC CHARACTERISTICS—Read-Only Operations[1]

| Versions[2] | | | $V_{CC} \pm 10\%$ | E28F001BX-120<br>N28F001BX-120<br>P28F001BX-120 | | E28F001BX-150<br>TE28F001BX-150<br>N28F001BX-150<br>TN28F001BX-150<br>P28F001BX-150 | | Unit |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | | **Parameter** | **Notes** | **Min** | **Max** | **Min** | **Max** | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | 120 | | 150 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | | | 120 | | 150 | ns |
| $t_{ELQV}$ | $t_{CE}$ | CE# to Output Delay | 3 | | 120 | | 150 | ns |
| $t_{PHQV}$ | $t_{PWH}$ | RP# High to Output Delay | | | 600 | | 600 | ns |
| $t_{GLQV}$ | $t_{OE}$ | OE# to Output Delay | 3 | | 50 | | 55 | ns |
| $t_{ELQX}$ | $t_{LZ}$ | CE# to Output Low Z | 4 | 0 | | 0 | | ns |
| $t_{EHQZ}$ | $t_{HZ}$ | CE# High to Output High Z | 4 | | 55 | | 55 | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | OE# to Output Low Z | 4 | 0 | | 0 | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | OE# High to Output High Z | 4 | | 30 | | 30 | ns |
| | $t_{OH}$ | Output Hold from Addresses, CE# or OE# Change, Whichever is First | 4 | 0 | | 0 | | ns |

**NOTES:**
1. See AC Input/Output Reference Waveform for timing measurements.
2. Model Number Prefixes: E = TSOP (Standard Pinout), N = PLCC, P = PDIP, T = Extended Temperature. Refer to standard test configuration.
3. OE# may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of CE# without impact on $t_{CE}$.
4. Sampled, not 100% tested.
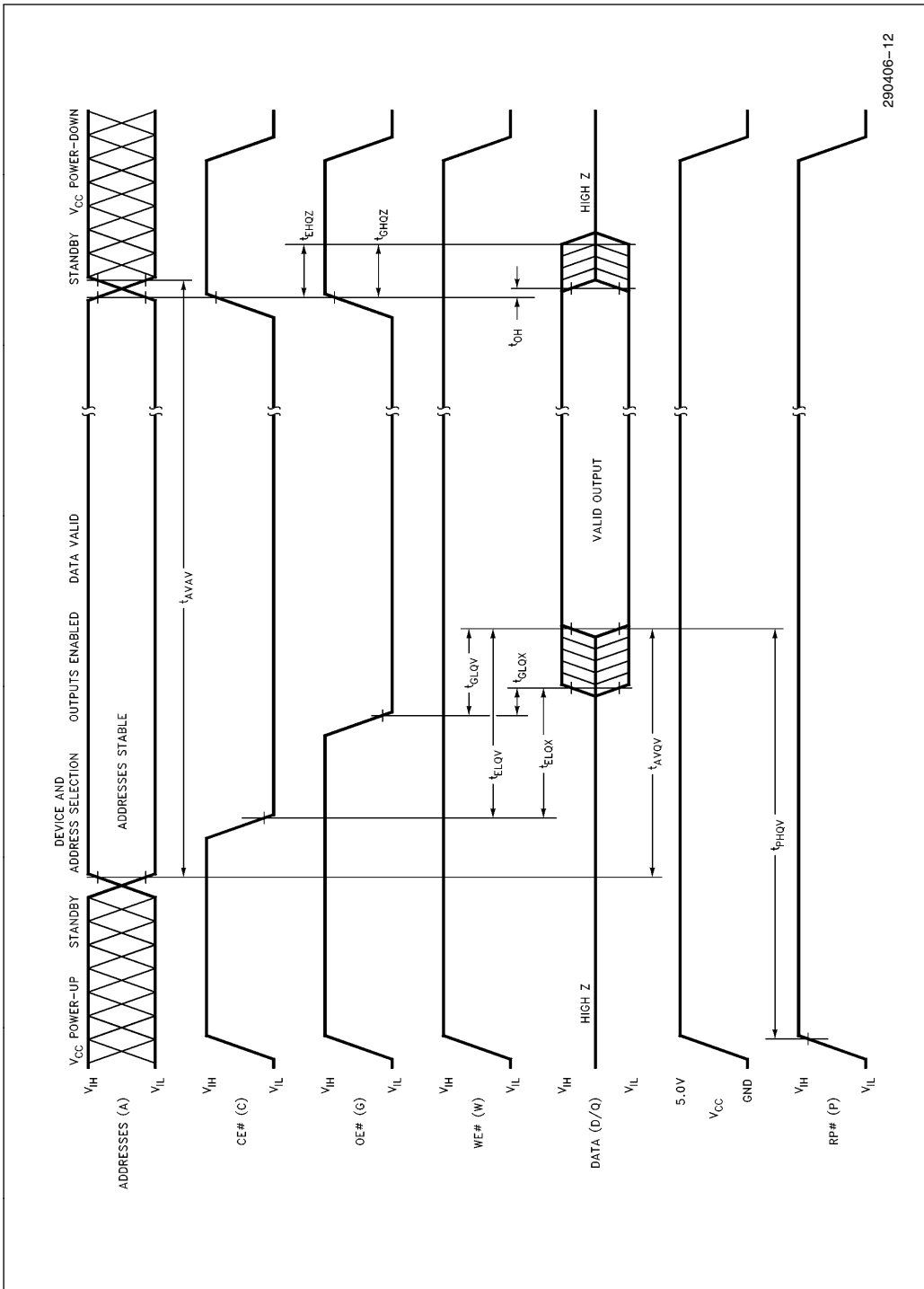
**Figure 12. AC Waveform for Read Operations**

## AC CHARACTERISTICS—Write/Erase/Program Operations[1, 9]

| Symbol | | Parameter | Notes | 28F001BX-70 $V_{CC}$ = 5V ±5%[10] 30 pF | | $V_{CC}$ = 5V ±10%[11] 100 pF | | 28F001BX-90 $V_{CC}$ = 5V ±10%[11] 100 pF | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | 70 | | 75 | | 90 | | ns |
| $t_{PHWL}$ | $t_{PS}$ | RP# High Recovery to WE# Going Low | 2 | 480 | | 480 | | 480 | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup to WE# Going Low | | 10 | | 10 | | 10 | | ns |
| $t_{WLWH}$ | $t_{WP}$ | WE# Pulse Width | | 35 | | 40 | | 40 | | ns |
| $t_{PHHWH}$ | $t_{PHS}$ | RP# $V_{HH}$ Setup to WE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| $t_{VPWH}$ | $t_{VPS}$ | $V_{PP}$ Setup to WE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| $t_{AVWH}$ | $t_{AS}$ | Address Setup to WE# Going High | 3 | 35 | | 40 | | 40 | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup to WE# Going High | 4 | 35 | | 40 | | 40 | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold from WE# High | | 10 | | 10 | | 10 | | ns |
| $t_{WHAX}$ | $t_{AH}$ | Address Hold from WE# High | | 10 | | 10 | | 10 | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold from WE# High | | 10 | | 10 | | 10 | | ns |
| $t_{WHWL}$ | $t_{WPH}$ | WE# Pulse Width High | | 35 | | 35 | | 35 | | ns |
| $t_{WHQV1}$ | | Duration of Programming Operation | 5, 6, 7 | 15 | | 15 | | 15 | | $\mu$s |
| $t_{WHQV2}$ | | Duration of Erase Operation (Boot) | 5, 6, 7 | 1.3 | | 1.3 | | 1.3 | | sec |
| $t_{WHQV3}$ | | Duration of Erase Operation (Parameter) | 5, 6, 7 | 1.3 | | 1.3 | | 1.3 | | sec |
| $t_{WHQV4}$ | | Duration of Erase Operation (Main) | 5, 6, 7 | 3.0 | | 3.0 | | 3.0 | | sec |
| $t_{WHGL}$ | | Write Recovery before Read | | 0 | | 0 | | 0 | | $\mu$s |
| $t_{QVVL}$ | $t_{VPH}$ | $V_{PP}$ Hold from Valid SRD | 2, 6 | 0 | | 0 | | 0 | | ns |
| $t_{QVPH}$ | $t_{PHH}$ | RP# $V_{HH}$ Hold from Valid SRD | 2, 7 | 0 | | 0 | | 0 | | ns |
| $t_{PHBR}$ | | Boot-Block Relock Delay | 2 | | 100 | | 100 | | 100 | ns |

**NOTES:**
1. Read timing characteristics during erase and program operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid $A_{IN}$ for byte programming or block erasure.
4. Refer to Table 3 for valid $D_{IN}$ for byte programming or block erasure.
5. The on-chip Write State Machine incorporates all program and erase system functions and overhead of standard Intel Flash Memory, including byte program and verify (programming) and block precondition, precondition verify, erase and erase verify (erasing).
6. Program and erase durations are measured to completion (SR.7 = 1). $V_{PP}$ should be held at $V_{PPH}$ until determination of program/erase success (SR.3/4/5 = 0).
7. For boot block programming and erasure, RP# should be held at $V_{HH}$ until determination of program/erase success (SR.3/4/5 = 0).
8. Alternate boot block access method.
9. Erase/Program Cycles on extended temperature products is 10,000 cycles.
10. See high speed test configuration.
11. See standard test configuration.

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## AC CHARACTERISTICS—Write/Erase/Program Operations[1, 9]

| Versions | | Parameter | $V_{CC} \pm 10\%$ [10] | 28F001BX-120 | | 28F001BX-150 | | Unit |
|---|---|---|---|---|---|---|---|---|
| Symbol | | Parameter | Notes | Min | Max | Min | Max | Unit |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | 120 | | 150 | | ns |
| $t_{PHWL}$ | $t_{PS}$ | RP# High Recovery to WE# Going Low | 2 | 480 | | 480 | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup to WE# Going Low | | 10 | | 10 | | ns |
| $t_{WLWH}$ | $t_{WP}$ | WE# Pulse Width | | 50 | | 50 | | ns |
| $t_{PHHWH}$ | $t_{PHS}$ | RP# $V_{HH}$ Setup to WE# Going High | 2 | 100 | | 100 | | ns |
| $t_{VPWH}$ | $t_{VPS}$ | $V_{PP}$ Setup to WE# Going High | 2 | 100 | | 100 | | ns |
| $t_{AVWH}$ | $t_{AS}$ | Address Setup to WE# Going High | 3 | 50 | | 50 | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup to WE# Going High | 4 | 50 | | 50 | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold from WE# High | | 10 | | 10 | | ns |
| $t_{WHAX}$ | $t_{AH}$ | Address Hold from WE# High | | 10 | | 10 | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold from WE# High | | 10 | | 10 | | ns |
| $t_{WHWL}$ | $t_{WPH}$ | WE# Pulse Width High | | 50 | | 50 | | ns |
| $t_{WHQV1}$ | | Duration of Programming Operation | 5, 6, 7 | 15 | | 15 | | $\mu s$ |
| $t_{WHQV2}$ | | Duration of Erase Operation (Boot) | 5, 6, 7 | 1.3 | | 1.3 | | sec |
| $t_{WHQV3}$ | | Duration of Erase Operation (Parameter) | 5, 6, 7 | 1.3 | | 1.3 | | sec |
| $t_{WHQV4}$ | | Duration of Erase Operation (Main) | 5, 6, 7 | 3.0 | | 3.0 | | sec |
| $t_{WHGL}$ | | Write Recovery before Read | | 0 | | 0 | | $\mu s$ |
| $t_{QVVL}$ | $t_{VPH}$ | $V_{PP}$ Hold from Valid SRD | 2, 6 | 0 | | 0 | | ns |
| $t_{QVPH}$ | $t_{PHH}$ | RP# $V_{HH}$ Hold from Valid SRD | 2, 7 | 0 | | 0 | | ns |
| $t_{PHBR}$ | | Boot-Block Relock Delay | 2 | | 100 | | 100 | ns |

### PROM Programmer Specifications

| Versions | | Parameter | $V_{CC} \pm 10\%$ | 28F001BX-120 | | 28F001BX-150 | | Unit |
|---|---|---|---|---|---|---|---|---|
| Symbol | | Parameter | Notes | Min | Max | Min | Max | Unit |
| $t_{GHHWL}$ | | OE# $V_{HH}$ Setup to WE# Going Low | 2, 8 | 480 | | 480 | | ns |
| $t_{WHGH}$ | | OE# $V_{HH}$ Hold from WE# High | 2, 8 | 480 | | 480 | | ns |

**NOTES:**
1. Read timing characteristics during erase and program operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid $A_{IN}$ for byte programming or block erasure.
4. Refer to Table 3 for valid $D_{IN}$ for byte programming or block erasure.
5. The on-chip Write State Machine incorporates all program and erase system functions and overhead of standard Intel Flash Memory, including byte program and verify (programming) and block precondition, precondition verify, erase and erase verify (erasing).
6. Program and erase durations are measured to completion (SR.7 = 1). $V_{PP}$ should be held at $V_{PPH}$ until determination of program/erase success (SR.3/4/5 = 0).
7. For boot block programming and erasure, RP# should be held at $V_{HH}$ until determination of program/erase success (SR.3/4/5 = 0).
8. Alternate boot block access method.
9. Erase/Program Cycles on extended temperature products is 10,000 cycles.
10. See standard test configuration.

## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Notes | 28F001BX-120 | | | 28F001BX-150 | | | Unit |
|-----------|-------|-----|--------|-----|-----|--------|-----|------|
|  |  | Min | Typ[1] | Max | Min | Typ[1] | Max |  |
| Boot Block Erase Time | 2 |  | 2.10 | 14.9 |  | 2.10 | 14.9 | Sec |
| Boot Block Program Time | 2 |  | 0.15 | 0.52 |  | 0.15 | 0.52 | Sec |
| Parameter Block Erase Time | 2 |  | 2.10 | 14.6 |  | 2.10 | 14.6 | Sec |
| Parameter Block Program Time | 2 |  | 0.07 | 0.26 |  | 0.07 | 0.26 | Sec |
| Main Block Erase Time | 2 |  | 3.80 | 20.9 |  | 3.80 | 20.9 | Sec |
| Main Block Program Time | 2 |  | 2.10 | 7.34 |  | 2.10 | 7.34 | Sec |
| Chip Erase Time | 2 |  | 10.10 | 65 |  | 10.10 | 65 | Sec |
| Chip Program Time | 2 |  | 2.39 | 8.38 |  | 2.39 | 8.38 | Sec |

**NOTES:**
1. 25°C, 12.0 $V_{PP}$.
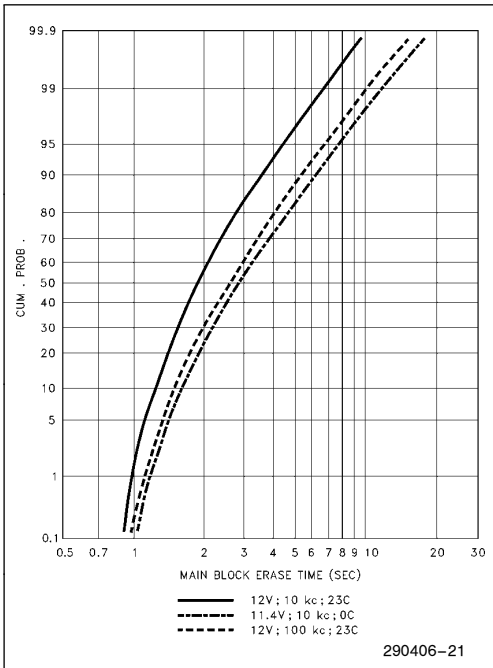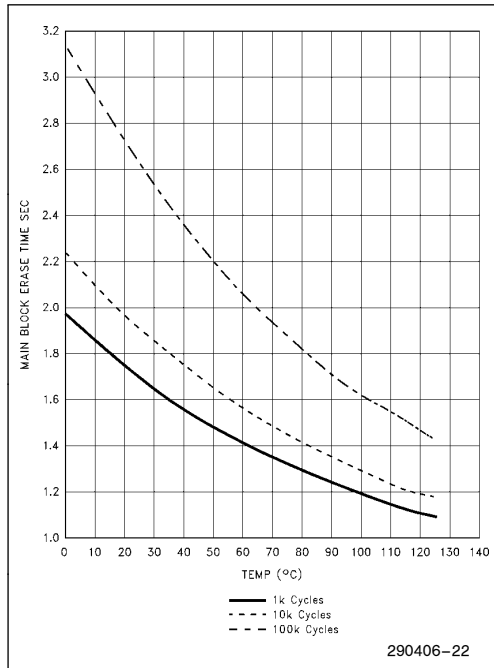2. Excludes System-Level Overhead.

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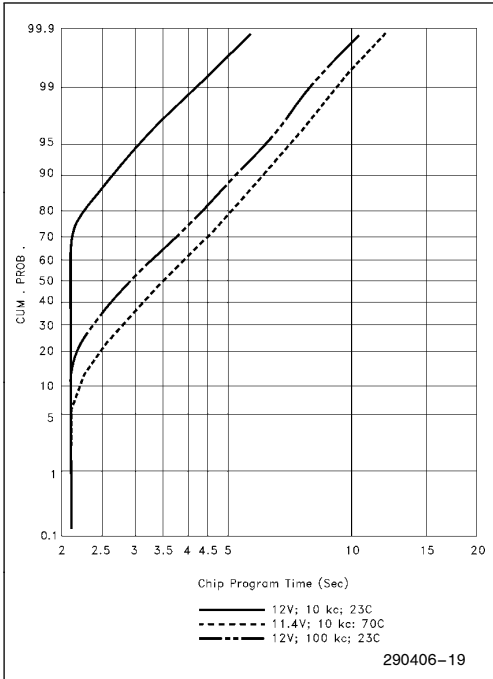


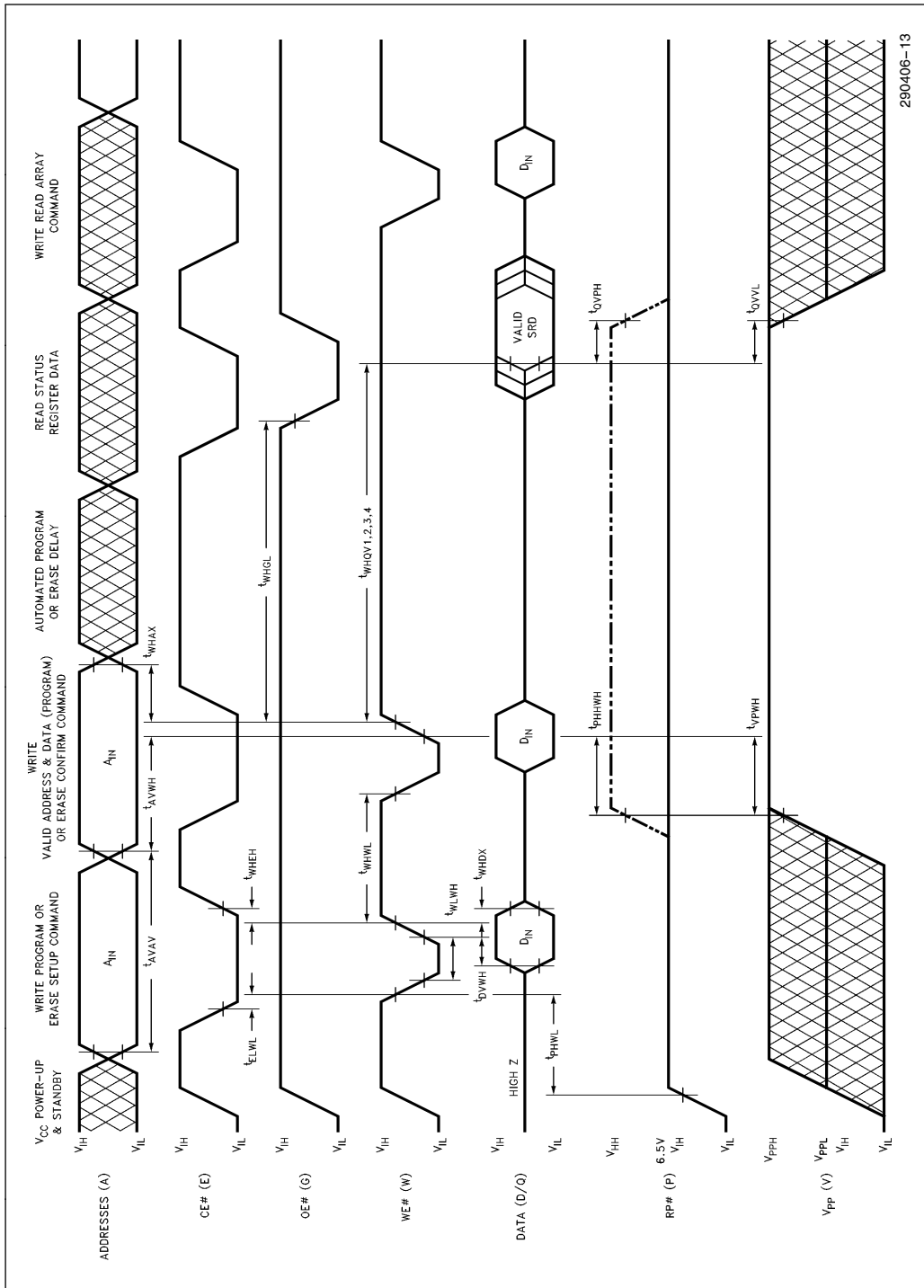**Figure 13. 28F001BX Typical
Programming Capability**
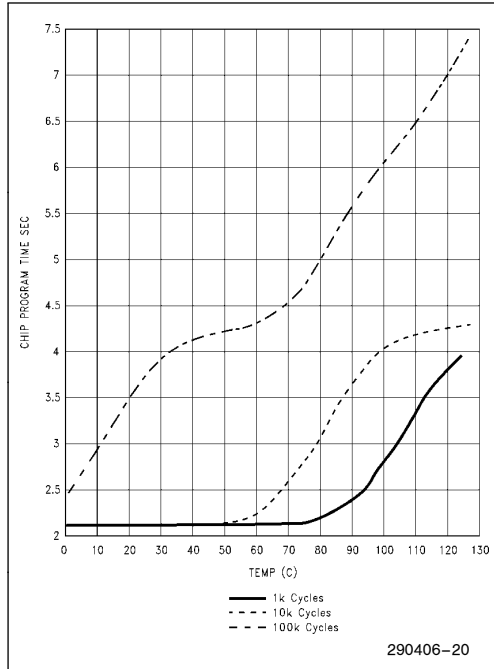


**Figure 14. 28F001BX Typical
Programming Time at 12V**



**Figure 15. 28F001BX Typical Erase Capability**



**Figure 16. 28F001BX Typical Erase Time at 12V**

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**Figure 17. AC Waveform for Write Operations**
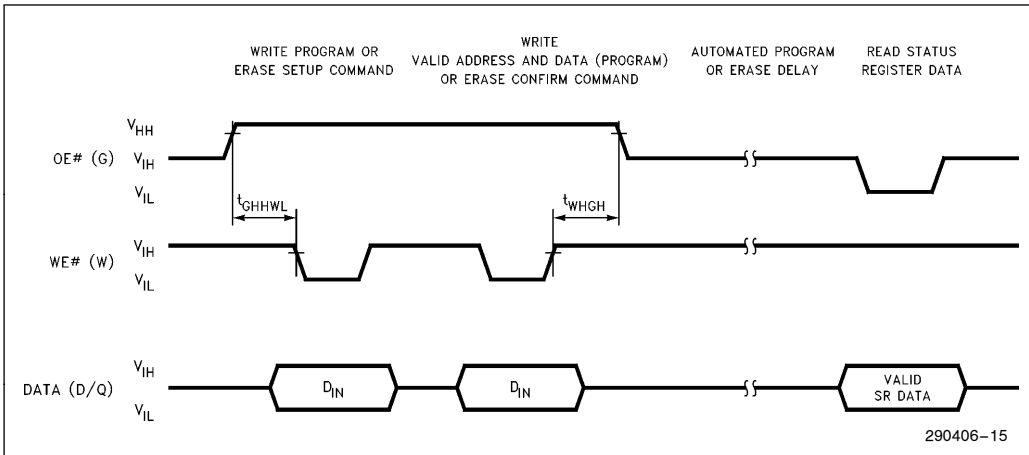
27

Figure 18. Alternate Boot Block Access Method Using OE #

## AC CHARACTERISTICS FOR CE#-CONTROLLED WRITES[1]

| Symbol | | Parameter | Notes | 28F001BX-70 | | | | 28F001BX-90 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC} = 5V$ $\pm 5\%$[8] 30 pF | | $V_{CC} = 5V$ $\pm 10\%$[9] 100 pF | | $V_{CC} = 5V$ $\pm 10\%$[9] 100 pF | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | 70 | | 75 | | 90 | | ns |
| $t_{PHEL}$ | $t_{PS}$ | RP# High Recovery to CE# Going Low | 2 | 480 | | 480 | | 480 | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup to CE# Going Low | | 0 | | 0 | | 0 | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | 50 | | 55 | | 55 | | ns |
| $t_{PHHEH}$ | $t_{PHS}$ | RP# $V_{HH}$ Setup to CE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| $t_{VPEH}$ | $t_{VPS}$ | $V_{PP}$ Setup to CE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| $t_{AVEH}$ | $t_{AS}$ | Address Setup to CE# Going High | 3 | 35 | | 40 | | 40 | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup to CE# Going High | 4 | 35 | | 40 | | 40 | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold from CE# High | | 10 | | 10 | | 10 | | ns |
| $t_{EHAX}$ | $t_{AH}$ | Address Hold from CE# High | | 10 | | 10 | | 10 | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold from CE# High | | 0 | | 0 | | 0 | | ns |
| $t_{EHEL}$ | $t_{EPH}$ | CE# Pulse Width High | | 20 | | 20 | | 20 | | ns |
| $t_{EHQV1}$ | | Duration of Programming Operation | 5, 6 | 15 | | 15 | | 15 | | $\mu$s |
| $t_{EHQV2}$ | | Duration of Erase Operation (Boot) | 5, 6 | 1.3 | | 1.3 | | 1.3 | | sec |
| $t_{EHQV3}$ | | Duration of Erase Operation (Parameter) | 5, 6 | 1.3 | | 1.3 | | 1.3 | | sec |
| $t_{EHQV4}$ | | Duration of Erase Operation (Main) | 5, 6 | 3.0 | | 3.0 | | 3.0 | | sec |
| $t_{EHGL}$ | | Write Recovery before Read | | 0 | | 0 | | 0 | | $\mu$s |
| $t_{QVVL}$ | $t_{VPH}$ | $V_{PP}$ Hold from Valid SRD | 2, 5 | 0 | | 0 | | 0 | | ns |
| $t_{QVPH}$ | $t_{PHH}$ | RP# $V_{HH}$ Hold from Valid SRD | 2, 6 | 0 | | 0 | | 0 | | ns |
| $t_{PHBR}$ | | Boot-Block Relock Delay | 2 | | 100 | | 100 | | 100 | ns |

**NOTES:**
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of CE# and WE#. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid $A_{IN}$ for byte programming or block erasure.
4. Refer to Table 3 for valid $D_{IN}$ for byte programming or block erasure.
5. Program and erase durations are measured to completion (SR.7 = 1). $V_{PP}$ should be held at $V_{PPH}$ until determination of program/erase success (SR.3/4/5 = 0).
6. For boot block programming and erasure, RP# should be held at $V_{HH}$ until determination of program/erase success (SR.3/4/5 = 0).
7. Alternate boot block access method.
8. See high speed test configuration.
9. See standard text configuration.

## AC CHARACTERISTICS FOR CE#-CONTROLLED WRITES[1]

| Versions | | | $V_{CC} \pm 10\%$ | 28F001BX-120 | | 28F001BX-150 | | Unit |
|---|---|---|---|---|---|---|---|---|
| Symbol | | Parameter | Notes | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | 120 | | 150 | | ns |
| $t_{PHEL}$ | $t_{PS}$ | RP# High Recovery to CE# Going Low | 2 | 480 | | 480 | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup to CE# Going Low | | 0 | | 0 | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | 70 | | 70 | | ns |
| $t_{PHHEH}$ | $t_{PHS}$ | RP# $V_{HH}$ Setup to CE# Going High | 2 | 100 | | 100 | | ns |
| $t_{VPEH}$ | $t_{VPS}$ | $V_{PP}$ Setup to CE# Going High | 2 | 100 | | 100 | | ns |
| $t_{AVEH}$ | $t_{AS}$ | Address Setup to CE# Going High | 3 | 50 | | 50 | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup to CE# Going High | 4 | 50 | | 50 | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold from CE# High | | 10 | | 10 | | ns |
| $t_{EHAX}$ | $t_{AH}$ | Address Hold from CE# High | | 15 | | 15 | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold from CE# High | | 0 | | 0 | | ns |
| $t_{EHEL}$ | $t_{EPH}$ | CE# Pulse Width High | | 25 | | 25 | | ns |
| $t_{EHQV1}$ | | Duration of Programming Operation | 5, 6 | 15 | | 15 | | $\mu$s |
| $t_{EHQV2}$ | | Duration of Erase Operation (Boot) | 5, 6 | 1.3 | | 1.3 | | sec |
| $t_{EHQV3}$ | | Duration of Erase Operation (Parameter) | 5, 6 | 1.3 | | 1.3 | | sec |
| $t_{EHQV4}$ | | Duration of Erase Operation (Main) | 5, 6 | 3.0 | | 3.0 | | sec |
| $t_{EHGL}$ | | Write Recovery before Read | | 0 | | 0 | | $\mu$s |
| $t_{QVVL}$ | $t_{VPH}$ | $V_{PP}$ Hold from Valid SRD | 2, 5 | 0 | | 0 | | ns |
| $t_{QVPH}$ | $t_{PHH}$ | RP# $V_{HH}$ Hold from Valid SRD | 2, 6 | 0 | | 0 | | ns |
| $t_{PHBR}$ | | Boot-Block Relock Delay | 2 | | 100 | | 100 | ns |

## PROM Programmer Specifications

| Versions | | $V_{CC} \pm 10\%$ | 28F001BX-120 | | 28F001BX-150 | | Unit |
|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Notes | Min | Max | Min | Max | |
| $t_{GHHEL}$ | OE# $V_{HH}$ Setup to CE# Going Low | 2, 7 | 480 | | 480 | | ns |
| $t_{EHGH}$ | OE# $V_{HH}$ Hold from CE# High | 2, 7 | 480 | | 480 | | ns |

**NOTES:**
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of CE# and WE#. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid $A_{IN}$ for byte programming or block erasure.
4. Refer to Table 3 for valid $D_{IN}$ for byte programming or block erasure.
5. Program and erase durations are measured to completion (SR.7 = 1). $V_{PP}$ should be held at $V_{PPH}$ until determination of program/erase success (SR.3/4/5 = 0).
6. For boot block programming and erasure, RP# should be held at $V_{HH}$ until determination of program/erase success (SR.3/4/5 = 0).
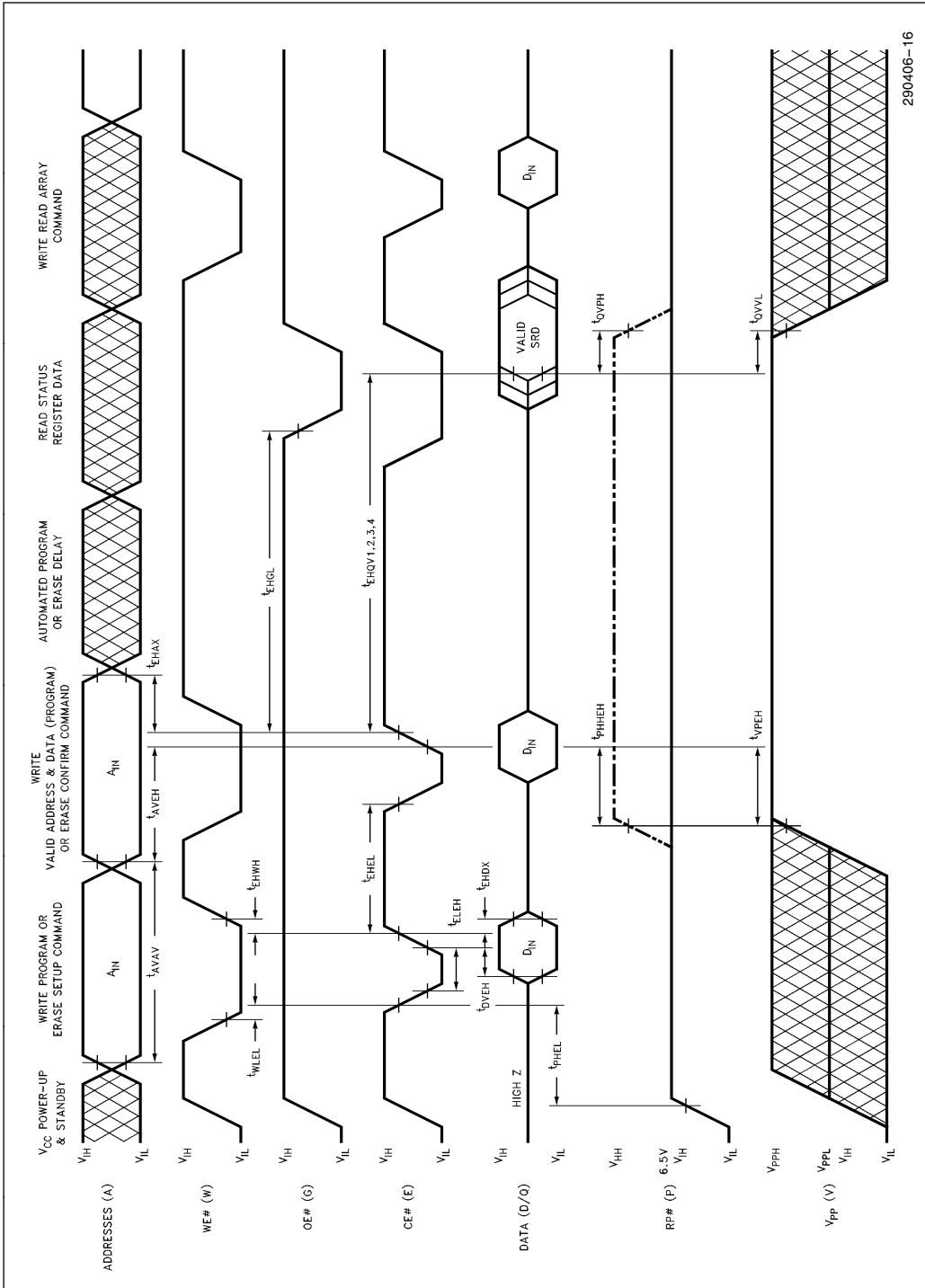7. Alternate boot block access method.

**Figure 19. Alternate AC Waveform for Write Operations**

## ORDERING INFORMATION

```
┌─┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┬─┐
│T│P│2│8│F│0│0│1│B│X│─│T│1│2│0│
└─┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┴─┘
```

ACCESS SPEED (ns)
70 ns
90 ns
120 ns
150 ns

PACKAGE
E  STANDARD 32 LEAD TSOP
N  32 LEAD PLCC
P  32-PIN PLASTIC DIP

TEMPERATURE RANGE
T = EXTENDED (−40°C to +85°C)
BLANK = COMMERCIAL (0°C to +70°C)

T  TOP BOOT DEVICE
B  BOTTOM BOOT DEVICE

290406−18

**VALID COMBINATIONS:**

|  | 32-Lead TSOP | 32-Lead PLCC | 32-Pin PDIP |
|---|---|---|---|
| **Commercial** | E28F001BX-T70 | N28F001BX-T70 | P28F001BX-T70 |
|  | E28F001BX-T90 | N28F001BX-T90 | P28F001BX-T90 |
|  | E28F001BX-T120 | N28F001BX-T120 | P28F001BX-T120 |
|  | E28F001BX-T150 | N28F001BX-T150 | P28F001BX-T150 |
|  |  |  |  |
|  | E28F001BX-B70 | N28F001BX-B70 | P28F001BX-B70 |
|  | E28F001BX-B90 | N28F001BX-B90 | P28F001BX-B90 |
|  | E28F001BX-B120 | N28F001BX-B120 | P28F001BX-B120 |
|  | E28F001BX-B150 | N28F001BX-B150 | P28F001BX-B150 |
|  |  |  |  |
| **Extended** | TE28F001BX-T90 | TN28F001BX-T90 | TP28F001BX-T90 |
|  | TE28F001BX-T150 | TN28F001BX-T150 | TP28F001BX-B90 |
|  |  |  |  |
|  | TE28F001BX-B90 | TN28F001BX-B90 |  |
|  | TE28F001BX-B150 | TN28F001BX-B150 |  |

## ADDITIONAL INFORMATION

### References

| Order Number | Document |
|---|---|
| 292046 | AP-316  ''Using Flash Memory for In-System Reprogrammable Nonvolatile Storage'' |
| 292077 | AP-341  ''Designing an Updateable BIOS Using Flash Memory'' |
| 292161 | AP-608  ''Implementing a Plug and Play BIOS Using Intel's Boot Block Flash Memory'' |
| 292178 | AP-623  ''Multi-Site Layout Planning Using Intel's Boot Block Flash Memory'' |
| 294005 | ER-20  ''ETOX II Flash Memory Technology'' |

## Revision History

| Number | Description |
|--------|-------------|
| -004 | Removed **Preliminary** classification. |
| | Latched address $A_{16}$ in Figure 5. |
| | Updated Boot Block Program and Erase section: "If boot block program or erase is attempted while RP# is at $V_{IH}$, **either the Program Status or Erase Status bit will be set to "1", reflective of the operation being attempted and indicating boot block lock."** |
| | Updated Figure 11, 28F001BX Erase Suspend/Resume Flowchart |
| | Added DC Characteristics typical current values |
| | Combined $V_{PP}$ Standby current and $V_{PP}$ Read current into one $V_{PP}$ Standby current spec with two test conditions (DC Characteristics table) |
| | Added maximum program/erase times to Erase and Programming Performance table. |
| | Added Figures 13–16 |
| | Added Extended Temperature proliferations |
| -005 | $\overline{PWD}$ changed to RP# for JEDEC standardization compatibility |
| | Revised symbols, i.e.; $\overline{CE}$, $\overline{OE}$, etc. to CE#, OE#, etc. |
| -006 | Added specifications for -90 and -70 product versions. |
| | Added $V_{OH}$ CMOS Specification. |
| -007 | Added reference to 28F001BN. |