	QUADRUPLE DIFFERENTIAL LINE RECEIV WITH 3-STATE OUTPU SLLS097C – JUNE 1980 – REVISED FEBRUARY 2
<ul> <li>Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-422 B and ITH Becommendations</li> </ul>	D, N, OR NS PACKAGE (TOP VIEW)
EIA/TIA-423-B and ITU Recommendations V.10 and V.11	
• 3-State, TTL-Compatible Outputs	1A [] 2   15 [] 4B 1Y [] 3   14 [] 4A
Fast Transition Times	1,2EN [ 4 13 ] 4Y
<ul> <li>Operates From Single 5-V Supply</li> <li>Designed to Be Interchangeable With</li> </ul>	2Y [] 5 12 [] 3,4EN 2A [] 6 11 [] 3Y
Motorola™ MC3486	2B 🗍 7 10 🗍 3A
locarintian	GND [ 8 9] 3B

#### description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B and ITU Recommendations V.10 and V.11. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

The MC3486 is characterized for operation from 0°C to 70°C.

AVAILABLE OF HONS						
	PACKAGED DEVICES					
TA	PLASTIC SMALL OUTLINE (D, NS)	PLASTIC DIP (N)				
0°C to 70°C	MC3486D MC3486NS	MC3486N				

AVAILABLE OPTIONS

The D package is available taped and reeled. Add the suffix R to the device type (e.g., MC3486DR). The NS package is only available taped and reeled.



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MC3486

2002

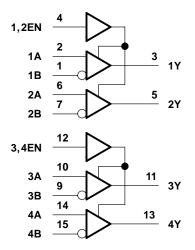
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#### **FUNCTION TABLE** (oach rocoivor)

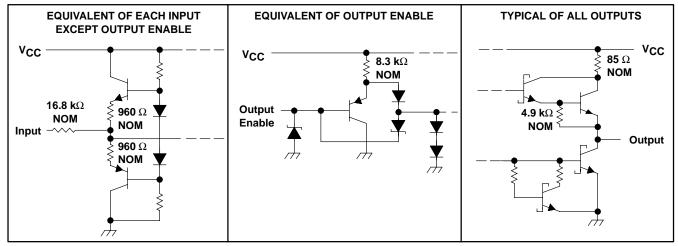
(each receiver)							
DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y					
$V_{ID} \le 0.2 V$	Н	Н					
$-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$	н	?					
$V_{ID} \leq -0.2 V$	н	L					
Irrelevant	L	Z					
Open	Н	?					

H = high level, L = low level, Z = high impedance (off),? = indeterminate

### logic diagram (positive logic)



### schematics of inputs and outputs





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub> (see Note 1)	8 V
Input voltage, V <sub>I</sub> (A or B inputs)	±15 V
Differential input voltage, VID (see Note 2)	±25 V
Enable input voltage	
Low-level output current, I <sub>OI</sub>	50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
N package	67°C/W
NS package	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.

2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.75	5	5.25	V
VIC	Common-mode input voltage			±7	V
VID	Differential input voltage			±6	V
VIH	High-level enable input voltage	2			V
VIL	Low-level enable input voltage			0.8	V
Т <sub>А</sub>	Operating free-air temperature	0		70	°C



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#### electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITION	S	MIN	MAX	UNIT
VIT+	Differential input high-threshold voltage	$V_{O} = 2.7 V$ , $I_{O} = -0.4 mA$			0.2	V
$V_{IT-}$	Differential input low-threshold voltage	$V_{O} = 0.5 V$ , $I_{O} = -8 mA$		-0.2†		V
VIK	Enable-input clamp voltage	I <sub>I</sub> = -10 mA			-1.5	V
Vон	High-level output voltage	$V_{ID} = 0.4 V$ , $I_O = -0.4 mA$ , See Note 4 and Figure 1		2.7		V
V <sub>OL</sub>	Low-level output voltage	$V_{ID} = -0.4 V$ , $I_O = 8 mA$ , See Note 4 and Figure 1			0.5	V
1	High impodence state output ourrest	$V_{IL} = 0.8 V$ , $V_{ID} = -3 V$ ,	V <sub>O</sub> = 2.7 V		40	
loz	High-impedance-state output current	$V_{IL} = 0.8 V$ , $V_{ID} = 3 V$ ,	V <sub>O</sub> = 0.5 V		-40 µA	μA
			$V_{I} = -10 V$		-3.25	mA
		V <sub>CC</sub> = 0 V or 5.25 V,	$V_{I} = -3 V$		-1.5	
IВ	Differential-input bias current	Other inputs at 0 V	V <sub>I</sub> = 3 V		1.5	
			V <sub>I</sub> = 10 V		3.25	
IIH High-level enable input current		VI = 5.25 V			100	A
		VI = 2.7 V			20	μA
۱ <sub>۱L</sub>	Low-level enable input current	$V_{I} = -0.5 V$			-100	μA
los	Short-circuit output current	$V_{\text{ID}} = 3 \text{ V}, \qquad \qquad V_{\text{O}} = 0,$	See Note 5	-15	-100	mA
ICC	Supply current	$V_{IL} = 0$			85	mA

<sup>†</sup> The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 4. Refer to ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.

5. Only one output should be shorted at a time.

### switching characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 15 pF, T<sub>A</sub> = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<sup>t</sup> PHL	Propagation delay time, high- to low-level output	See Figure 2		28	35	ns
<sup>t</sup> PLH	Propagation delay time, low- to high-level output	See Figure 2		27	30	ns
<sup>t</sup> PZH	Output enable time to high level			13	30	ns
<sup>t</sup> PZL	Output enable time to low level	Soo Eiguro 2		20	30	ns
<sup>t</sup> PHZ	Output disable time from high level	See Figure 3		26	35	ns
<sup>t</sup> PLZ	Output disable time from low level			27	35	ns



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#### PARAMETER MEASUREMENT INFORMATION

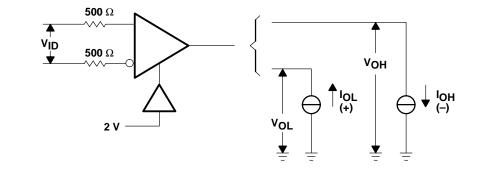
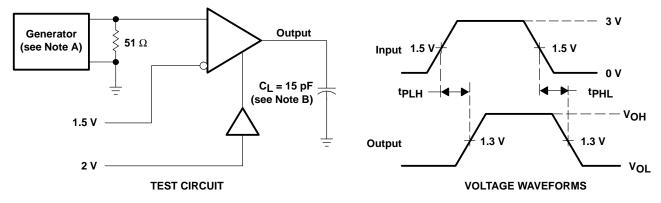


Figure 1. VOH, VOL

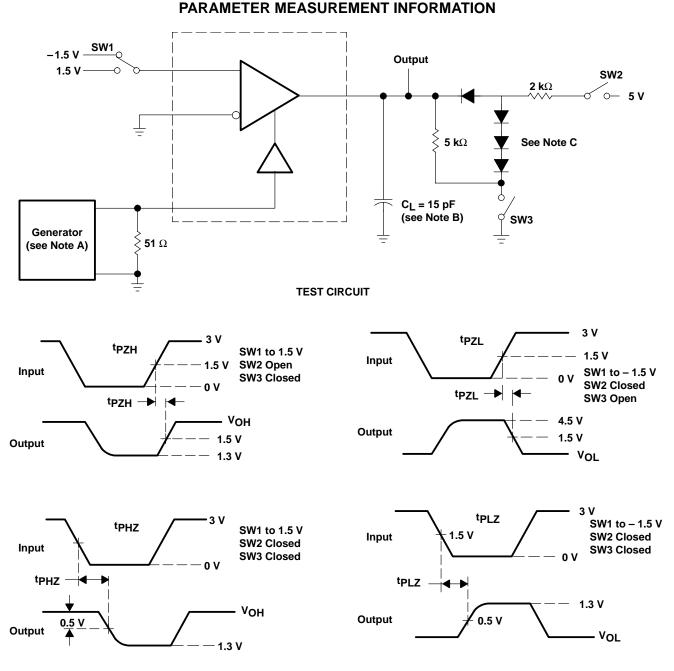


- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%, t<sub>r</sub>  $\leq$  6 ns,  $t_f \le 6 \text{ ns.}$ 
  - B. CL includes probe and stray capacitance.

#### **Figure 2. Test Circuit and Voltage Waveforms**

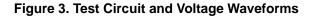


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NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%, t<sub>f</sub>  $\leq$  6 ns, t<sub>f</sub>  $\leq$  6 ns.

- B.  $C_L$  includes probe and stray capacitance.
- C. All diodes are 1N916 or equivalent.





### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
MC3486D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
MC3486DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
MC3486J	OBSOLETE	CDIP	J	16		None	Call TI	Call TI
MC3486N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
MC3486NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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