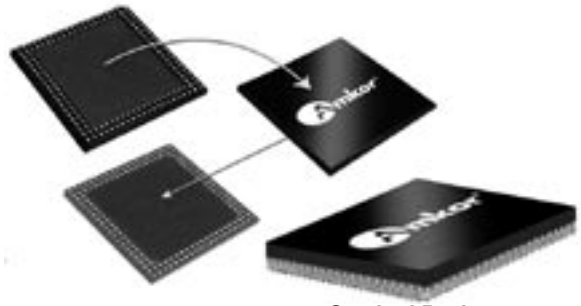
PoP
Package on Package

Amkor Technology®

NEW!

Amkor is offering daisy chain samples of their award winning bottom Package Stackable Very Thin Fine Pitch BGA (PSvfBGA) and their top PoP optimized for Package on Package (PoP) requirements. PoP has become the solution of choice for an increasing number of mobile consumer applications for 3D integration of logic and memory devices. Amkor's PSvfBGA is a high density fine pitch BGA package supporting logic or ASIC devices including base band, application and image processors. PoP stacking allows the OEM greater device, supplier and time to market flexibility by sourcing the bottom and top devices from their preferred logic and memory suppliers and then stacking the devices in the PWB surface mount assembly flow. A wide range of leading wireless and mobile integrated device manufacturers are relying on Amkor's technical and industry leadership in PoP.



Stacked Package

PoP Package on Package—*Mating Top and Bottom Daisy Chain Samples*

Part Number	I/O Count	Pitch	Body Size	Ball Matrix	Ball Alignment	Quantity Per Tray
12mm Body Size						
A-PoP128-.65mm-12mm-DC	128 (top)	.65mm	12mm	18 x 18	Perimeter	160
A-PSvfBGA305-.5mm-12mm-DC	305 (bottom)	.5mm	12mm	23 x 23	Perimeter	160
14mm Body Size						
A-PoP152-.65mm-14mm-DC	152 (top)	.65mm	14mm	21 x 21	Perimeter	126
A-PSvfBGA353-.5mm-14mm-DC	353 (bottom)	.5mm	14mm	26 x 26	Perimeter	126

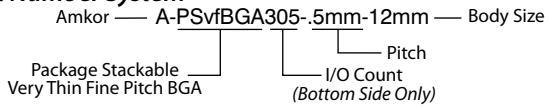
Notes

- Fine pitch 0.5mm bottom package footprints
- Stacked package heights of 1.2mm to 1.6mm available in a variety of configurations (see Stack Up table on following pages)
- Wafer thinning / handling < 100 µm
- Consistent product performance and reliability
- Package configurations compliant with JEDEC standards
- Moisture Resistance Testing is JEDEC Level 3 @ 260 °C
- Temp Cycle –55/+125 °C, 1000 cycles
- HAST 130 °C, 85% RH, 96 hours
- Temp/Humidity 85 °C/85%RH/1000 hours
- High Temp Storage 150 °C, 1000 hours
- Board level Thermal Cycle –40/+125 °C, 1000 cycles
- Parts packaged in JEDEC matrix trays
- PoPs are only available Pb-free (not Tin-Lead). Available alloys are: SAC305, SAC405, SAC105 and SAC125Ni*
- *SAC125Ni (1.2%Sn/0.5%Ag/.05%Cu/98.25%Ni) is only available for bottom packages.
- It is recommended that parts be pre-baked at 125 °C for 48 hrs before using parts regarding moisture concern.
- PoP's are not available without solder balls.

See drawings on the following pages (5–10) for additional technical data. Color coded version available on our website: www.practicalcomponents.com

Practical Components is the exclusive distributor of Amkor Technology Mechanical Components.

Part Number System



Ball Diameter

I/O Count	Ball Diameter
128	0.45mm
152	0.45mm
305	0.3mm
353	0.3mm

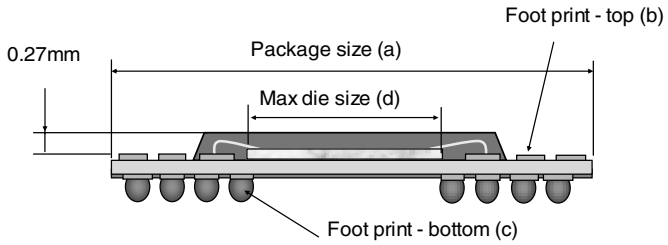
For recommended kits see pages 74 and 78.

Please Note

- **Amkor supporting data is available on our website for: Board Level Reliability (BLR), PoP application notes, PoP Stencil & Stacking paper for SMT Conditions.**
- **IMAPS and SMTA White Paper Articles for additional supporting data available on our website: www.practicalcomponents.com.**

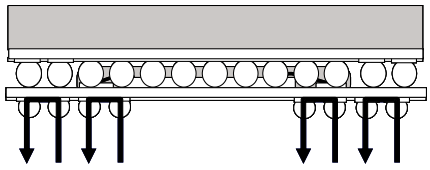
Package on Package (PoP)
12x12mm, 0.65mm to pitch
Stacked Daisy Chain

12mm 305 PSvfBGA Bottom Package Design Dimensions

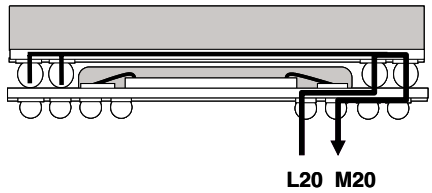


Body (a)	Foot Print–top (b)	Foot Print–bottom (c)	Die (d)	Bond Fingers Available
12 x 12mm	0.65 pitch, 128 ball 18 matrix, 2 row	0.5 pitch, 292 I/Os 23 matrix, 4 row + 12 NC + A1 ball 305 BGA	7.0 mm	332

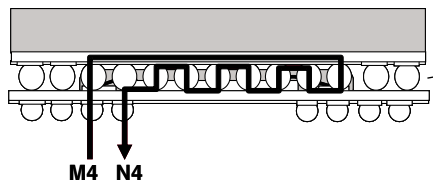
PoP Daisy Chain 3 Net Design



Daisy chain netlist of PSvfBGA, Bottom package balls.



Daisy chain netlist of top side (Top PoP to PSvfBGA 12 corner balls reserved for NC or additional supplies as memory combinations may require).



Daisy chain netlist of top side (Top PoP to PSvfBGA 116 pin memory interface).

Bottom package called: Package Stackable very thin fine pitch BGA (PSvfBGA).

**** Color diagram of DC Net design available on our website.***

Package on Package (PoP)
12x12mm Stacked Daisy Chain

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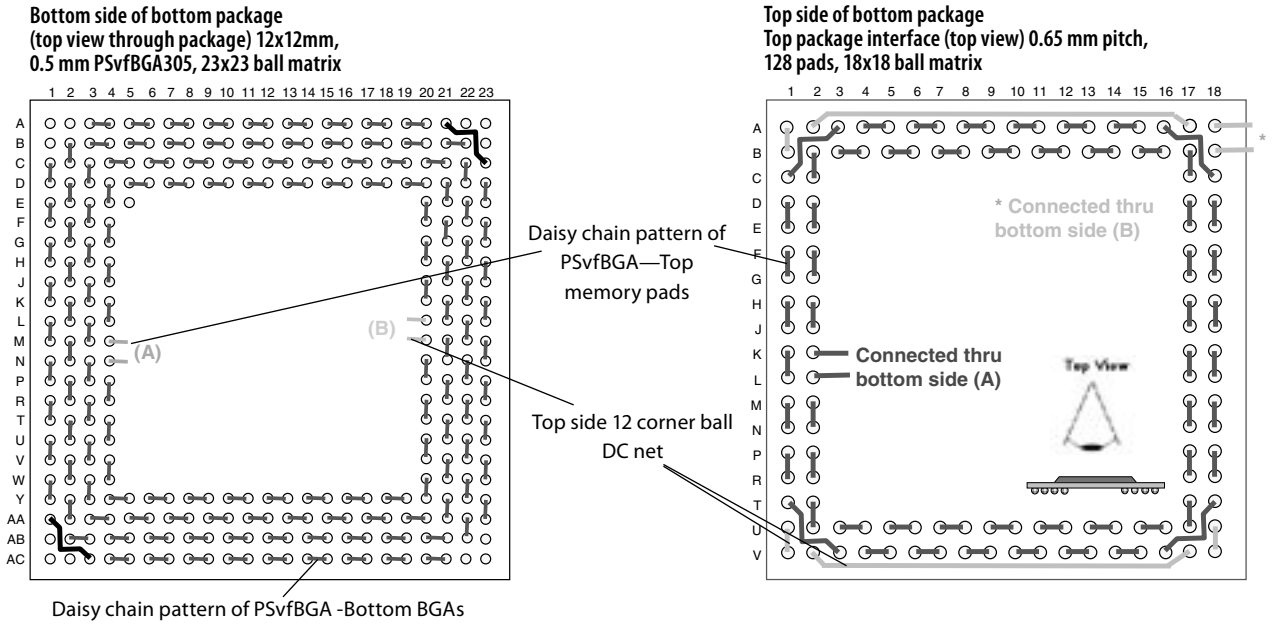
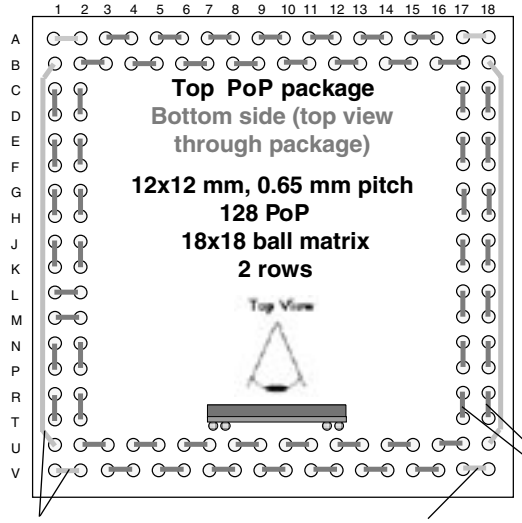
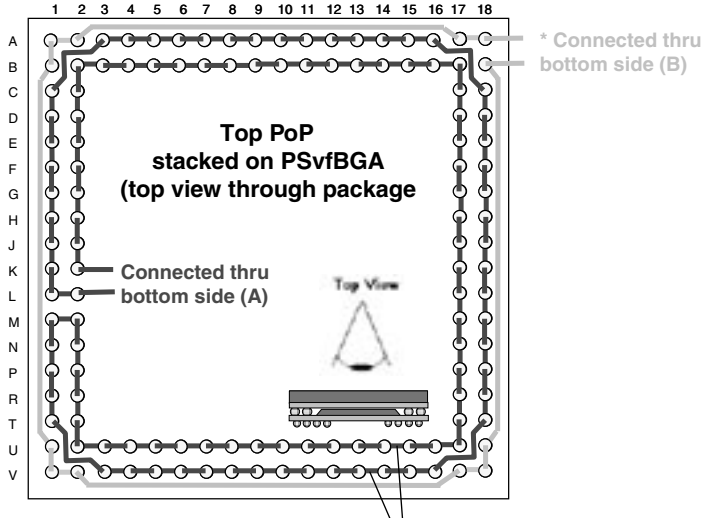
PSvfBGA 305
(Bottom Package) Daisy Chain Nets



128 PoP (Top Package) Daisy Chain Netlist



PoP + PSvfBGA Daisy Chain Netlist



Daisy chain pattern for 12 corner balls (typically reserved as NC for applications with no underfill, or option to add additional I/O or memory supplies as required for high density combinations)

Daisy chain pattern of Top package for 116I/O memory interface

Daisy chain netlist of Top PoP and PSvfBGA.

**** Color diagram of DC Net design available on our website.***

Package on Package (PoP)

12x12mm Stacked Daisy Chain

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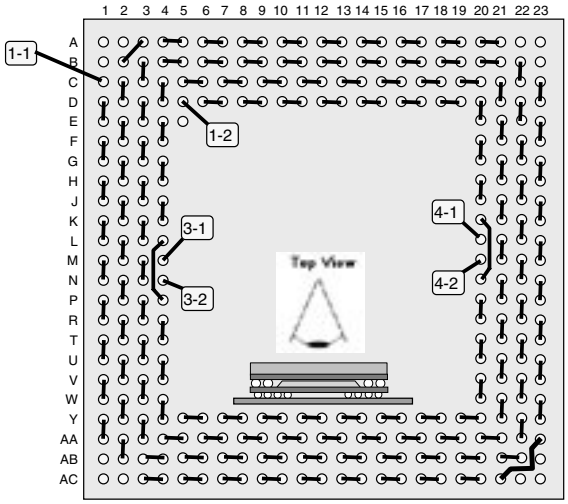
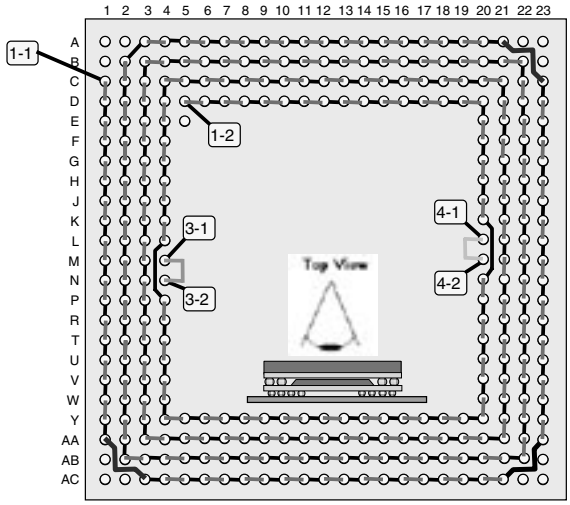
PWB Netlist Pattern for BLR Testing



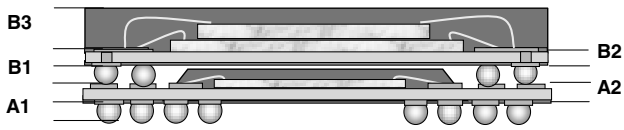
Black line: PWB pattern
In: 1-1, 3-1, 4-1
Common: 1-2, 3-2, 4-2

Stacked view of 3 DC Nets for BLR testing



Black line: PWB pattern
In: 1-1, 3-1, 4-1
Common: 1-2, 3-2, 4-2

PoP Overall Stack Up Example



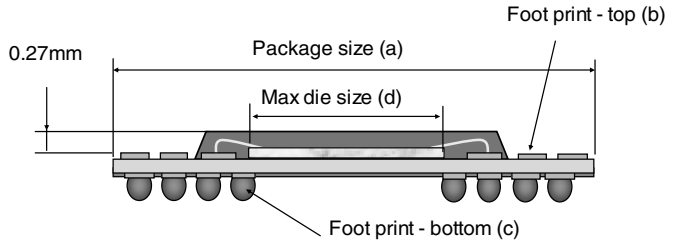
		PoP +PSvfBGA		
Symbol	**Unit**	**Min**	**Max**	**Nom**
A1 (Ball, 0.5 pitch)	mm	0.150	0.250	0.200
A2 (4L laminate)	mm	0.260	0.340	0.300
B1 (Ball, 0.65 pitch)	mm	0.270	0.330	0.300
B2 (2L laminate)	mm	0.180	0.240	0.210
B3 (Mold cap)	mm	0.420	0.480	0.450
Overall Pkg Height	mm	1.378	1.542	1.460

B2 and B3 may vary depending on top memory PoP (MCP) design rules.
Overall Stack up to be finalized based on top PoP rules.

**** Color diagram of DC Net design available on our website.***

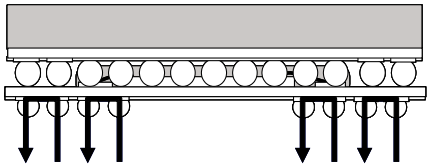
Package on Package (POP)
14x14mm
Stacked Daisy Chain

14mm 353 PSvfBGA
Bottom Package Design Dimensions

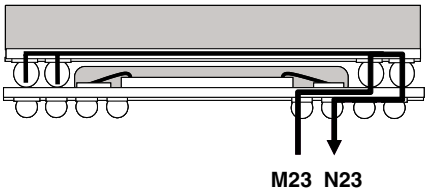


Body (a)	Foot Print–top (b)	Foot Print–bottom (c)	Die (d)	Bond Fingers Available
14 x14 mm	0.65 pitch, 152 ball 21 matrix, 2 row	0.5 pitch, 340 I/Os 26 matrix, 4 row + 12 NC + A1 ball 353 BGA	8.9 mm	328 to 396

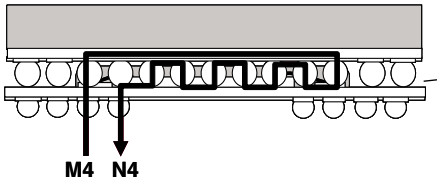
PoP Daisy Chain 3 Net Design



Daisy chain netlist of PSvfBGA, Bottom package balls



Daisy chain netlist of top side (Top PoP to PSvfBGA 12 corner balls reserved for NC or additional supplies as memory combinations may require).



Daisy chain netlist of top side (Top PoP to PSvf-BGA 140 pin memory interface)

Bottom package called: Package Stackable very thin fine pitch BGA (PSvfBGA)

**** Color diagram of DC Net design available on our website.***

Package on Package (PoP)

14x14mm Stacked Daisy Chain

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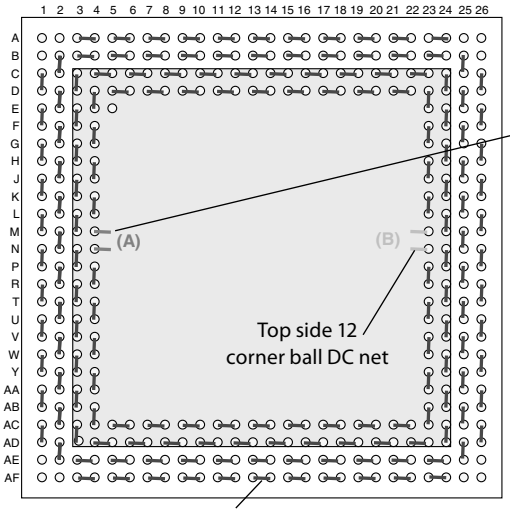
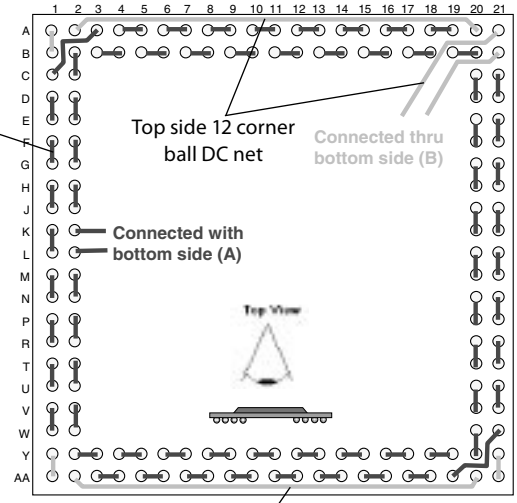
PSvfBGA 353 (Bottom Package) Daisy Chain Nets

Bottom side (top view through package) 14x14mm, 0.5 mm PSvfBGA353, 26x26 ball matrix



Daisy chain pattern of PSvfBGA—Top memory pads

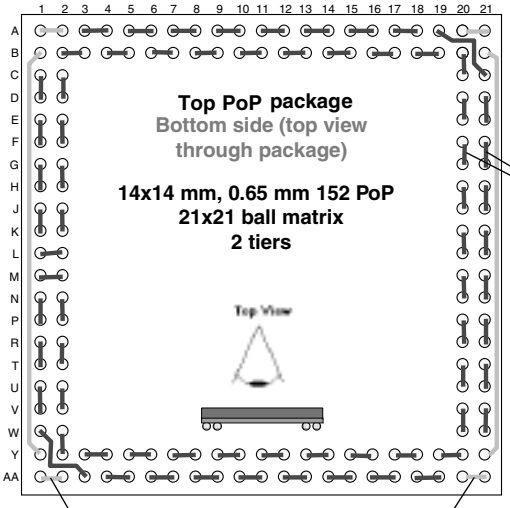
Top side—Top package interface (top view) 0.65 mm pitch, 152 pads, 21x21 ball matrix



Daisy chain pattern of PSvfBGA—Bottom BGAs

Top side 12 corner ball DC net

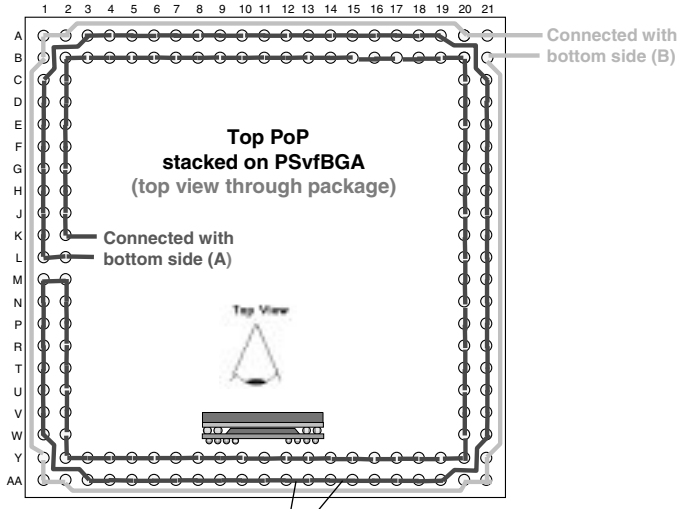
152 PoP (Top Package) Daisy Chain Netlist



Daisy chain pattern of Top package for 140 I/O memory interface

Daisy chain pattern for 12 corner balls (typically reserved as NC for applications with no underfill, or option to add additional I/O or memory supplies as required for high density combinations).

Top PoP + PSvfBGA Daisy Chain Netlist



Daisy chain netlist of Top FBGA and PSvfBGA

**** Color diagram of DC Net design available on our website.***

Package on Package (PoP)

14x14mm Stacked Daisy Chain

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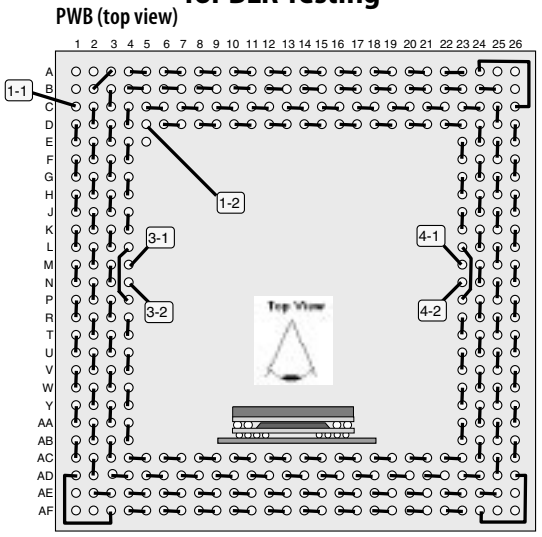
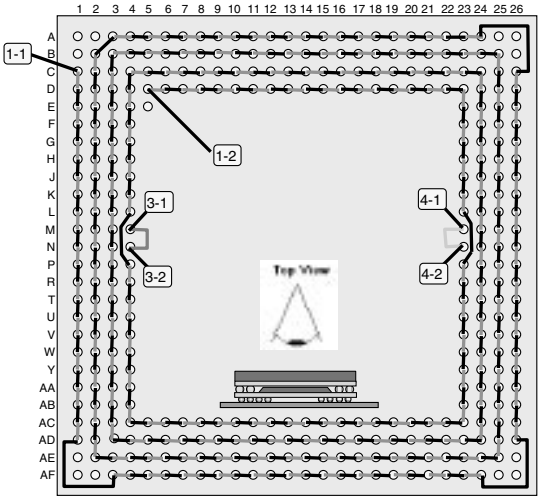
PWB Netlist Pattern for BLR Testing



Black line: PWB pattern
In: 1-1, 3-1, 4-1
Common: 1-2, 3-2, 4-2

Stacked View of 3 DC Nets For BLR Testing



Black line: PWB pattern
In: 1-1, 3-1, 4-1
Common: 1-2, 3-2, 4-2

PoP Overall Stack Up Example

		PoP + PSvfBGA		
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Overall Package Height	mm	1.378	1.542	1.460

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