

Flip Chip describes the method of electrically connecting the die to the package carrier. The package carrier, either substrate or leadframe, then provides the connection from the die to the exterior of the package. The interconnection between die and carrier in flip chip packaging is made through a conductive bump that is placed directly on the die surface. The bumped die is then flipped over and placed face down, with the bumps connecting to the carrier. After the die is soldered, underfill is applied between the die and the substrate, around the solder bumps. The underfill is designed to contract the stress in the solder joints caused by the difference in thermal expansion between the silicon die and carrier.

UBM is the Al/NiV/Cu (under bump metallization) covering about 1% of the wafer which is under the bumps only. Nitride passivation is an invisible glass-like protective coating over 99% of the wafer, except under the bumps. The bumps will not stick to the Nitride, only the UBM. Nitride coating is standard for all Flip Chip wafers.

Flip Chips

Part Numbers:	PB18-250x250	PB18-500x500	FA10-200x200 FA10-400x400 FA10-600x600	PB08-200x200 PB08-400x400	PST02-150x150	PB06-200x200 PB06-400x400 PB06-400x600
Die Size	250 x 250 mils	500 x 500 mils	200 x 200 mils 400 x 400 mils	200 x 200 mils 400 x 400 mils	150 x 150 mils	200 x 200 400 x 400 400 x 600
Bump Pitch	457 µm, 18 mil	457 µm, 18 mil	254 µm, 10 mil	203 µm, 8 mil	457 µm, 18 mil	152µm, 6mil
Passivation Via	102 µm	102 µm	80 µm	73 µm	102 µm	89µm
UBM Diameter	178 µm	178 µm	102 µm	95 µm	152 µm	—
Bump Height	140 µm	140 µm	120 µm	98 µm	130 µm	85µm
Bump Diameter	190 µm	190 µm	135 µm	120 µm	160 µm	—
No. of Bumps	48	96	317	88	21	112
Final Metal Pad Size Thickness Type	193 x 193 µm	193 x 193 µm	127 x 127 µm	115 x 115 µm	165 x 165 µm	—
Metal Composition	98/1/1 Al/Cu/Si	98/1/1 Al/Cu/Si	98/1/1 Al/Cu/Si	98/1/1 Al/Cu/Si	98/1/1 Al/Cu/Si	98/1/1 Al/Cu/Si
Packaging						
Uncut Wafer*	5" Wafer 250 x 250 mils (243) Die	5" Wafer 500 x 500 mils (46 Die)	5" Wafer 200 x 200 mils (344Die) 400 x 400 mils (87 Die)	5" Wafer 200 x 200 mils (344 Die)	5" Wafer 150 x 150 mils (682 die)	5" Wafer 200 x 200 mils (344 Die) 400 x 400 mils (87 Die)
Tray	Sawed 5" Wafer 25 per tray 2" sq Waffle Pack	Sawed 5" Wafer 9 per tray 2" sq Waffle Pack	Sawed 5" Wafer 36 per tray 200 x 200 9 per tray 400 x 400 Waffle Pack	Sawed 5" Wafer 36 per tray 200 x 200 Waffle Pack	Sawed 5" Wafer 25 per tray 2" sq Waffle Pack	Sawed 5" Wafer 25 per tray 2" sq Waffle Pack
Tape and Reel	Call For Availability	Call For Availability	Call For Availability	Call For Availability	Call For Availability	Call For Availability

Notes

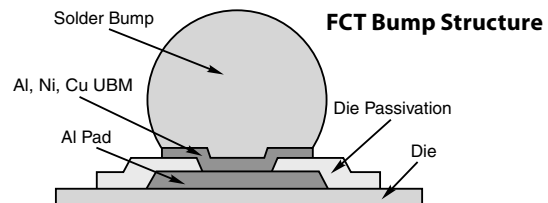
- * Die count represents expected yield per wafer.
- All die is packaged in waffle pack trays unless otherwise specified.
- All test wafers are currently 5" diameter and are 0.635mm thick. Passivation is one-micron thick plasma Nitride with round via openings.
- The potential multiple is the number of die repeats on the wafer. With the wafer orientated flat down, a right hand coordinate system applies.
- Die size is from scribe line to center-to-center. Scribe width is 0.05mm passivated. Each bump is electrically connected to one other bump and isolated from all others to facilitate electrical test.
- Bump pitch is defined as center-to-center distance between passivation openings.
- Bump height is defined as silicon surface to the top of the bump.
- Bump diameter is defined as the maximum diameter.
- UBM = Under Bump Metallurgy
- Test board is not available for the PB06 package.
- Lead-free parts are available with 95.5% Sn/ 3.5% Ag/ 1.0% Cu alloy.
- Unbumped wafers are available upon special request.



Part Number System



- Add "WR" to end of part number for Wafer Cut and left in Seal Ring.
- Add "TR" to end of part number for die on Tape and Reel.
- Add "EUT" to end of part number for Eutectic.
- Add "LF2" to end of part number for Lead-Free.
- Add "W" to end of part number for Uncut Wafer.
- Add "unbumped" to end of part number for unbumped wafer/die.



For kits see pages 71, 80 and 81 .

About Lead-Free Flip Chips

Flip Chips are used in evaluating assembly techniques, board continuity, temperature cycle life test evaluation, underfill processes and other generic Flip Chip evaluations. When using Lead-Free Flip Chips, consideration needs to be given to the appropriate flux, underfill, temperature profile, and pad finish for the assembly. Many companies are developing and qualifying alternative pad finishes such as immersion Sn. Lead-Free Flip Chips address the need for environmentally conscious assemblies as well as Alpha particle tolerant packaging.

Lead-Free Die

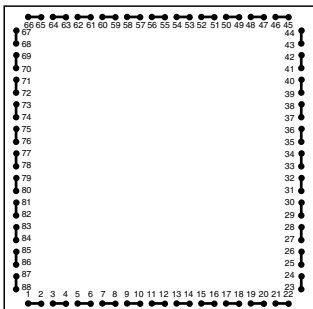
- All Flip Chips are available Lead-Free with Alloy LF2 composition 95.5% Sn /3.5% Ag /1.0% Cu.
- When ordering Lead-Free Flip Chips, add "LF2" to end of part number.
- LF2 was introduced by FCT (the acronym is Lead-Free #2).



For kits see pages 71, 80 and 81.

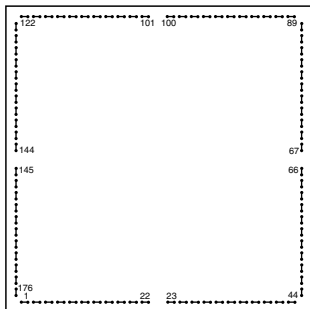
Daisy-Chain Patterns

PB08-200x200



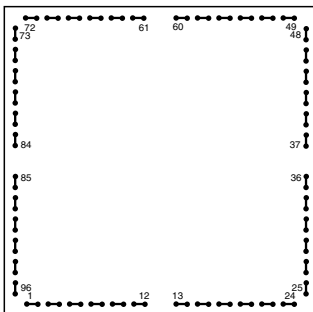
Die size: 5.08mm sq.

PB08-400x400



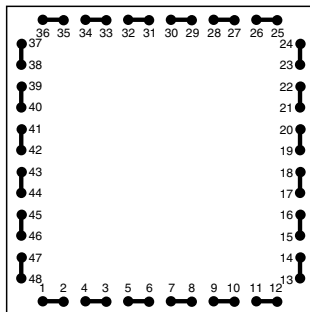
Die size: 10.16mm sq.

PB18-500x500



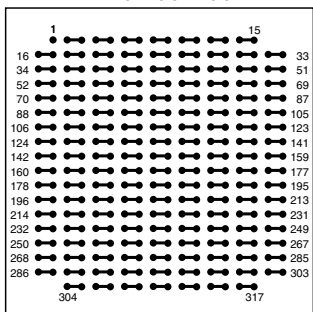
Die size: 12.70mm sq.

PB18-250x250



Die size: 6.35mm sq.

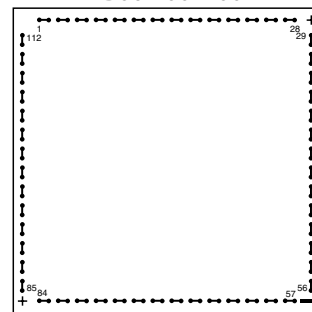
FA10-200x200



Die size: 5.08mm sq.

The FA10 daisy-chain test die is designed with a 10-mil pitch (254µm) array of solder bumps across the surface of the die. They are configured in "quad" structures for versatile assembly and evaluation options. The array pattern is an 18 row x 18 column footprint minus four pairs of corner bumps. The addition of a key bump in the upper left corner addresses alignment requirements. Each die contains 317 I/O (158 daisy-chain pairs). This device is offered with eutectic or Pb-free solder bumps.

PB06-200x200



Die size: 5.08mm sq.

The PB08 daisy-chain test die is designed with an 8-mil (203µm) solder bump pitch around the perimeter of the device. Each die contains 99 I/O (44 daisy-chain pairs). The device comes in two sizes: 200mil x 200mil and 400mil x 400mil. The PB08-400x400 device consists of 4 PB08-200x200 devices without the inner I/O's bumped.

The PB18 daisy-chain test die is designed with an 18-mil solder bump pitch around the perimeter of the device. Each die contains 48 I/O (24 daisy-chain pairs). The device comes in two sizes: 250mil x 250mil (6.35mm x 6.35mm) and 500mil x 500mil (12.7mm x 12.7mm). The PB18-500x500 device consists of 4 PB18-250x250 devices without the inner I/O's bumped.

Al/NiV/Cu Combination of thin film conductor layers that are sputtered and then etched to form the UBM pads in FlipChip's SFC, Repassivation, UltraCSP, and Polymer Collar WLP flows. Also forms the redistribution runners in the UltraCSP flow. Also known as one of the combinations of metals used to form the Under-Bump-Metallurgy (UBM).

Array A pattern of columns and rows. Used to describe bumps that are evenly spaced in rows and columns all across the die surface and not just near the edges.

Array Pattern Number of rows and columns in a matrix-designed layout of solder balls. Can be a fully formed array or may be partially depopulated, with the absence of bumps toward the center of the array.

Ball Diameter Diameter of the pre-formed solder sphere used in Wafer Level Packaging. Typical ball diameters are 300, 350, 400, and 500µm.

BCB (Benzocyclobutene) Dielectric coating that provides an additional passivation layer on top of the IC passivation for Repassivation, Redistribution, UltraCSP, and Polymer Collar WLP designs.

BCB1 Opening (Via) Opening in the first layer of BCB where IC aluminum pads will be re-routed to facilitate a certain UltraCSP designs.

BCB2 Opening (Via) Opening in the second layer of BCB which will define the metal exposure (wettable area) of the UBM pad. BCB2 will cover all re-distribution traces to protect metal runners from corrosion and physical damage.

Bond Pad Exposed final metal portion of the device I/O (also see, Pad).

Bump A small metal alloy deposit on the die that is melted to a pad on the board to form the electrical connection between the board and the die.

Bump Diameter The widest measurement through the center cross-section of a re-flowed bump.

Bump Height Vertical measurement from the top of the device passivation to the top of the bump after reflow (not yet attached to PCB substrate). After assembly, the analogous measurement is called "stand-off height".

Bump Shear Shear value (force measured in grams) and failure mode measured during ball shear test.

Bump Standoff Height Measurement from FR4 surface to silicon surface.

Cu Pad Solder receiving pad on the substrate that is Cu etch-defined.

Die (Chip) A square or rectangular piece cut from the wafer that contains the electrical pattern and is repeated in several rows and columns across the top surface of the wafer.

Die (Chip) Size The active silicon chip area bounded on the outside by the scribe street.

Die (Chip) Stepping Distance The distance between one point on a die and the same point on an adjacent die. This measurement takes into account both the die size along with the width of the street.

DNP Distance to neutral point. The distance from an I/O to the center of the die. Maximum DNP defines the largest array size for a given process technology that will meet the minimum thermal fatigue performance criteria as established by FlipChip.

EliteCSP A WLCSP product line that is specifically designed for bumping applications that require rapid cycle times, quick time to market, low bumping costs, and high temperature stability. Utilizes a plated Nickel UBM.

ESD (Electrostatic discharge) The release of static electricity from one surface to another. Because IC devices and assemblies may be damaged by ESD, precautions are taken to eliminate ESD in IC manufacturing and test areas.

Final Metal Uppermost metal layer in a device. This layer is usually covered with a thick dielectric passivation.

Flip Chip A die that has bumps to create the electrical connection between the die and the board. So called because the die has to be flipped over in order to be assembled.

I/O The location of the signal interfaces that contacts to the "outside" world.

I/O Final Metal Bond Pad Same as I/O.

I/O Metal Pad Size Size of metal bond pad on an I/O, as manufactured during normal IC processing.

Maximum DNP DNP stands for Distance to Neutral Point. A maximum DNP is the distance from the furthest I/O (solder bump) to the minimum stress point on the die. For a symmetric array pattern, it is also the geometric center of the die.

MDIF (Mask Design Information Form) FlipChip information form that provides FlipChip with a description of the wafer, the die, and how you would like to bump it.

NSMD (Non-Solder Mask Defined) PCB Copper pads that are smaller than the solder mask openings.

Pad Metal area on the die that the bump or wire is attached to (also see, Bond Pad).

Partial Die An incomplete die usually located on the edge of the wafer.

Passivation Uppermost layer on an IC. Used for circuit protection and cushioning. Typically Nitride, Polyimide, Oxide, or Oxi-Nitride.

Peripheral The edge of the die. Used to describe bumps that are placed near the edges of the die.

PO (Passivation Opening) Opening in the passivation over the I/O final metal bond pads.

PCB Printed Circuit Board

Pitch The linear distance between the centers of two adjacent I/Os or bumps.

PIQ (Polyimide Isoindoro Quinazorindione) Dielectric polymer material used as a passivation layer in some semiconductor devices.

Repassivation Layer of Passivation added by FlipChip as part of the bumping process. This layer adds robustness and can correct inappropriate Passivation Openings and Final Metal Pads. The repassivation layer is typically BCB or Spheron Polymer.

RDL (Re-Distribution Line) Metal deposited at the same time as the UBM pad for the purpose of re-routing I/O sites, for example from edge-distributed bond pads used in wire-bonded applications, to an array layout. Also broadly used to describe the process of rerouting I/O.

SMD (Solder Mask Defined) PCB pads that have solder-mask openings smaller than the copper pads.

Solder Mask A layer of passivation material covered on top of outer-layer conductor (Cu) that has openings to allow solder wet to the Cu pads and prevents solder bridging in the rest area. These openings are called Solder Mask Openings.

Solder Paste Reflowable pre-mixed solder paste that is printed and formed into a solder sphere. Provides the electrical connection between the die and the package substrate or printed circuit board. Since it is premixed, it provides for excellent composition control. Typically made up of two to four metals.

Solder/Flux Ratio The volume ratio of flux to solder in the solder paste. A 50/50 ratio of solder to flux is recommended.

Spheron™ New FlipChip WL-CSP product predominately used in high frequency applications.

Stencil Aperture Opening The laser-cut, Nickel Additive (E-Fab), Chemically Etched, or Electroform aperture openings on the solder paste stencil.

Stepping Distance Linear measurements in both the x and y directions comprising die size and to the center of the scribe streets on all four sides. (see die stepping distance).

Street The non-electrically active area on the wafer in between the die. Also known as the Saw Street.

UBM (Under-Bump-Metallurgy) The metal stack that is deposited under the bump as part of the solder bumping process. It has the combined features of adhesion layer, diffusion barrier, wetting layer and oxidation protection layer. FlipChip uses NiV/Cu, Al/NiV/Cu, or Al/NiV/Cu/Ti/NiV/Cu as the UBM

Wafer A round flat disk most often made of silicon that is patterned with several die by semiconductor thin-films processing. Each wafer has a flat or notch cut into its edge to help with aligning or orienting the wafer.

Wafer Map A representation of the wafer that notes where all of the defective die are located.

Wire Bond The electrical connection consisting partially of a wire that bridges the die to the board.

WLP Wafer level package

Daisy-Chain Patterns



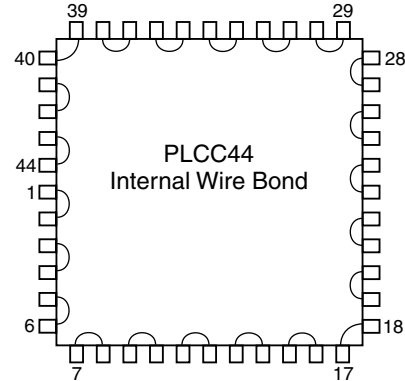
Daisy Chain "Even" Pattern

Example of daisy-chain "even" pattern for leadframe packages. Pin 1-2, 3-4, 5-6, 7-8, etc.

Continuity testing requires dummy components to contain daisy-chain connections.

The standard daisy chain pattern for non-BGA IC's is Even.

There is no standard daisy chain pattern for BGA, Flip Chip and chip scale packages.



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For the latest information on all of our products, package outline drawings and daisy-chain (dog-bone) patterns, please see our website www.practicalcomponents.com.



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**NOW
AVAILABLE!**

Pb-Free HASL PCB Finish

One of the most popular final finishes is known as Hot Air Surface Leveling otherwise known as HASL. A viable lead free HASL process utilizing the Nihon Superior SN100CL lead free solder alloy is available.

Testing to date has shown that the SN100CL lead free HASL process offers superior solderability to the final finishes on the market today. All of the final finishes available on the market today have both their merits and demerits. Many in the board industry are concerned about switching from HASL to a less forgiving final finish as they transition to the up and coming lead free era. Our process should ease these concerns. This process is also directed towards those who are not completely satisfied with their current final finish. There are two major lead free solder alloys on the market today: SN100CL and the SAC alloy. The SN100CL nominal composition is a stabilized eutectic tin copper. The SAC 305 alloy consists of tin, copper and 3% silver.

The Advantages of SN100CL Lead-Free HASL

- A robust process.
- Improved shelf life compared to 63/37 (2).
- Minimal temperature increase in the solder pot (Solder pot temp. est. 485-500°F).
- No copper attack (e.g., copper traces, holes on circuit board).
- Minimal stainless steel attack. SAC 305 alloy rapidly attacks Stainless Steel.
- Superior wetting yielding a more uniform and flat surface.
- Capable of handling very fine pitch due to excellent wetting.
- Compatible with both conventional 63/37 and lead free final assembly.
- More economical (No Silver).

Call Practical for availability.

Plastic Ball Grid Arrays (PBGA) incorporate advanced assembly processes and designs for low cost, high performance applications. PBGAs are designed for low inductance, improved thermal operation and enhanced SMT-ability.

All PBGAs listed on this page are daisy-chained and available lead-free.

PBGA Plastic Ball Grid Array 1.0mm Pitch

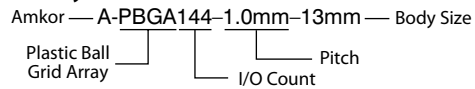
Part Number	I/O Count	Pitch	Body Size	Ball Matrix	Ball Alignment	Quantity Per Tray	Available Lead-Free Alloys
A-PBGA144-1.0mm-13mm	144	1.0mm	13mm	12 x 12	Full Array	160	SAC405, SAC305 or Sn3.5Ag
A-PBGA156-1.0mm-15mm	156	1.0mm	15mm	14 x 14	Perimeter	126	SAC405, SAC305 or Sn3.5Ag
A-PBGA160-1.0mm-15mm	160	1.0mm	15mm	14 x 14	Perimeter	126	SAC405, SAC305 or Sn3.5Ag
A-PBGA196-1.0mm-15mm	196	1.0mm	15mm	14 x 14	Full Array	126	SAC405, SAC305 or Sn3.5Ag
A-PBGA208-1.0mm-17mm	208	1.0mm	17mm	16 x 16	Perimeter	90	SAC405, SAC305 or Sn3.5Ag
A-PBGA256-1.0mm-17mm	256	1.0mm	17mm	16 x 16	Full Array	90	SAC405, SAC305 or Sn3.5Ag
A-PBGA288-1.0mm-23mm	288	1.0mm	23mm	22 x 22	Perimeter	60	SAC405, SAC305 or Sn3.5Ag
A-PBGA289-1.0mm-19mm	289	1.0mm	19mm	17 x 17	Full Array	84	SAC405, SAC305 or Sn3.5Ag
A-PBGA324-1.0mm-19mm	324	1.0mm	19mm	18 x 18	Full Array	84	SAC405, SAC305 or Sn3.5Ag
A-PBGA324-1.0mm-23mm	324	1.0mm	23mm	22 x 22	Perimeter	60	SAC405, SAC305 or Sn3.5Ag
A-PBGA484-1.0mm-27mm	484	1.0mm	27mm	26 x 26	Perimeter	40	SAC405, SAC305 or Sn3.5Ag
A-PBGA516-1.0mm-31mm	516	1.0mm	31mm	30 x 30	Perimeter	27	SAC405, SAC305 or Sn3.5Ag
A-PBGA580-1.0mm-35mm	580	1.0mm	35mm	34 x 34	Perimeter	24	SAC405, SAC305 or Sn3.5Ag
A-PBGA676-1.0mm-27mm	676	1.0mm	27mm	26 x 26	Full Array	40	SAC405, SAC305 or Sn3.5Ag
A-PBGA680-1.0mm-35mm	680	1.0mm	35mm	34 x 34	Perimeter	24	SAC405, SAC305 or Sn3.5Ag
A-PBGA928-1.0mm-40mm	928	1.0mm	40mm	39 x 39	Perimeter	21	SAC405, SAC305 or Sn3.5Ag
A-PBGA1156-1.0mm-35mm	1,156	1.0mm	35mm	34 x 34	Full Array	24	SAC405, SAC305 or Sn3.5Ag

Notes

- Overall thickness of 1.0mm pitch PBGA packages will vary (please call for more details).
- Parts are packaged in JEDEC trays.
- Call for tape and reel quantity and availability.
- Solder ball material is eutectic 63/37 SnPb.
- All components are daisy-chained.
- Daisy-chained connections are connections between I/O (input/output) of the component.
- BT (Bismaleimide-Triazine) substrates.
- JEDEC MS-034 standard outlines.
- Ball diameter varies (see chart).
- BGA packages should be baked at 125°C for 24 hours prior to assembly to prevent delamination during the assembly process.
- Moisture sensitivity is JEDEC level 3.
- Lead-free parts are available with (SAC405) 95.5% Sn/ 4.0% Ag/ 0.5% Cu alloy or 96.5%Sn/3.0%Ag/0.5%Cu alloy (SAC305) is also available. Sn3.5Ag is also available (call for availability).
- PBGA's are not available without solder balls.



Part Number System



- Add "TR" to end of part number for Tape and Reel.
- Add "SAC405" or "SAC305" or "Sn3.5Ag" to end of part number for Lead-Free.



For kits see pages 56, 57, 58, 60, 63, 64, 73, 79 and 82.



Practical Components is the exclusive distributor of Amkor Technology Mechanical Components.

PBGA

Plastic Ball Grid Array



Amkor Plastic Ball Grid Arrays (PBGA) incorporate advanced assembly processes and designs for low cost, high performance applications. PBGAs are designed for low inductance, improved thermal operation and enhanced SMT ability.

Some PBGAs are available daisy-chained. All PBGAs are available lead-free.



PBGA Plastic Ball Grid Array 1.5mm/1.27mm Pitch

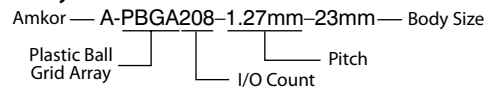
Part Number	I/O Count	Pitch	Body Size	Ball Matrix	Ball Alignment	Quantity Per Tray	Available Lead-Free Alloys
A-PBGA208-1.27mm-23mm*	208	1.27mm	23mm	17 x 17	Perimeter	60	SAC405, or SAC305 or Sn3.5Ag
A-PBGA217-1.27mm-23mm*	217	1.27mm	23mm	17 x 17	Perimeter	60	SAC405, or SAC305 or Sn3.5Ag
A-PBGA256-1.27mm-27mm*	256	1.27mm	27mm	20 x 20	Perimeter	40	SAC405, or SAC305 or Sn3.5Ag
A-PBGA272-1.27mm-27mm*	272	1.27mm	27mm	20 x 20	Perimeter	40	SAC405, or SAC305 or Sn3.5Ag
A-PBGA329-1.27mm-31mm	329	1.27mm	31mm	23 x 23	Perimeter	27	SAC405, or SAC305 or Sn3.5Ag
A-PBGA356-1.27mm-27mm*	356	1.27mm	27mm	20 x 20	Perimeter	40	SAC405, or SAC305 or Sn3.5Ag
A-PBGA388-1.27mm-35mm*	388	1.27mm	35mm	26 x 26	Perimeter	24	SAC405, or SAC305 or Sn3.5Ag
A-PBGA420-1.27mm-35mm	420	1.27mm	35mm	26 x 26	Perimeter	24	SAC405, or SAC305 or Sn3.5Ag
A-PBGA456-1.27mm-35mm	456	1.27mm	35mm	26 x 26	Perimeter	24	SAC405, or SAC305 or Sn3.5Ag
A-PBGA564-1.27mm-40mm*	564	1.27mm	40mm	30 x 30	Perimeter	21	SAC405, or SAC305 or Sn3.5Ag

Notes

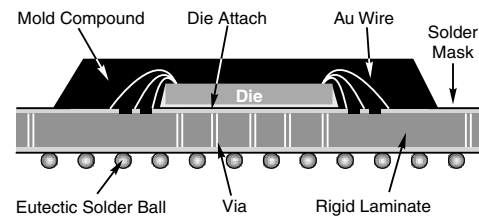
- * = DC available
- Parts are packaged in JEDEC trays.
- Call for tape and reel quantity and availability.
- Solder ball material is eutectic 63/37 SnPb.
- Daisy-chained connections are connections between I/O (input/output) of the component.
- BT (Bismaleimide-Triazine) substrates.
- JEDEC MS-034 standard outlines.
- Ball diameter varies (see chart).
- BGA packages should be baked at 125°C for 24 hours prior to assembly to prevent delamination during the assembly process.
- Moisture sensitivity is JEDEC level 3.
- Lead-free parts are available with (SAC405) 95.5% Sn/ 4.0% Ag/ 0.5% Cu alloy or 96.5%Sn/3.0%Ag/0.5%Cu alloy (SAC305) or Sn3.5Ag (call for SnAg availability)
- PBGA's are not available without solder balls.



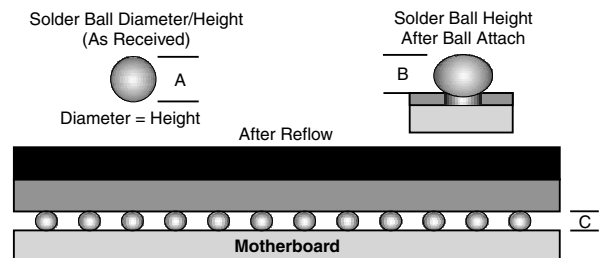
Part Number System



- Add "TR" to end of part number for Tape and Reel.
- Add "SAC405" or "SAC305" or "Sn3.5Ag" to end of part number for Lead-Free.



Note: Drawing not to scale.



Package	Pitch	Solder Ball Diameter (A)	Solder Ball Land On Package and Board	Solder Ball Height on Package (B)	Solder Joint Height After SMT* (C)
⁽¹⁾ PBGA	1.00	0.50	0.45	0.40	0.32
⁽²⁾ PBGA	1.00	0.63	0.45	0.55	0.48
PBGA	1.27	0.76	0.63	0.60	0.52
PBGA	1.50	0.76	0.63	0.60	0.52

Units = mm

*Assumptions: 5 mils Solder Paste

Solder Mask Defined Pad

Notes

- applies to 13, 15 and 17mm packages.
- applies to 23, 27, 31, 35mm, 37.5mm and 40.0mm packages.



For kits see pages 53 57, 60, 62, 64, 73 and 82.

SuperBGA® (SBGA) package is a very low profile, high-power BGA. The IC is directly attached to an integrated copper heatsink. Since the IC and the I/O are on the same side, signal vias are eliminated.

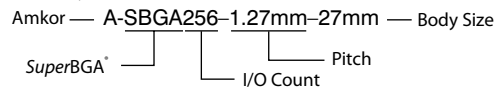
SBGA SuperBGA® 1.27mm Pitch

Part Number	I/O Count	Pitch	Body Size	Ball Matrix	Ball Alignment	Quantity Per Tray
A-SBGA256-1.27mm-27mm	256	1.27mm	27mm	20 x 20	Perimeter	40
A-SBGA304-1.27mm-31mm	304	1.27mm	31mm	23 x 23	Perimeter	27
A-SBGA352-1.27mm-35mm	352	1.27mm	35mm	26 x 26	Perimeter	24
A-SBGA432-1.27mm-40mm	432	1.27mm	40mm	31 x 31	Perimeter	21
A-SBGA520-1.27mm-40mm	520	1.27mm	40mm	31 x 31	Perimeter	21
A-SBGA560-1.27mm-42.5mm	560	1.27mm	42.5mm	33 x 33	Perimeter	12
A-SBGA600-1.27mm-45mm	600	1.27mm	45mm	35 x 35	Perimeter	12

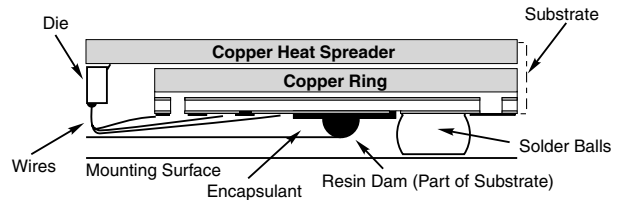
Notes

- Superior thermal performance.
- Light weight
- Low profile (1.4mm mounted)
- Moisture resistant (JEDEC level 3)
- JEDEC MO-192 standard outlines
- Enhanced electrical performance > 1 GHz
- Parts are packaged in JEDEC trays.
- Call for tape and reel quantity and availability.
- Solder ball material is eutectic 63/37 SnPb.
- BGA packages should be baked at 125°C for 24 hours prior to assembly to prevent delamination during assembly process.
- Parts can be baked and dry-packed.
- All components are daisy-chained except for 520 I/O.
- Lead-free parts are available with (SAC405) 95.5% Sn/ 4.0% Ag/ 0.5% Cu alloy or 96.5%Sn/3.0%Ag/0.5%Cu alloy (SAC305). Sn3.5Ag is also available (call for availability).
- SBGA's are not available without solder balls.

Part Number System



- Add "TR" to end of part number for Tape and Reel.
- Add "SAC405" or "SAC305" or "Sn3.5Ag" to end of part number for Lead-Free.

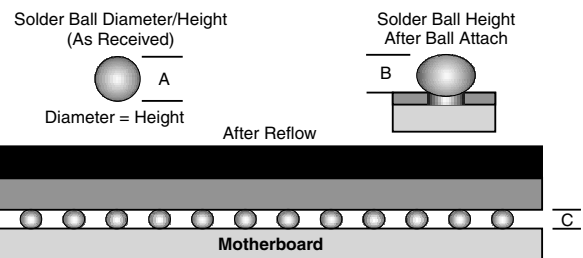


Note: Drawing not to scale.



Looking for Lead-Free?

This symbol indicates that lead-free parts are available!



Package	Pitch	A	B	C
SBGA	1.27	.76	.62	.52

All units in mm.

Assumptions: 5 mils solder paste. Solder mask defined pad. Typical motherboard no solder mask defined pad:

- 0.50 Pitch – 0.28
- 0.80 Pitch – 0.30
- 1.00 Pitch – 0.38

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