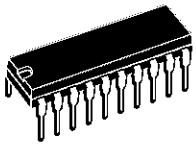
SGS-THOMSON MICROELECTRONICS

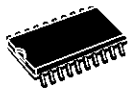
74AC573

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT NON INVERTING

- HIGH SPEED: t_{PD} = 4.5 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 8 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24 mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 573
- IMPROVED LATCH-UP IMMUNITY



B
(Plastic Package)



M
(Micro Package)

ORDER CODES :

74AC573B 74AC573M

DESCRIPTION

The AC573 is an advanced high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power applications mantaining high speed operation similar to equivalent Bipolar Schottky TTL.

These 8 bit D-Type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

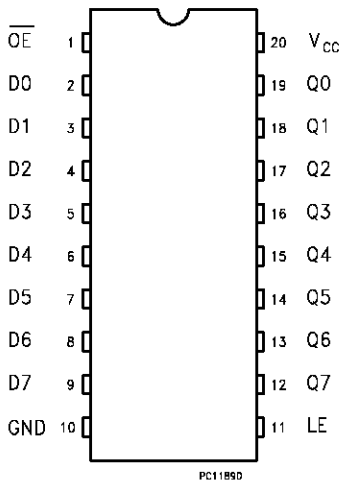
While the LE input is held at a high level, the Q outputs will follow the data input precisely.

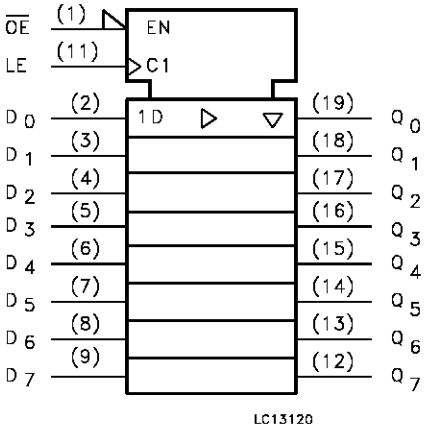
When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data.

While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

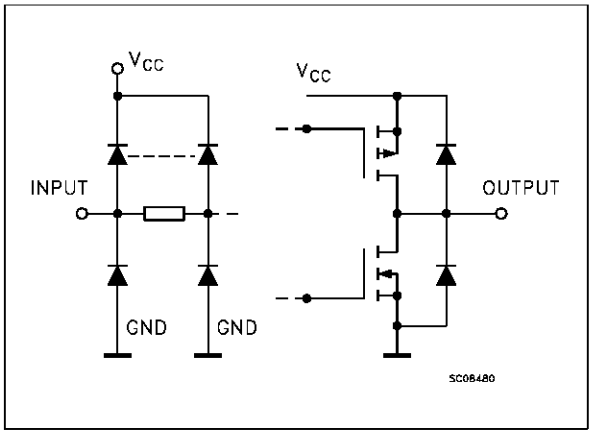
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

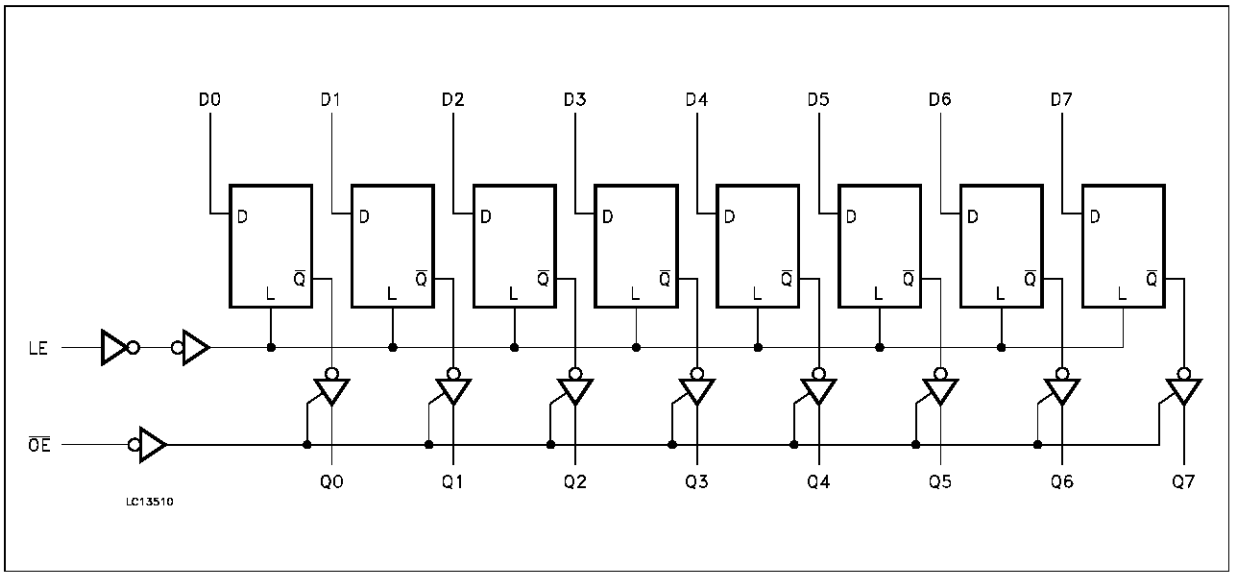
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X: Don't care
Z: High impedance
* Q output are latched at the time when the LE inputs taken low logic level.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	^oC
T_L	Lead Temperature (10 sec)	300	^oC

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	^oC
dt/dv	Input Rise and Fall Time V_{CC} = 3.0, 4.5 or 5.5 V(note 1)	8	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	3.0	V_O = 0.1 V or V_{CC} - 0.1 V		2.1	1.5		2.1		V
		4.5			3.15	2.25		3.15		
		5.5			3.85	2.75		3.85		
V_{IL}	Low Level Input Voltage	3.0	V_O = 0.1 V or V_{CC} - 0.1 V			1.5	0.9		0.9	V
		4.5				2.25	1.35		1.35	
		5.5				2.75	1.65		1.65	
V_{OH}	High Level Output Voltage	3.0	V_I(*) = V_{IH} or V_{IL}	I_O=-50 µA	2.9	2.99		2.9		V
		4.5		I_O=-50 µA	4.4	4.49		4.4		
		5.5		I_O=-50 µA	5.4	5.49		5.4		
		3.0		I_O=-12 mA	2.56			2.46		
		4.5		I_O=-24 mA	3.86			3.76		
		5.5		I_O=-24 mA	4.86			4.76		
V_{OL}	Low Level Output Voltage	3.0	V_I(*) = V_{IH} or V_{IL}	I_O=50 µA		0.002	0.1		0.1	V
		4.5		I_O=50 µA		0.001	0.1		0.1	
		5.5		I_O=50 µA		0.001	0.1		0.1	
		3.0		I_O=12 mA			0.36		0.44	
		4.5		I_O=24 mA			0.36		0.44	
		5.5		I_O=24 mA			0.36		0.44	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3-State Output Off-state Current	5.5	V_I = V_{CC} or GND V_O = V_{CC} or GND $V_{I(OE)}$ = V_{IH}				±0.5		±5	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				8		80	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	5.5	V_{OLD} = 1.65 V max						75	mA
I_{OHD}			V_{OHD} = 3.85 V min						-75	mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.
(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time LE to Q	3.3(*)			6	10		12	ns
		5.0(**)			4.5	8		9	
t_{PLH} t_{PHL}	Propagation Delay Time D to Q	3.3(*)			5.5	10		12	ns
		5.0(**)			4.5	8		9	
t_{PZL} t_{PZH}	Output EnableTime	3.3(*)			6.5	11		13	ns
		5.0(**)			5	9		10	
t_{PLZ} t_{PHZ}	Output Disable Time	3.3(*)			7	12		14	ns
		5.0(**)			6	10		11	
t_w	Clock Pulse Width HIGH or LOW	3.3(*)			1.5	4		4.5	ns
		5.0(**)			1.5	3.5		4	
t_s	Setup Time Q to CK HIGH or LOW	3.3(*)			0.5	3		3.5	ns
		5.0(**)			0	2.5		3	
t_h	Hold Time Q to CK HIGH or LOW	3.3(*)			-0.5	3		3.5	ns
		5.0(**)			0	2.5		3	

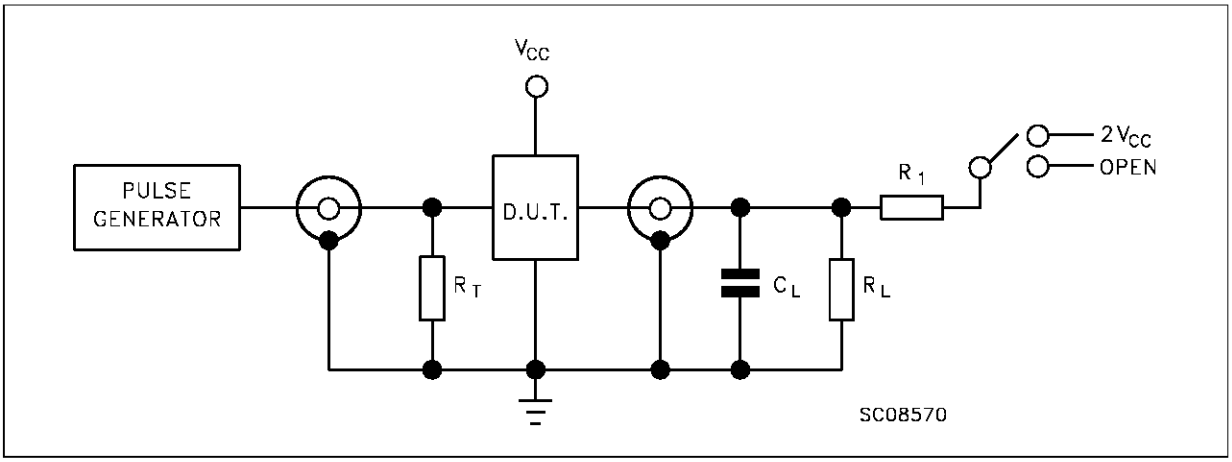
(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C_{OUT}	Output Capacitance	5.0			8				pF
C_{IN}	Input Capacitance	5.0			4				pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			20				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/n$ (per circuit)

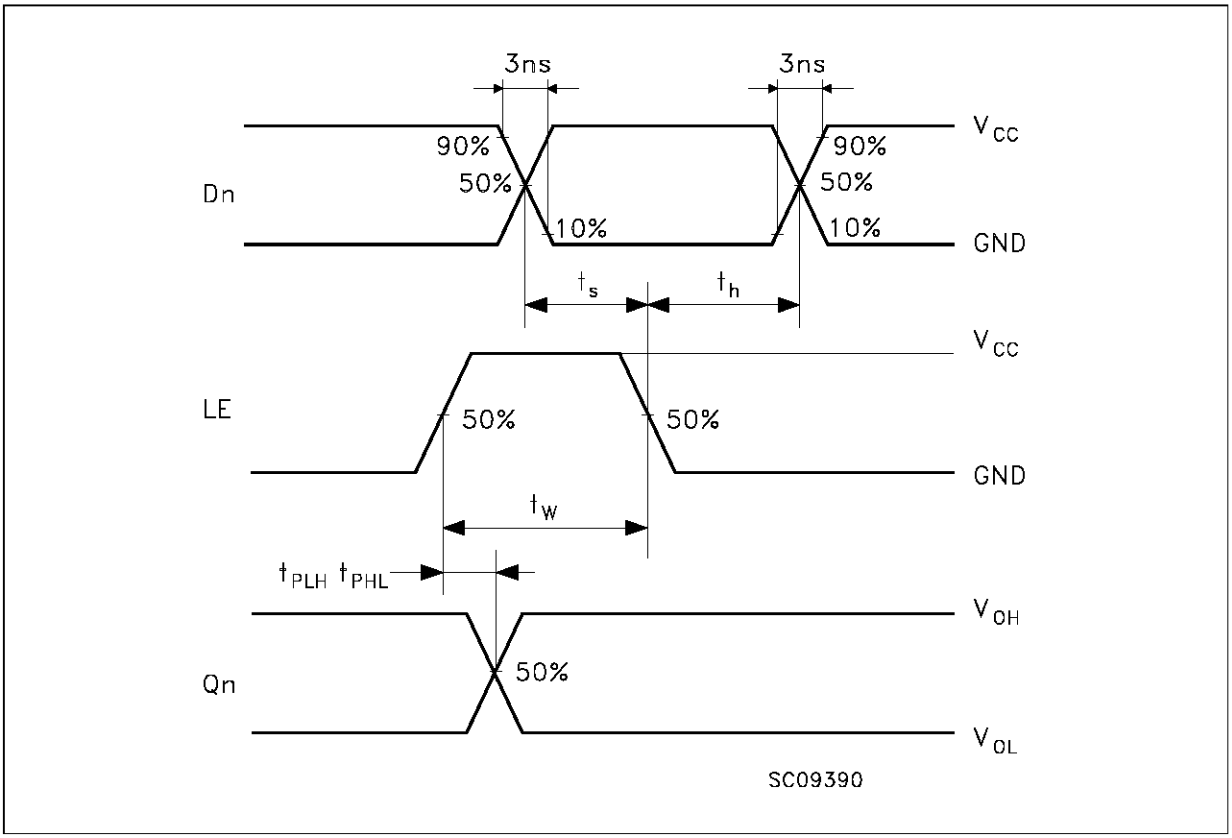
TEST CIRCUIT



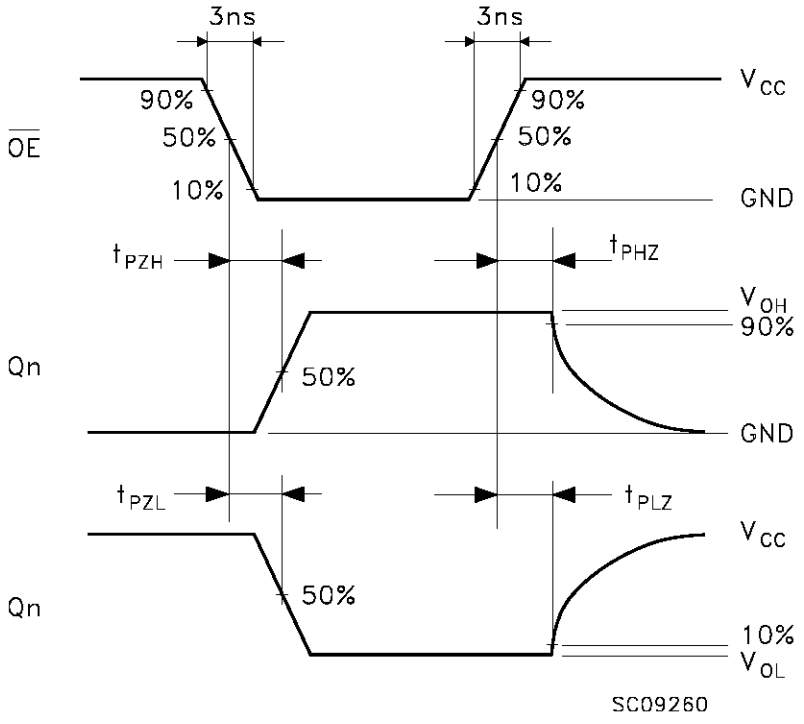
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	Open

C_L = 50 pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

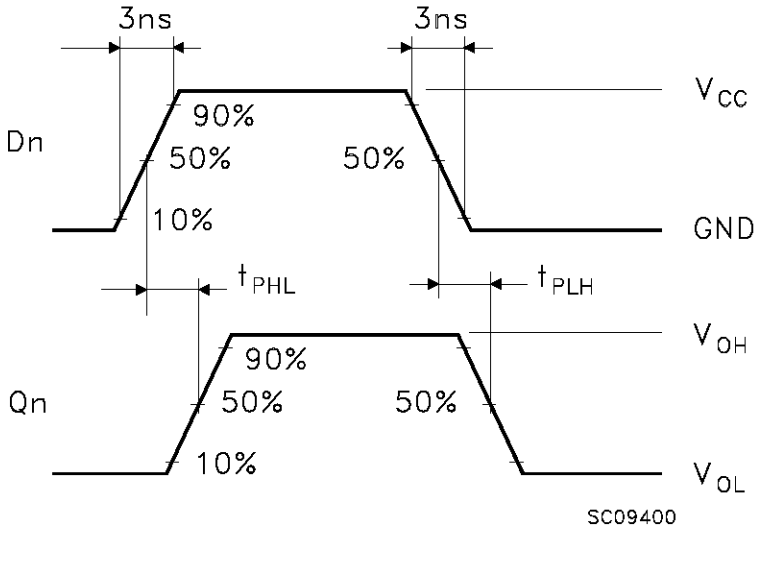
WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

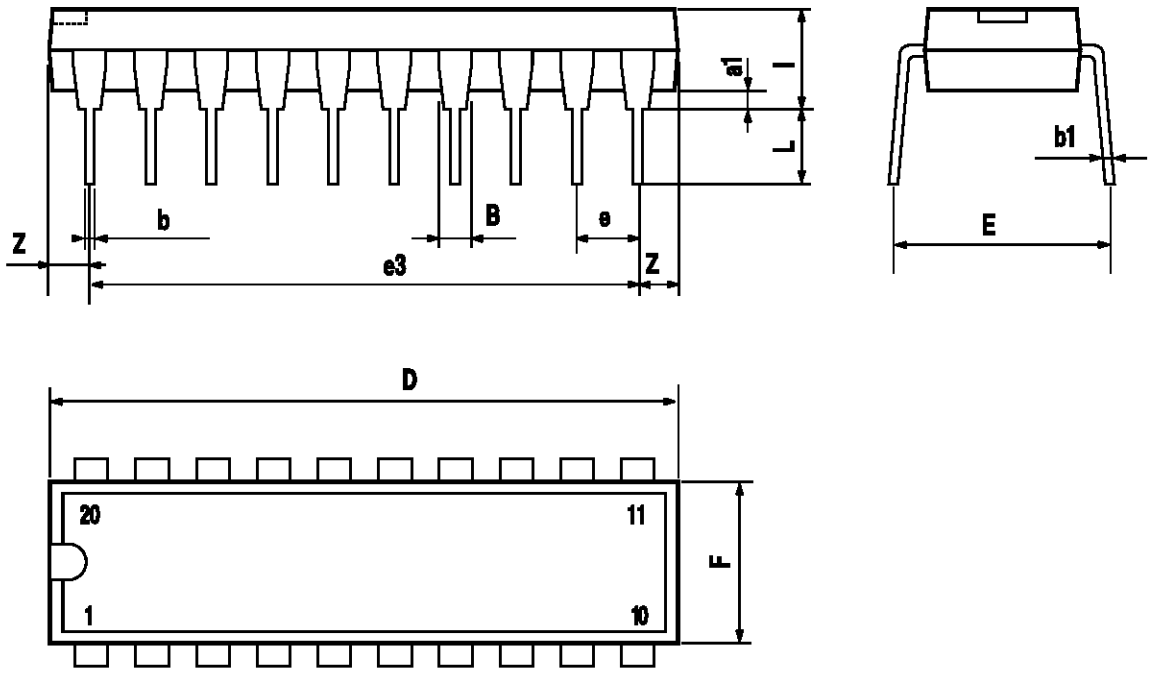


WAVEFORM 3: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



Plastic DIP20 (0.25) MECHANICAL DATA

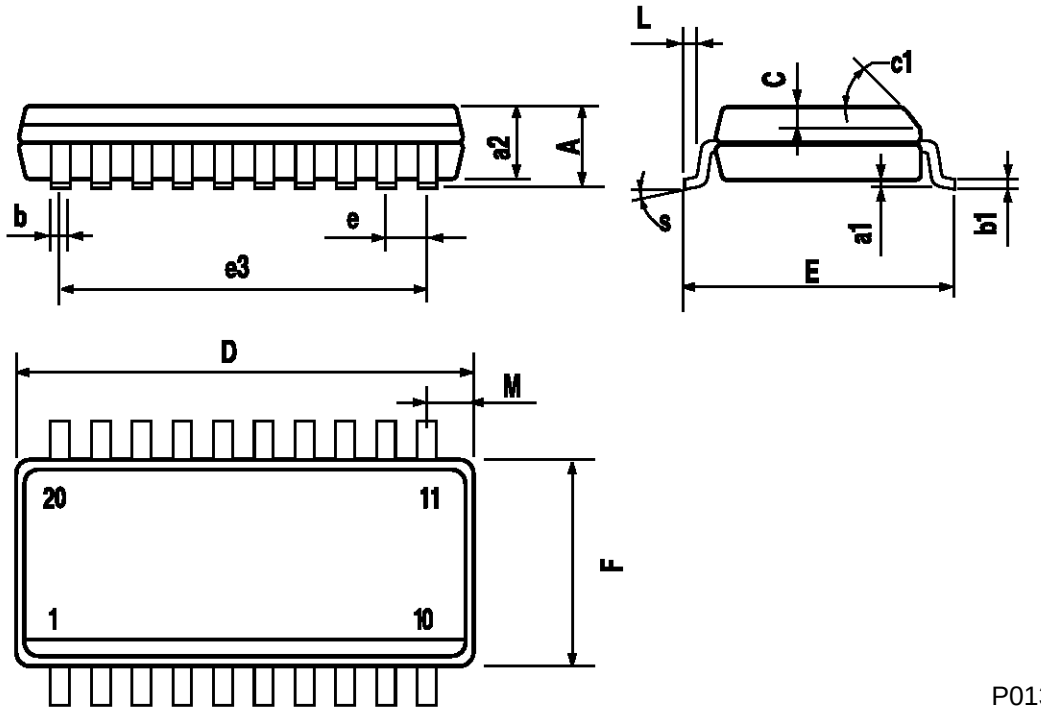
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



P013L